ALICE TPC ELECTRONICS

Charge Sensitive Shaping Amplifier (PASA)

Technical Specifications

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Introduction

The ALICE TPC PASA (**P**re-**A**mplifier **S**haping **A**mplifier) is an Application Specific Integrated Circuit that implements a 16-channel charge sensitive shaping amplifier. This circuit is conceived and optimized to fulfill the requirements set by the readout of the ALICE Time Projection Chamber (TPC) [1].

The ALICE TPC consists of a cylindrical gas volume (about 90 m^3 of Ne-CO_2), divided in two drift regions by a high voltage plane located at its axial centre, under a uniform electrostatic field. At the endplates, conventional Multi-Wire Proportional Chambers provide the charge amplification and readout by means of a cathode plane segmented in about $5.7x10^5$ pads. In the MWPC the signal released on the pads is characterised by a fast rise time (less than 1 ns) and a long tail. The amplitude has a typical value of 7 μA. The signal is delivered on the detector impedance that, to a very good approximation, is a pure capacitance of the order of few pF.

The front-end electronics for the ALICE TPC is built on two basic units: the PASA and the ALTRO chips. The latter [2] is a mixed-signal ASIC that integrates 16 channels, each consisting of a 10-bit 25-MSPS ADC, the baseline subtraction, a filter for the cancellation of the signal tail, the zero suppression and a multi-event buffer. The complete readout chain is contained in Front End Cards (FEC), with 128 channels each, connected to the detector by means of capton cables.

A comprehensive description of the requirements and specifications of the ALICE TPC electronics can be found in [3]. For convenience the main requirements for the PASA circuit are recalled in table. 1.

Parameter	Requirement
Equivalent Noise Charge (electrons)	< 1000 e
Conversion Gain	12 mv / fC
Shaping Time (FWHM)	190ns
Channel-to-Channel Crosstalk	< 0.3%
Non Linearity	< 1%
Gain Dispersion	< 10%
Power Consumption	< 320 mW

Table 1. ALICE TPC requirements for the PASA circuit.

This document describes the technical specifications of the PASA circuit. Chapter 1 gives a general description and the technical specifications of the circuit. Chapter 2 deals with the circuit performance

under different operating conditions, and its sensitivity to the manufacturing process parameters. Eventually, Chapter 3 gives a physical description of the device in terms of circuit layout, package diagram and pinout.

Chapter 1

General Description

The ALICE TPC PASA is an Application Specific Integrated Circuit that implements 16 channels, each consisting of a charge sensitive amplifier combined to a 4th order shaping amplifier. The circuit features a conversion gain (CG) of 12mV/fC, an Equivalent Noise Charge (ENC) of 260e^- (r.m.s.) for 0pF input capacitance, an integral linearity better than 3‰ over a range of input charge up to 150fC, a shaping time (FWHM) of 210ns, a channel-to-channel cross–talk below -60 dB and a power consumption of 120mW. Each of the sixteen channels has a single-ended input and a differential output. As illustrated in fig. 1.1, PASA has an impulse response function described by a Γ_4 function. The PASA requires a single positive supply voltage at 3.3V, and three reference voltages (V_{REFP}, V_{REFM} and V_{CM}), common to all sixteen channels, which define the steady state level of the output signals. The circuit is available in a TQFP 144-pin package.

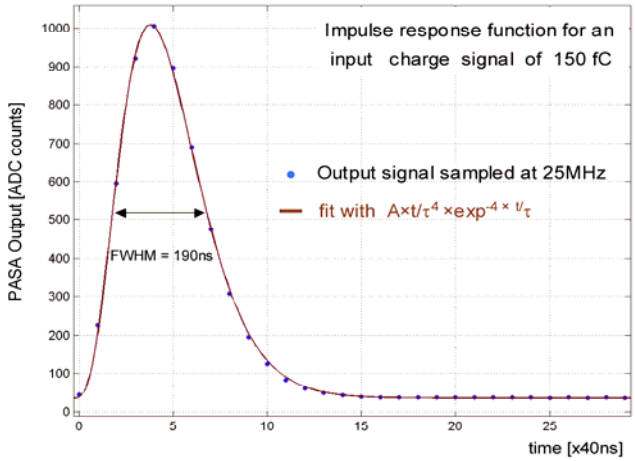

FIGURE 1.1. PASA Impulse Response Function. The picture has been obtained by sampling the PASA output signals at 25MHz with the ALTRO circuit [2]. This measurement was performed on one engineering sample of the ALICE TPC production and with a input capacitance of 0pF. Due to intraprocess and interprocess variations, the shaping time of the circuit is subject to vary within the range ($\pm 3\sigma$) 144ns - 292ns (for 0pF input capacitance). The mean *typical* FWHM has a value of 208ns for a 0pF input capacitance. The circuits produced for the ALICE TPC have a mean value of 190ns, showing that the process parameters for that specific wafer lot are offset towards the *best* case.

Circuit Specifications

For a circuit like the PASA, the precision of the manufacturing process is extremely critical. To determine the extent of such effects, the distribution of various electrical parameters, such as device gain factors and interconnect resistances and capacitances, due to variations in the manufacturing processes must be determined. Once this distribution is known, which is called the design envelope, the design corners can be identified. Besides the variations of the manufacturing process, the circuit parameters are also subject to the operating conditions (mainly temperature and supply voltage). Table 1.1 reports the design corners simulated with SPECTRE under the following conditions:

- The distributions of process parameters provided by the manufacturer (AMS) [4]; for the purpose of determining the design corners, we have been very conservative and assumed that the process parameters can vary within a $\pm 3\sigma$ range (very conservative!).
- Temperature range: 30°C – 50°C;
- Supply voltage range: 3.2V – 3.4V.

A characterization of the statistical variations in the PASA's electrical parameters based on measurements would require a sample consisting drawn from random locations on at least ten wafers that are drawn from different wafers lots. In practice, for the PASA we have a single wafer lot. That is the reason why in table 1.1 we have to refer to the values projected by the simulations.

Note

In semiconductor manufacturing there are two sources of variations: Global variations (lot to lot or wafer to wafer, named also interprocess variations) and Local variations (die to die or intraprocess variations). The distributions of the circuit parameters, which are due to wafer to wafer or die to die variations, are expected to be significantly narrower than those due to lot to lot variations. In particular the CG and the FWHM are expected to have a maximum variation of ±10%.

In Chapter 2 we will describe in some more detail the sensitivity of the circuit to the manufacturing process parameters as well as to the operating conditions: temperature, supply voltage and input capacitance.

PARAMETER	OPERATING CONDITIONS	MIN	TYP	MAX
ENC	C_{INPUT} = 0pF	250 e	260 e	275 e
ENC	C_{INPUT} = 12pF	371	397 e	410 e
ENC	C_{INPUT} = 25pF	589 e	616 e	630 e
dENC/ **d**C_{IN} For C_{IN}> 5pF		16.8 e/pF		
Conversion Gain		11.6mV/fC	12.74 mV/fC	13.7mV/fC
Input Range		165 fC		
Differential Output Range	T = 30 °C, V_{supply} = 3.3V	1914 mV	2100 mV	2260
AC Input Impedance		-	500 Ω	-
AC Output Impedance		-	300 Ω	-
Output Maximum Capacitive Load		-	14 pF	-
Integral Non-linearity	-	0.14 %	0.19 %	0.34 %
Shaping Time FWHM	C_{INPUT} = 25pF	152 ns	217 ns	301 ns
Variation of diff. output dc level	T = 30 °C, V_{supply} = 3.3V	-	120 mV	-
Power Consumption	V_{supply} = 3.3V	128 mW	192 mW	320 mW
Supply Voltage	-	3.2V	3.3V	3.4V

TABLE1.1. PASA design corners simulated with SPECTRE: ±3σ variations in process parameters, temperature in the range 30°C – 50°C (typical corresponds to 40°C), and supply voltage in the range +3.2V – 3.4V (typical corresponds to 3.3V).

Block Diagram

Figure 1.2 illustrates the architecture of one channel. The circuit consists of a Charge Sensitive Amplifier (CSA), followed by a Pole-Zero Cancellation network and two 2nd order T-bridge RC shapers.

Charge Sensitive Amplifier and Pole-Zero Cancellation

The CSA is based on a *Folded Cascode* amplifier. Its feedback consists of a capacitance C_F that is continuously discharged over a feedback MOS transistor (M_F). The discharge has a time constant $T_d=C_F \bullet R_{ds}(M_F)$, where R_{ds} is the channel's resistance of the feedback transistor M_F. The nominal values of C_F and R_{ds} are respectively 500fF and 10MΩ, yielding a time constant T_d= 5μs. The feedback transistor M_F is biased in the triode region by using a Self-Adaptive Bias technique [5]. This technique allows biasing M_F in the MΩ region, essential to keep low the contribution to the noise, while tracking process, temperature, supply voltage variations, and preserve good gain linearity despite of the presence of a non-linear resistance in the feedback. It should be noticed that the MOS transistor M_{zero} is biased in the same way as M_F during the discharge of C_F. Therefore, the zero associated to the network M_{zero}-C_1, adapts itself dynamically to accurately cancel the pole associated to the network C_F-M_F. The CSA has an AC input impedance of about 500Ω and an open-loop gain of about 80dB.

4th Order Shaping Amplifier. 1st filter

THE FIRST FILTER is based on a Folded Cascode amplifier with the same topology as the one employed in the CSA.The T-bridge network on the feedback generates two poles and one zero. In order to minimize the variations of the DC level of the shaper output signal caused by variations of the process parameters and operating conditions, a "dummy" folded cascade amplifier with a unity gain configuration is part of is part of the first filter to feed the second stage with in differential mode. The first filter has an open-loop gain of about 75dB.

4th Order Shaping Amplifier. 2nd filter

THE SECOND FILTER is based on a fully differential folded cascade circuit. This second stage of the shaper, besides implementing two other poles and one zero that together with the first stage implant a semi-Gaussian CR-RC^4, has the function to split the single-ended single-polarity input in a pair of differential signals centred on the common-mode voltage.

Output Stage

A Common-Mode FeedBack circuit (CMFB), which is connected to the output of the second filter, holds the common mode of the output signals to the external reference voltage V_{CM}. The CMBF circuit probes the mean value between Vout+ and Vout- (generated by a network of two resistors and two capacitors). Any deviation from V_{CM} is fed back to the 2nd filter and corrected. This scheme ensures a fully balanced differential output over a voltage range limited by the Common Mode Range (CMR) of the output stage of the 2nd filter.

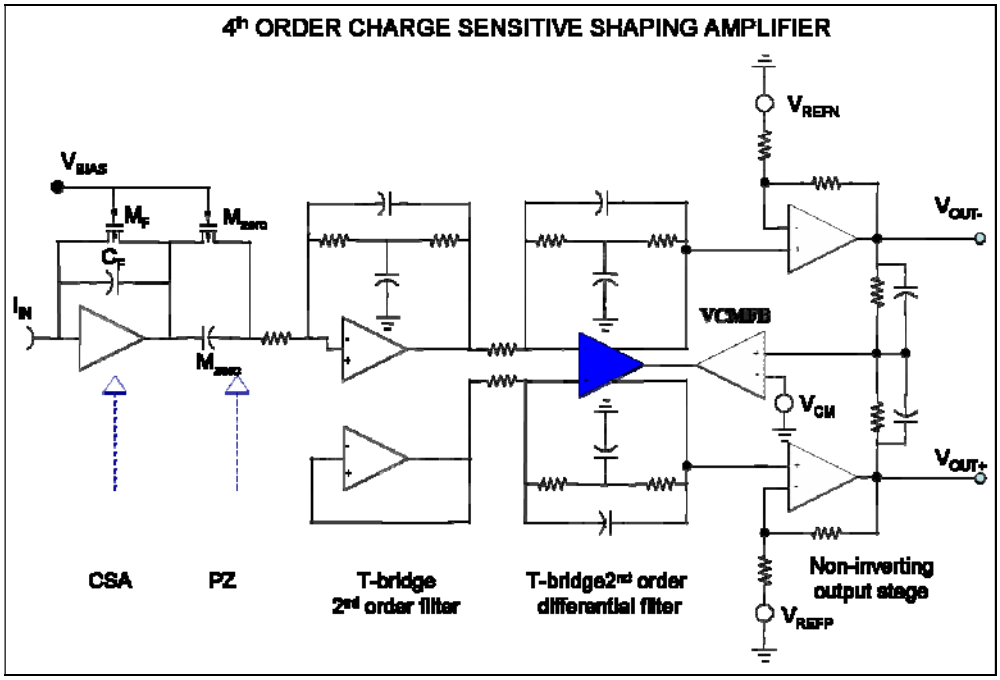

FIGURE 1.2. Architecture of one single channel.

Chapter

2

Typical Characterization Curves

This chapter describes the some of the characteristic curves of the PASA circuit. The emphasis is put on the variation of the PASA characteristic parameters as function of the operating and process parameters. The PASA is implemented in the 0.35μm CMOS process (C35B3C1) featured by Austria Microsystems (AMS). As any other semiconductor process, the C35B3C1 parameters are subject interprocess (lot-to-lot and wafer to wafer) and intraprocess (die to die) variations. Theses variations results in variations of the basic parameters of the passive (resistors and capacitors) and active (transistors) devices. A detailed description of the dispersion of the process parameters is beyond the scope of this document and can be found in [4]. Nevertheless, to give the reader a hint of the extent of the variations to be expected, we report in table 2.1, the maximum deviations, with respect to the design values, of resistors, capacitors and threshold voltage of the transistors.

AMS 0.35mm CMOS Process (C35B3C1) Variations	
Resistor	25%
Capacitor	10%
Transistor Threshold Voltage	25%

TABLE2.1. Maximum deviation of the characteristic device parameters due to the variation of the process parameters.

Though the circuit employs some techniques to minimize the effect of the variation of the process parameters, the later has an important effect on the circuit parameters.

Impulse Response Function

The impulse response function is the response of the circuit to an input current delta pulse. As seen in figure 1.1, which shows the PASA response digitized by the ALTRO circuit, the PASA impulse response function is very well approximated by a Γ_4 function. Figure 2.1 shows the PASA impulse response function for each of the two output signals (V_{OUTP} and V_{OUTN}). Figure 2.2 shows the PASA differential response function ($V_{OUTP} = V_{OUTP} - V_{OUTN} + 1V$). The curves plotted in figures 2.1 and 2.2 are valid for *typical* values of the process parameters, temperature and supply voltage. Fig.2.3 shows the differential impulse response signal for 8 different *corners* of the circuit envelope. These 8 corners, which are built combining *worst*, *typical*, and *best* values of *process parameters*, *temperature* and *supply voltage*, are representative of the entire design envelop.

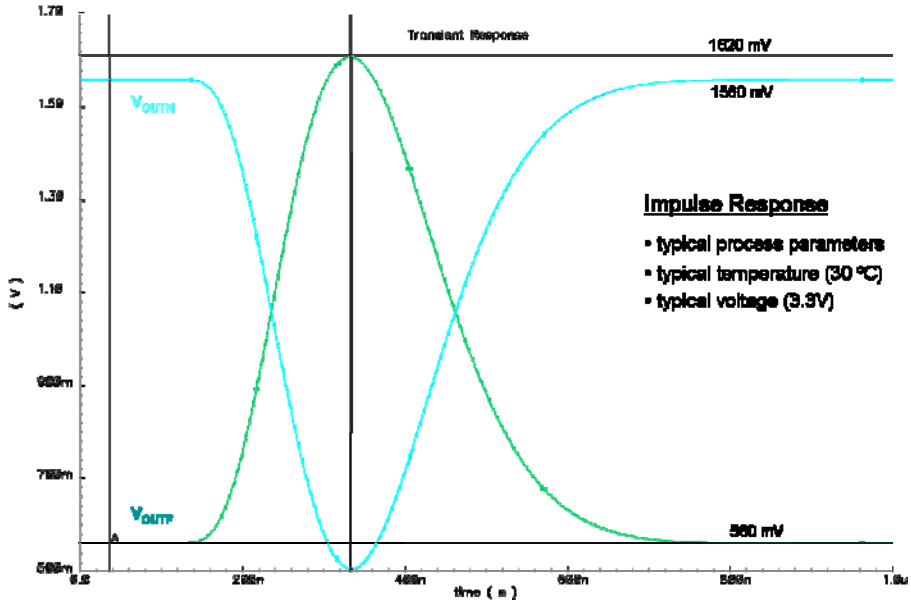

FIGURE 2.1. PASA impulse response function: in green the output signal with positive polarity (V_{OUTP}); in sky-blue the output signal with negative polarity (V_{OUTN}). In steady state *typical* values of V_{OUTP} and V_{OUTN} are 560mV and 1560mV respectively.

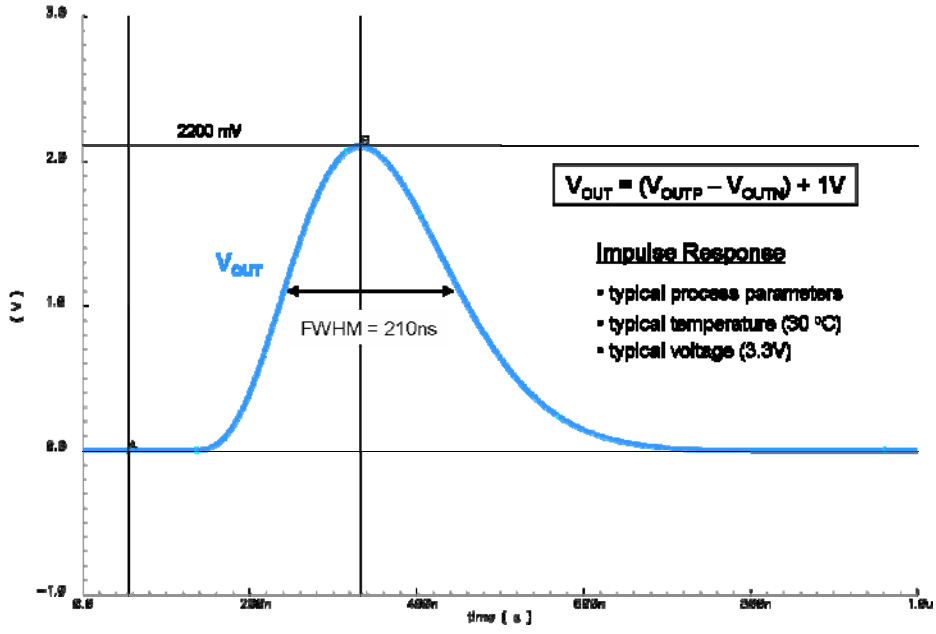

FIGURE 2.2. PASA differential impulse response function for typical values of process and operating parameters: the blue curve is the plot of $V_{OUT} = (V_{OUTP} - V_{OUTN}) + 1V$. in this plot, the output signal covers the full dynamic range of the PASA.

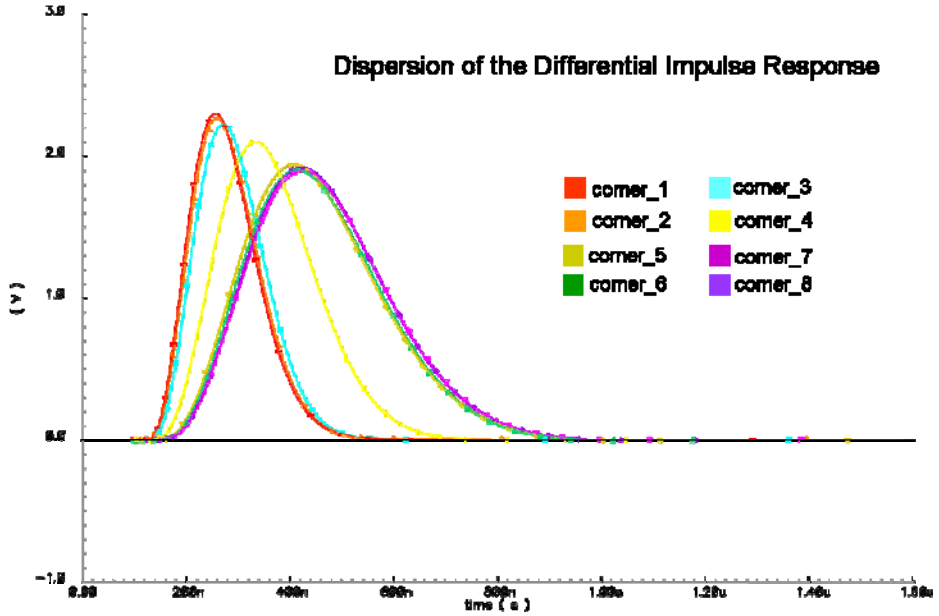

FIGURE 2.3. PASA impulse response signal for 8 different combinations of process parameters, temperature and supply voltage. Concerning the process parameters, the analysis takes into account the most unfavorable variations of resistance, capacitance, NMOS and PMOS devices. For the temperature it is considered a variation in the range 30ºC – 50ºC. For the supply voltage variations in the range 3.2 V – 3.4V.

As already mentioned, the impulse response function is well approximated by a Γ_4 function. The latter is characterized completely by the conversion gain (CG) and the full width half maximum (FWHM). These parameters both depend on the circuit input capacitance C_{IN}. Table 2.1 tabulates the variations of CG and FWHM as function of the input capacitance for *best*, *typical* and *worst* cases.

PARAMETER	**CONDITIONS**	**C_{IN}**	
		0pF	25pF
CONVERSION GAIN	Best	14.3 mV/fC	13.7 mV/fC
	Typical	13.3 mV/fC	12.7 mV/fC
	Worst	12.1 mV / fC	11.6 mV/fC
FWHM	Best	144 ns	151 ns
	Typical	208 ns	217 ns
	Worst	292 ns	306 ns

TABLE 2.2. Variations of conversion gain (CG) and shaping time (FWHM) for two different values of the input capacitance (C_{IN}) and the three standard *best*, *typical* and *worst* conditions.

Figure 2.4 plots the conversion gain for six different values of the input capacitance C_{IN}.

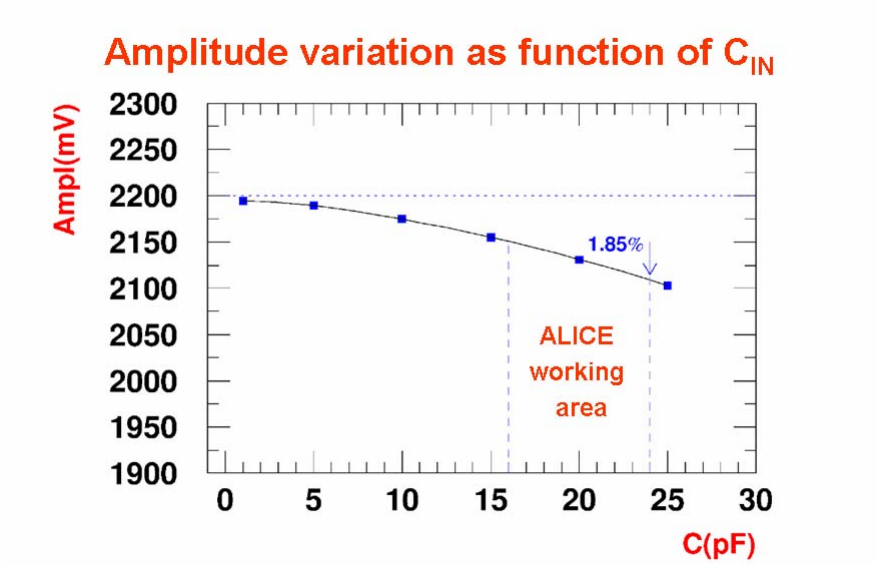

FIGURE 2.4. Amplitude of the PASA impulse response signal as function of the input capacitance C_{IN},over the range 1pF – 25pF.

Output Signals DC Levels

The PASA's differential output signals, V_{OUTP} and $V_{OUTN,}$ have a DC steady state defined by three reference voltages: a positive reference voltage (V_{REFP}), a negative reference voltage (V_{REFN}) and a common mode reference voltage (V_{CM}). V_{CM} should be set to V_{REFN} + (V_{REFP} - V_{REFN})/2. Within the ranges indicated in table 2.3, nominally V_{OUTP} and V_{OUTN} should be equal to V_{REFP} and V_{REFN} respectively. Table 2.3 shows the maximum range of values for the three reference voltages.

REF. VOLTAGE	MIN	TYP	MAX
V_{REFP}	400mV	560mV	720mV
V_{CM}	740mV	1060mV	1380mV
V_{REFN}	1400mV	1560mV	1720mV

TABLE 2.3. Specifications for the output stage reference voltages V_{REFP}, V_{CM}, V_{REFN}.

Figure 2.5, 2.6 and 2.7 show how the output signals V_{OUTP} and V_{OUTN} depend on the reference voltages V_{REFP}, V_{CM} and V_{REFN}.

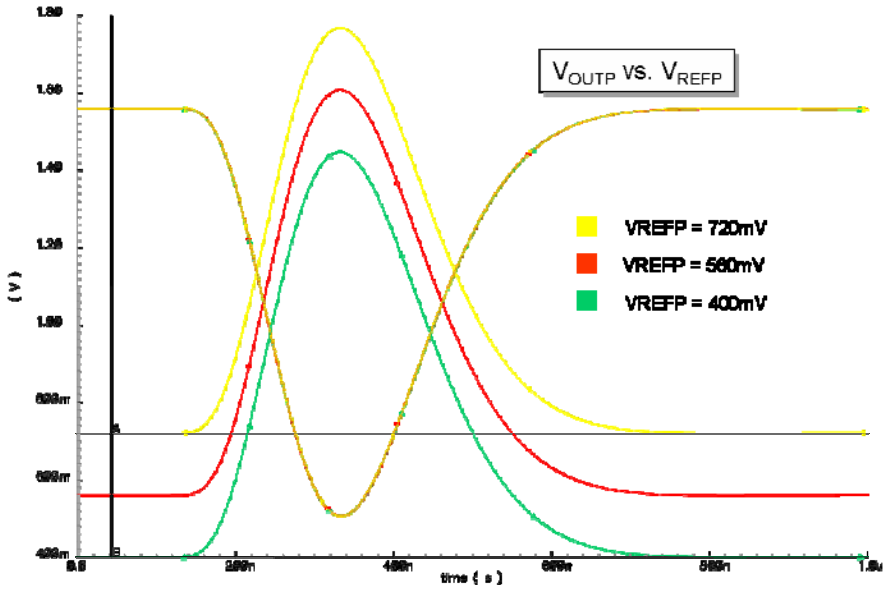

FIGURE 2.5. Range of variation of V_{REFP} and corresponding variation of V_{OUTP}.

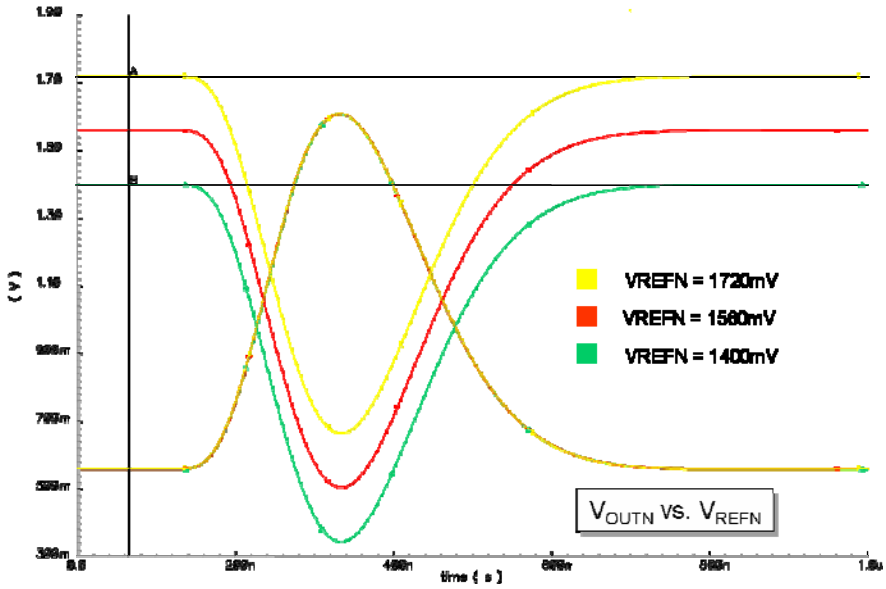

FIGURE 2.6. Range of variation of V_{REFN} and corresponding variation of V_{OUTN}.

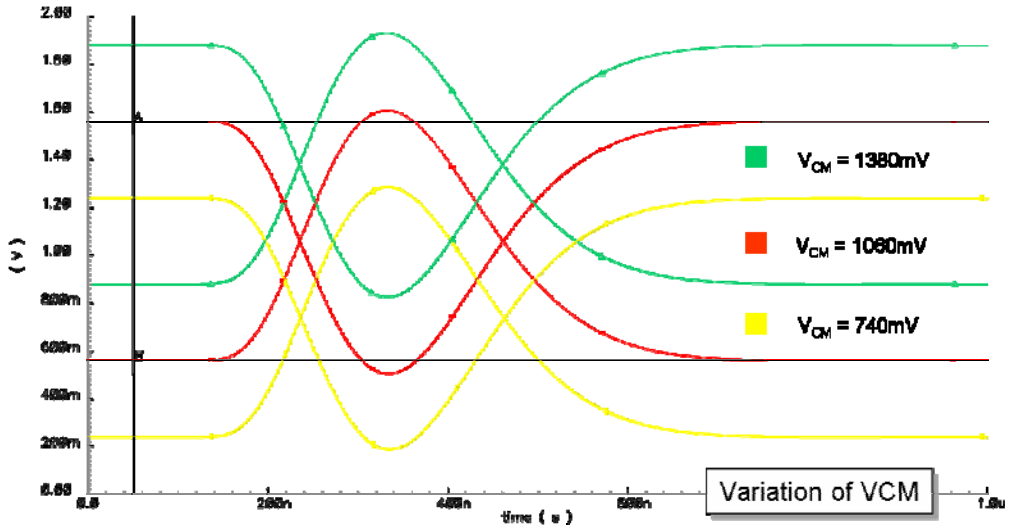

FIGURE 2.7. Range of variation of VCM and corresponding variation of VOUTP and VOUTN.

Chapter

3

Physical Description

The PASA has 16 pins for the input signals, 32 pins for the output signals, 3 pins for the reference voltages, 14 GND pins and 8 VDD pins for a total of 73 pins. However, as can be seen in figure 3.4, the pads are all placed on two opposite edges of the silicon die. Therefore, in order to allow a proper bonding between the pads on the silicon die and the package leads, the circuit has been packaged in a TQFP-144 package. The package outline is shown in figure 3.1, while table 3.1 lists all pins with short descriptions. Figure 3.2 shows the Cadence pin diagram (Concept symbol) used for electrical schematic drawings. Eventually figure 3.4 shows the circuit layout.

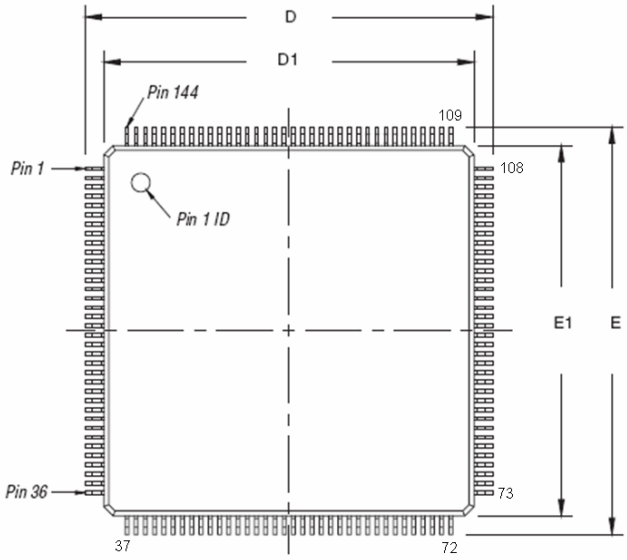

FIGURE 3.1. PASA package outline (TQFP 144). The dimensions are: D=E=22mm and D1 = E1 = 20mm.

PIN NAME	PIN NUMBER	DESCRIPTION
IN0	1	Input signal to channel 0
GND0	2	Ground
IN1	3	Input signal to channel 1

GND1	4	Ground
IN2	5	Input signal to channel 2
GND2	6	Ground
IN3	7	Input signal to channel 3
GND3	8	Ground
IN4	9	Input signal to channel 4
GND4	10	Ground
IN5	11	Input signal to channel 5
GND5	12	Ground
IN6	13	Input signal to channel 6
GND6	14	Ground
IN7	15	Input signal to channel 7
NC	16	Not connected
VDDa	17	3.3V Supply Voltage
VDDb	18	3.3V Supply Voltage
VDDc	19	3.3V Supply Voltage
VDDd	20	3.3V Supply Voltage
NC	21	Not connected
IN8	22	Input signal to channel 8
GND7	23	Ground
IN9	24	Input signal to channel 9
GND8	25	Ground
IN10	26	Input signal to channel 10
GND9	27	Ground
IN11	28	Input signal to channel 11
GND10	29	Ground
IN12	30	Input signal to channel 12
GND11	31	Ground
IN13	32	Input signal to channel 13
GND12	33	Ground
IN14	34	Input signal to channel 14
GND13	35	Ground
IN15	36	Input signal to channel 15

VDDe	37	3.3V Supply Voltage
NC	38, 39, …, 71	Not connected
VDDf	72	3.3V Supply Voltage
NC	73	Not connected
OUT15+	74	Positive polarity Output signal of channel 15
OUT15-	75	Negative polarity Output signal of channel 15
OUT14+	76	Positive polarity Output signal of channel 14
OUT14-	77	Negative polarity Output signal of channel 14
OUT13+	78	Positive polarity Output signal of channel 13
OUT13-	79	Negative polarity Output signal of channel 13
OUT12+	80	Positive polarity Output signal of channel 12
OUT12-	81	Negative polarity Output signal of channel 12
OUT11+	82	Positive polarity Output signal of channel 11
OUT11-	83	Negative polarity Output signal of channel 11
OUT10+	84	Positive polarity Output signal of channel 10
OUT10-	85	Negative polarity Output signal of channel 10
OUT9+	86	Positive polarity Output signal of channel 9
OUT9-	87	Negative polarity Output signal of channel 9
OUT8+	88	Positive polarity Output signal of channel 8
OUT8-	89	Negative polarity Output signal of channel 8
V_{REFP}	90	Reference Voltage for Positive output signals
V_{CM}	91	Reference Voltage for the output signals Common Mode
V_{REFN}	92	Reference Voltage for Negative output signals
OUT7-	93	Negative polarity Output signal of channel 7
OUT7+	94	Positive polarity Output signal of channel 7
OUT6-	95	Negative polarity Output signal of channel 6
OUT6+	96	Positive polarity Output signal of channel 6
OUT5-	97	Negative polarity Output signal of channel 5
OUT5+	98	Positive polarity Output signal of channel 5
OUT4-	99	Negative polarity Output signal of channel 4
OUT4+	100	Positive polarity Output signal of channel 4
OUT3-	101	Negative polarity Output signal of channel 3
OUT3+	102	Positive polarity Output signal of channel 3

OUT2-	103	Negative polarity Output signal of channel 2
OUT2+	104	Positive polarity Output signal of channel 2
OUT1-	105	Negative polarity Output signal of channel 1
OUT1+	106	Positive polarity Output signal of channel 1
OUT0-	107	Negative polarity Output signal of channel 0
OUT0+	108	Positive polarity Output signal of channel 0
VDDAg	109	3.3V Supply Voltage
NC	110, 111, …, 143	Not connected
VDDh	144	3.3V Supply Voltage

TABLE 3.1. PASA PINOUT

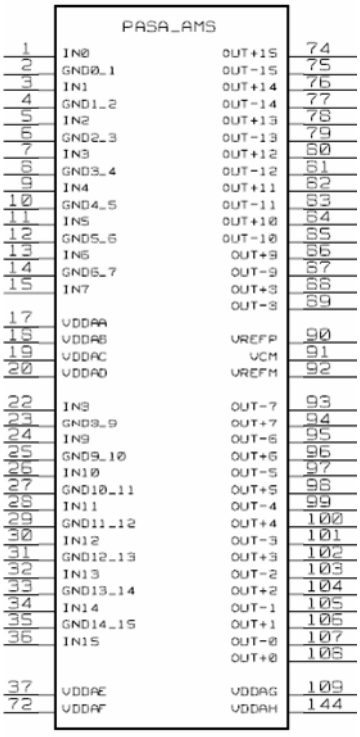

FIGURE 3.2. CADENCE (Concept) symbol for electrical schematic drawings.

Figure 3.3 shows a possible implementation of the circuit for the generation of the reference voltages V_{REFP}, V_{REFN}, V_{CM}.

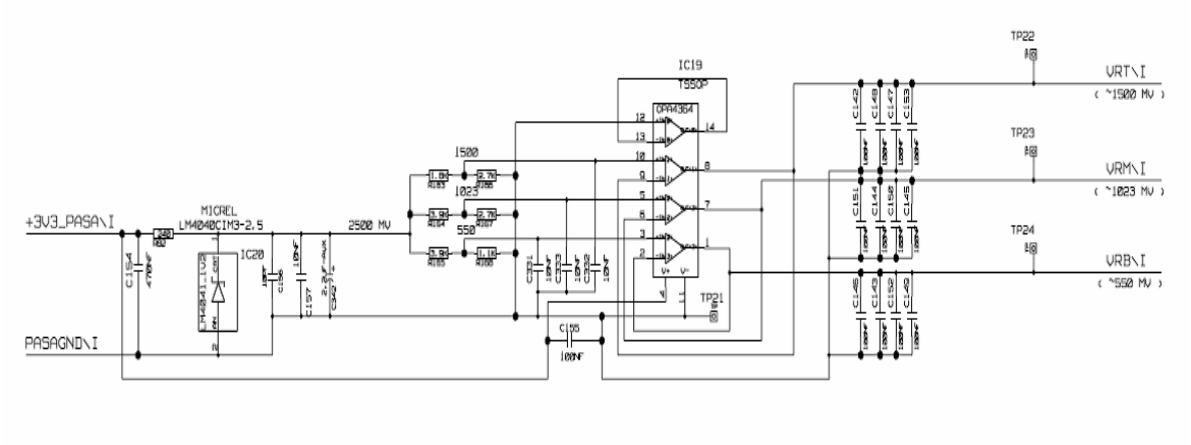

FIGURE 3.3. Circuit that has been used in the ALICE TPC Front End Card for the generation of the PASA's reference Voltages. In this diagram VRT stays for V_{REFP}, VRM for V_{CM} and VRB for V_{REFN}.

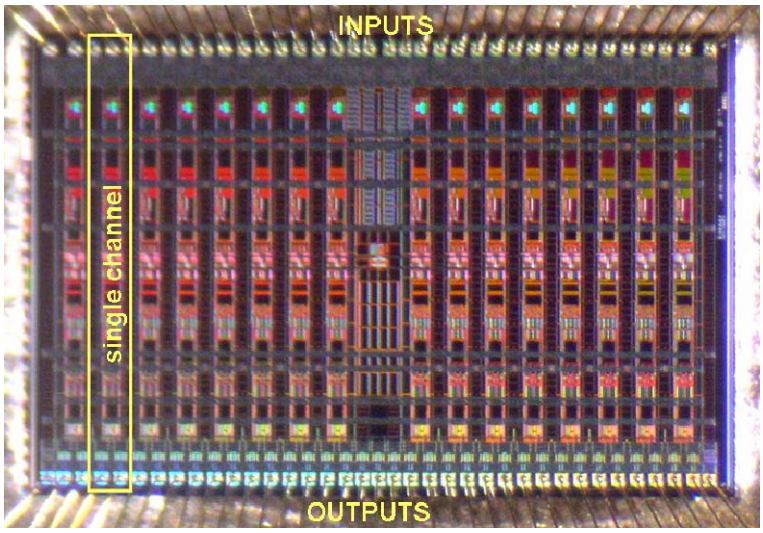

FIGURE 3.4. Layout of the PASA silicon die. The circuit has an area of 18mm^2

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