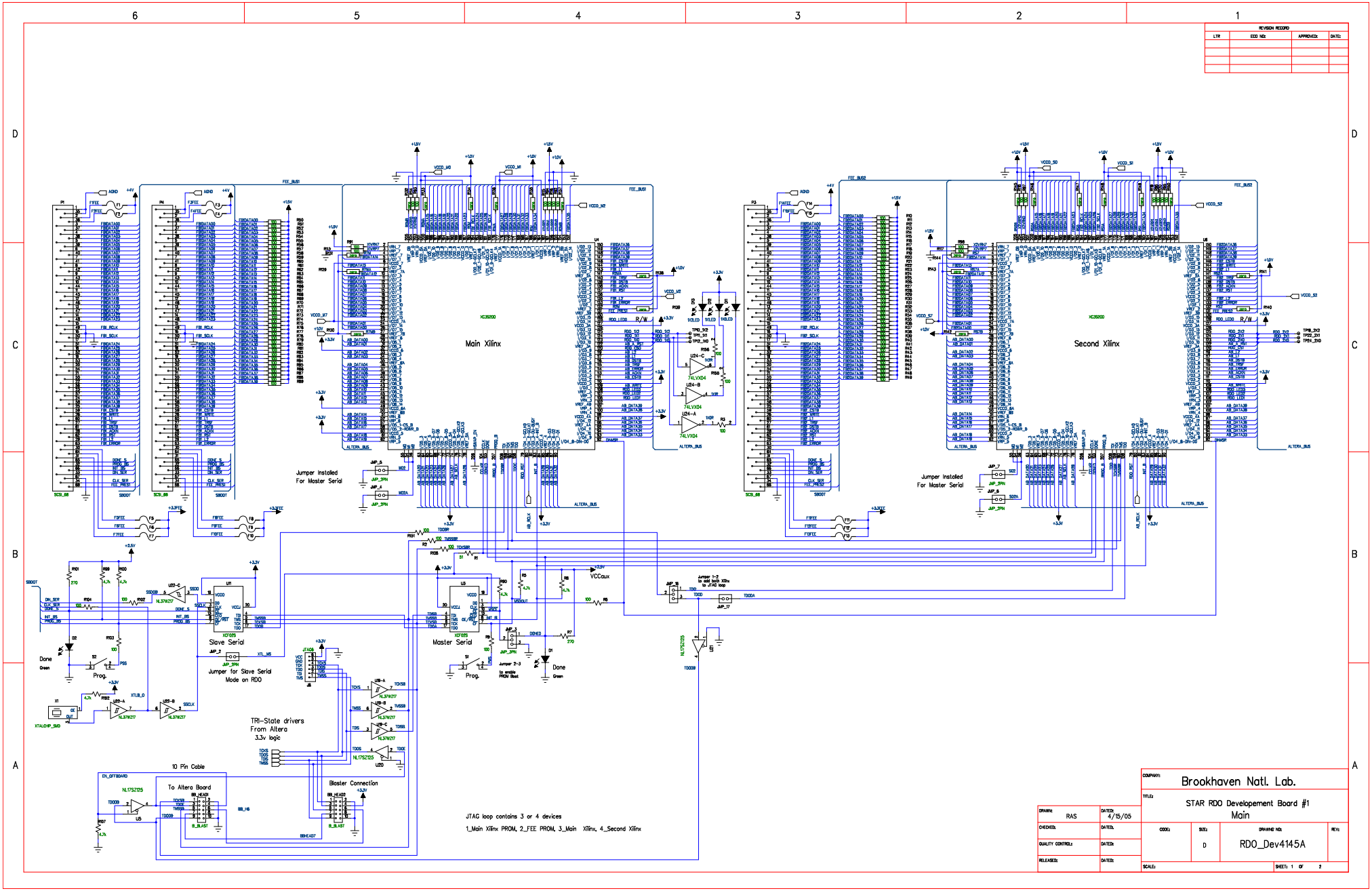
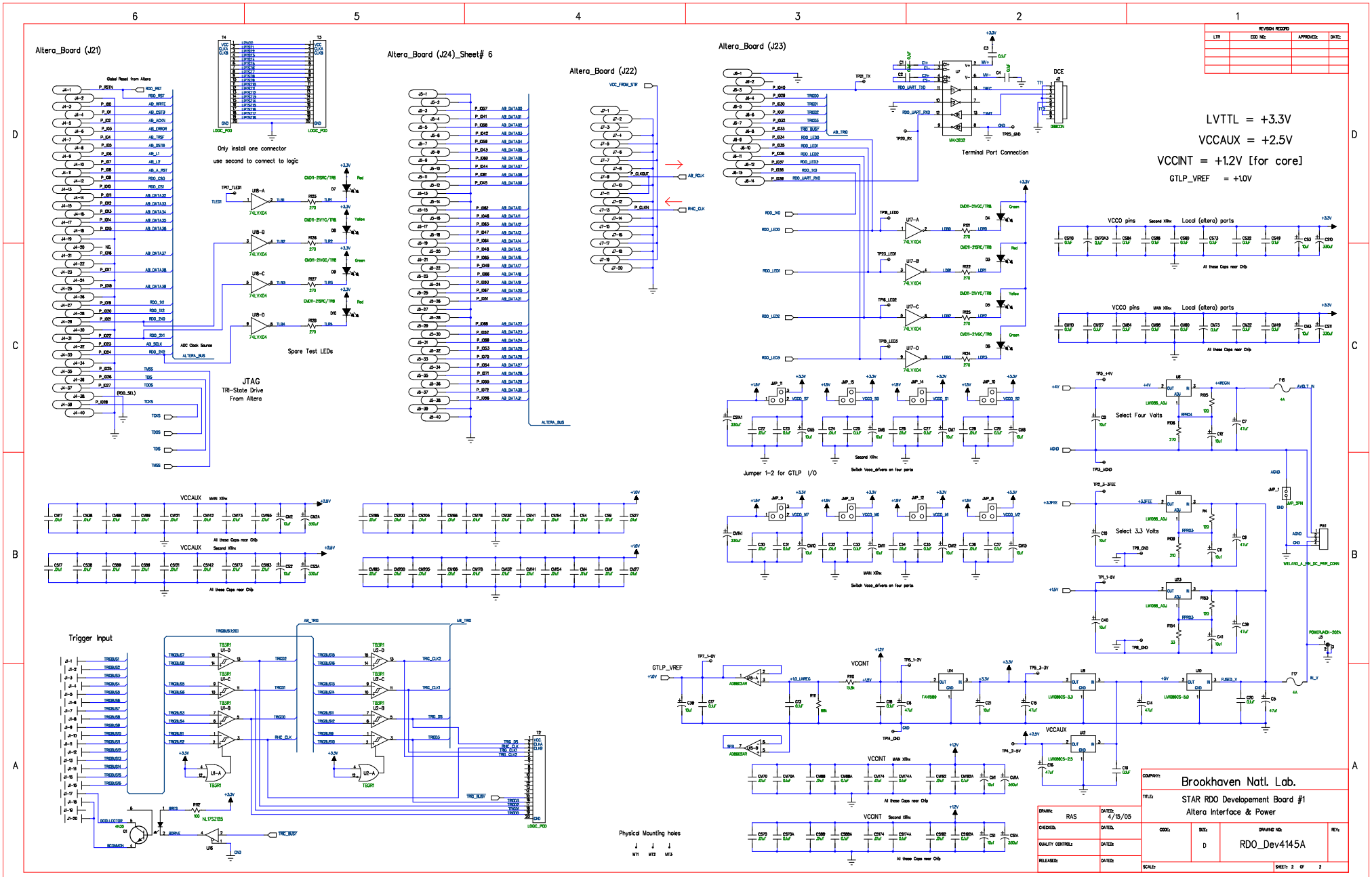

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
Main Xilinx
Second Xilinx
Jumper Installed
For Master Serial
Slave Serial
Jumper for Slave Serial
Mode on RDO
Master Serial
Prog.
Done
Green
TRI-State drivers
From Altera
3.3v logic
10 Pin Cable
To Altera Board
Blaster Connection
JTAG loop contains 3 or 4 devices
1_Main Xilinx PROM, 2_FEE PROM, 3_Main Xilinx, 4_Second Xilinx
COMPANY:
Brookhaven Natl. Lab.
TITLE:
STAR RDO Developement Board #1
Main
DRAWN:
RAS
DATE:
4/15/05
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
D
DRAWING NO:
RDO_Dev4145A
REV:
SCALE:
SHEET: 1 OF 2


Altera_Board (J21)
Altera_Board (J24)_Sheet# 6
Altera_Board (J22)
Altera_Board (J23)
Only install one connector
use second to connect to logic
Spare Test LEDs
JTAG
TRI-State Drive
From Altera
Terminal Port Connection
LVTTL = +3.3V
VCCAUX = +2.5V
VCCINT = +1.2V [for core]
GTLP_VREF = +1.0V
Jumper 1-2 for GTLP I/O
Select Four Volts
Select 3.3 Volts
Trigger Input
Physical Mounting holes
Brookhaven Natl. Lab.
STAR RDO Developement Board #1
Altera Interface & Power
RDO_Dev4145A