STAR DAQ 1000 Readout Board Prototype

User's Manual

Rev 2.0

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Overview

The First prototype RDO development board will be used to test initial concepts of various bus driver types and general design features and limitations. This first prototype is a daughter board to the commercial Board (Microtronic Stratix) that contains the Altera chip and a bidirectional optical link module.

In the next version of the RDO development phase, the Altera part and the fiber link module will be moved to the RDO board. The development boards will have logic probe connections and multiple test points with LED indicators.

Description

The first RDO board has two Xilinx FPGA parts (XC3S200) that are used as bidirectional ports for cable drivers to the FEE cables. The "main" part has two 68-pin connectors attached while the secondary part only has one 68-pin connector. These two parts will normally be programmed at power up with the same code from a Xilinx PROM (XCF02S). A second XCF02S on this board will be used to program the Xilinx FEE parts connected by the 68 pin ribbon cables. A JTAG string, which can be accessed by three different sources, is also available for part configuration and can program the local FPGAs directly.

Features

A. Boot options to select mode for Slave Serial or Master Serial at power up time for Xilinx FPGA's on this board. Remote FPGA's on the FEE boards are always programmed in Slave Serial mode.

B. JTAG testing and configuration of parts on both mother and daughter boards are supported. The JTAG string is automatically extended to include the devices on the Altera board when a 10-pin jumper cable is installed between the two boards. The JTAG string contains buffer resistors and drivers to deal with the 2.5v and 3.3v used by the different parts in the string.

C. Options to test different Driver protocols for the FEE cables have been implemented. Jumpers are provided to change the I/O voltage on these ports

Open questions

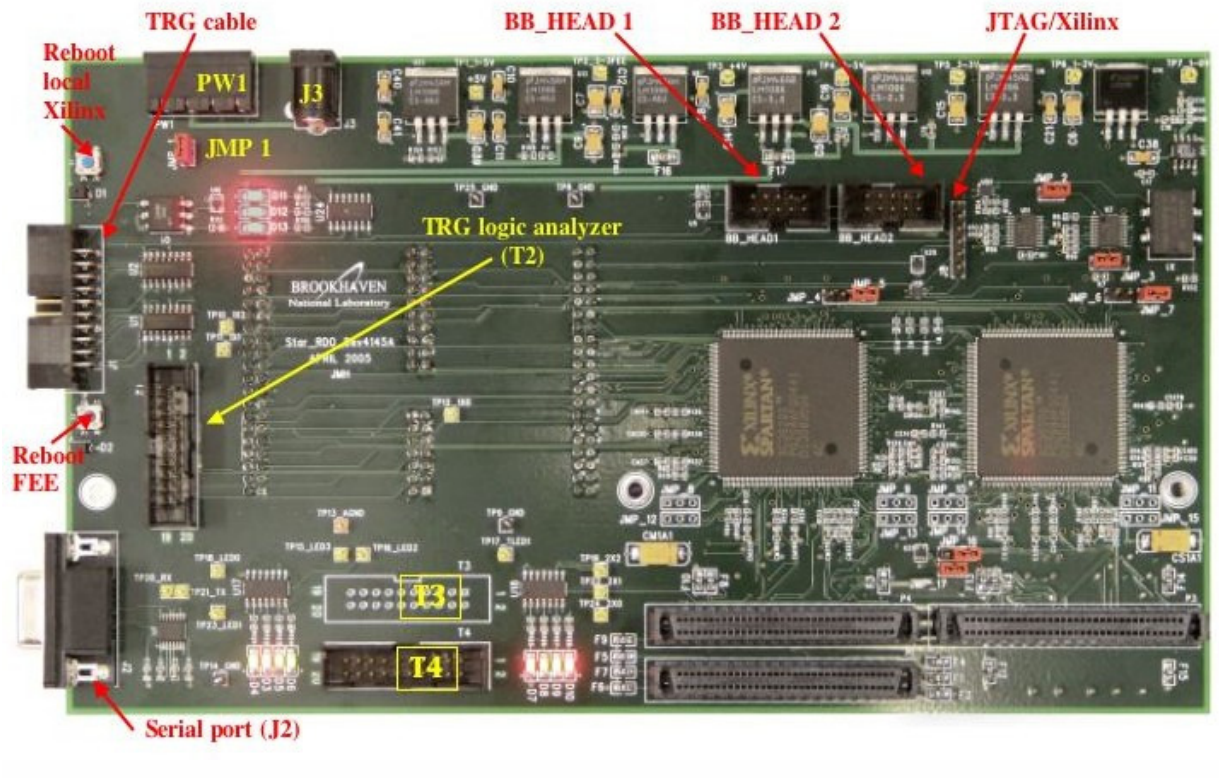
- Terminations on GTL cables: On each cable there are two FEEs, each with a Xilinx. They sit on the same cable, and terminate the cable with a configurable (soldered) resistor. If they are both correctly terminated, will the double

termination bother the data sent from RDO to the FEEs? Is the termination active only when the device is active on the GTL bus?

Board layout

There is a full-page drawing of the board in Appendix A.

Connectors and Pushbuttons



Logic Analyzer headers

There are two logic analyzer headers provided:

- T2 provides access to the trigger signals
- T3 is uncommitted. Each signal is connected to a test block (T4) which may be connected to any signal of interest.

Serial port connector

J2 provides the connection to the Stratix serial port.

Power supply connections

Power plug PW1 provides +4V for the analog circuitry on the FEE cards. It has a separate ground. It also provides +DC which should be greater than 5V.

JMP 1: (**1-2**) Connect the analog and logic grounds together
Else: no jumper

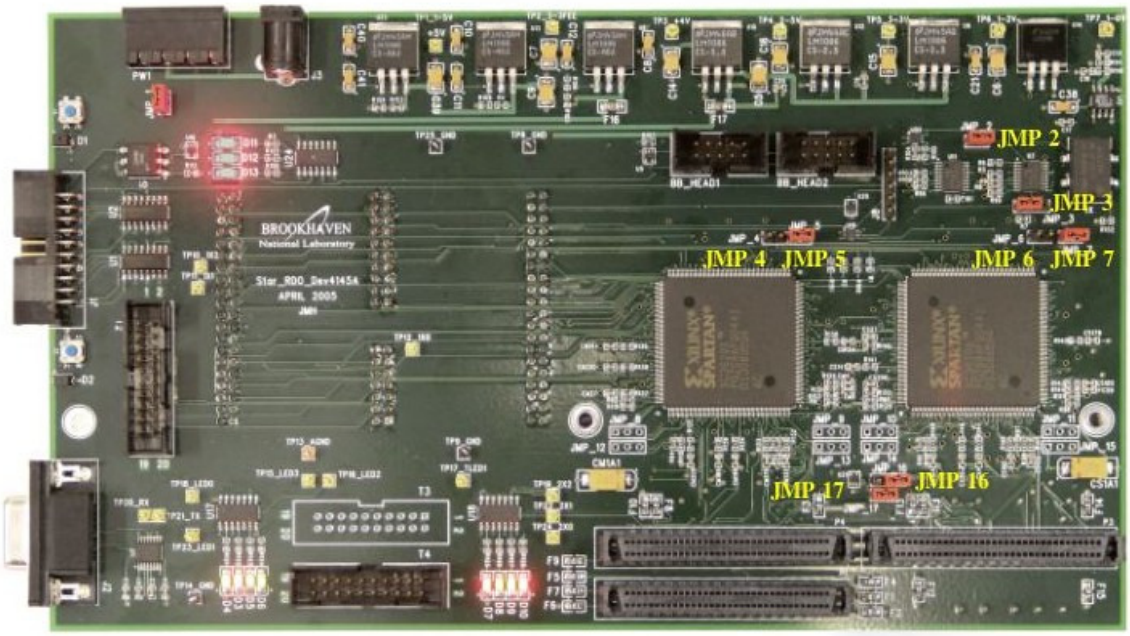
J3: Is a small connector that can be used to provide >5VDC for the logic circuitry alone.

Push buttons

S1: Push button forces onboard Xilinxes to boot.

S2: Push button forces off-board Xilinxes to boot.

Configuration options



Boot source

JMP 2: (**1-2**) PROM clock to the onboard FPGAs is supplied by on-board 1Mhz crystal, used when the 2 on-board FPGAs are in slave serial mode
Else no connection

JMP 3: (**2-3)** For the 2 on-board FPGAs, enable boot from PROM
(**1-2)** configure the FPGA remotely for testing, using the JTAG string from the Altera port, or locally, using the 6 or 10 pin connectors.

Mode jumpers

JMP 4, 5: For Xilinx 1 to be Master of the configuration process, connect pins 1-2 on both jumpers
For Xilinx 1 to configure by JTAG connect only JMP 5
For Xilinx 1 to be configured by local PROM, without being master, both JMP 4 and JMP 5 should be unpopulated.

JMP 6, 7: For Xilinx 2 to be Master of the configuration process, connect pins 1-2 on both jumpers
For Xilinx 2 to configure by JTAG connect only JMP 7
For Xilinx 2 to be configured by local PROM, without being master, both JMP 6 and JMP 7 should be unpopulated.

Only one of the Xilinxes on board should be configured as the serial master.

If either on-board Xilinx is a master, it will request data from the PROM on power up, providing its own clock, resulting in both on-board Xilinxes being configured. Otherwise, they will be configured as slaves to the PROM or by JTAG, depending on the setting of JMP 3 and mode jumpers JMP4 through JMP7.

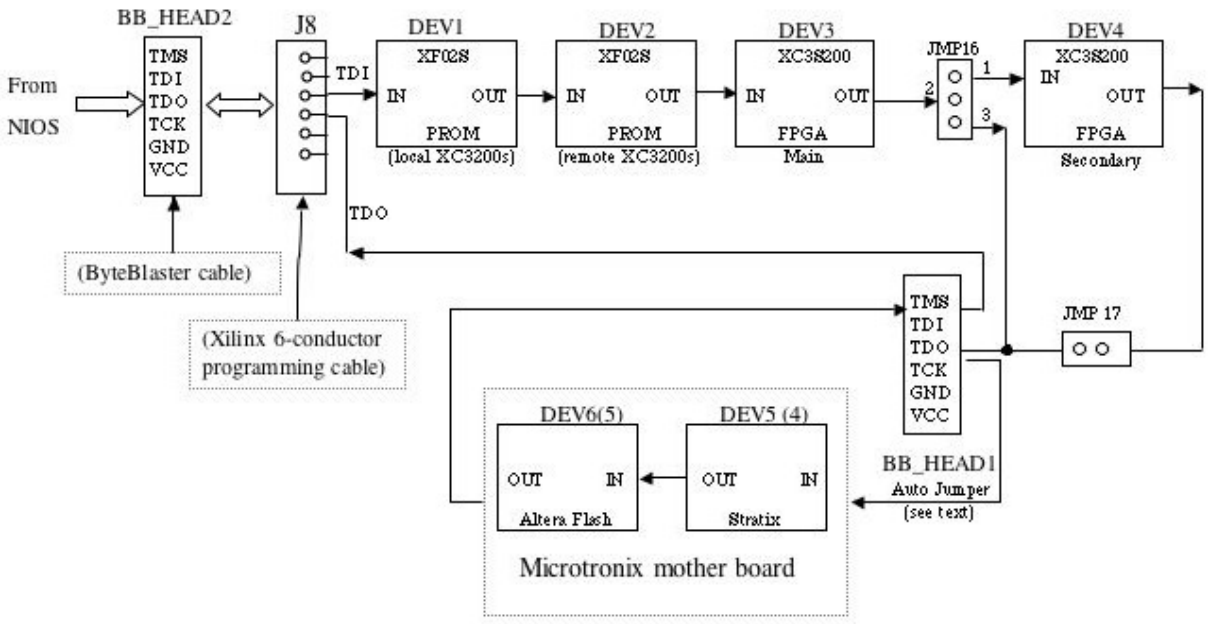
JTAG configuration

The JTAG chain allows a variety of methods for programming the devices on this board. Devices on the FEE boards, however, can only be programmed from the PROMs on this prototype RDO board.

There are 3 possible sources to the JTAG chain, as shown in the figure below:

- The 6-conductor Xilinx cable connected to J8
- The Byteblaster cable (10-conductor) connected to BB_HEAD2
- The NIOS CPU in the Altera Stratix

☛ **NOTE:** *The JTAG string is driven by both the ByteBlaster/Xilinx cable and the Altera output pins TDI, TCK, TMS (from the NIOS). If the cable is connected it is essential that the Altera pins be tri-stated. Only one of the (Xilinx, Byteblaster) cables may be connected at any one time.*



The header BB_HEAD1 allows the Altera parts on the Microtronix board to be included in the JTAG chain. This inclusion is handled automatically on the RDO prototype by sensing the presence of the 3.3V coming from the cable connected to the Microtronix board: the source of TDO is either the output of the JTAG devices on the Microtronix

board or that of the devices on the RDO prototype, depending on the presence of the 3.3V.

JMP 16: To include Xilinx 2 in the JTAG chain, JMP 17 and JMP 16 must have pins **1-2** connected.
Else connect JMP 16 pins **2-3**

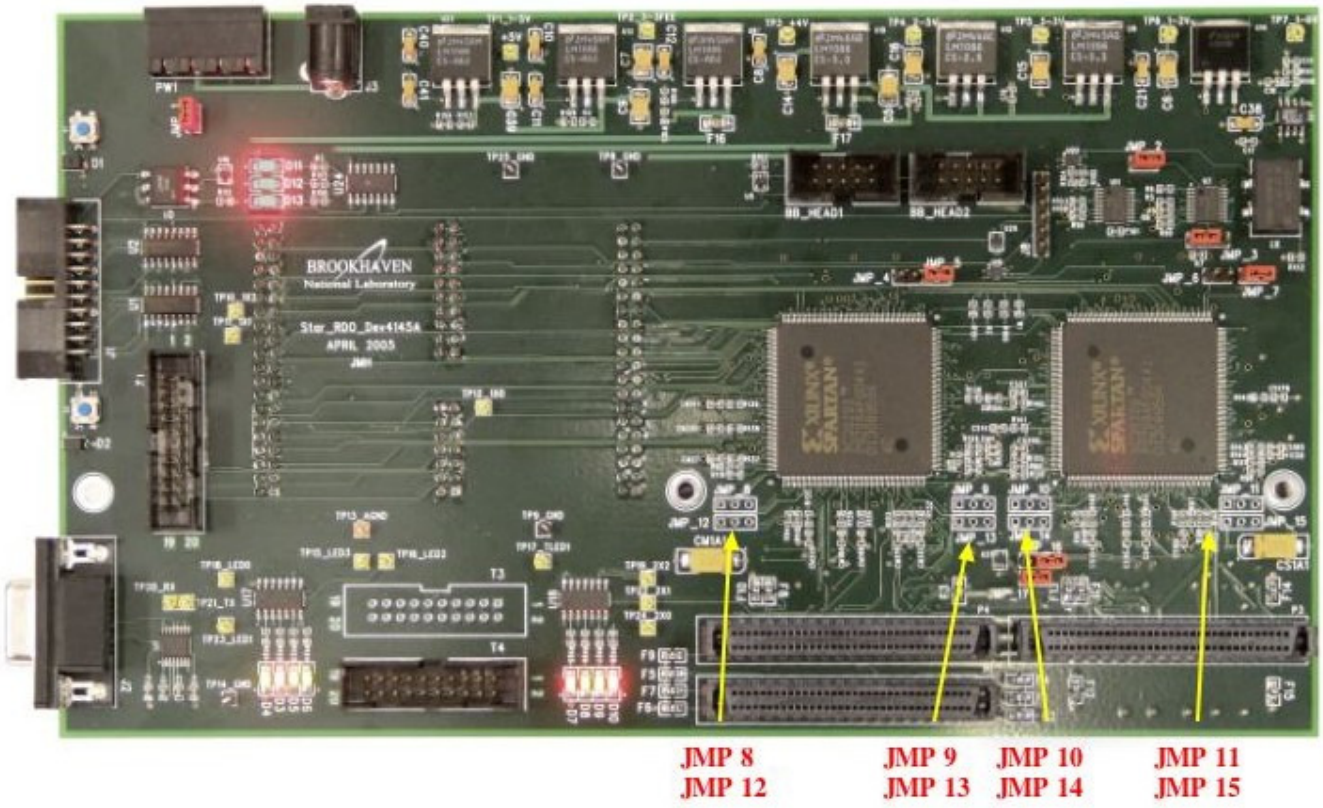
JMP 17: see above

Altera Byte Blaster cable header:
if a cable is connected to header BB_HEAD1 from the Altera board, and the host PC is connected to BB_HEAD2, then the Altera is automatically included in the chain. If no cable is present on BB_HEAD1 then the chain is closed without the Altera part.

GTL option

Select 3.3V or 1.5V I/O driver voltage for ports used to drive FEE cables. This allows testing of GTL+ and LVTTL drivers. For GTL+ mode, zero ohm resistors must also be installed to supply a VREF voltage for those ports, in LVTTL mode VREF pins could be used as additional I/O by using the resistor pad as a solder point for an additional signal.

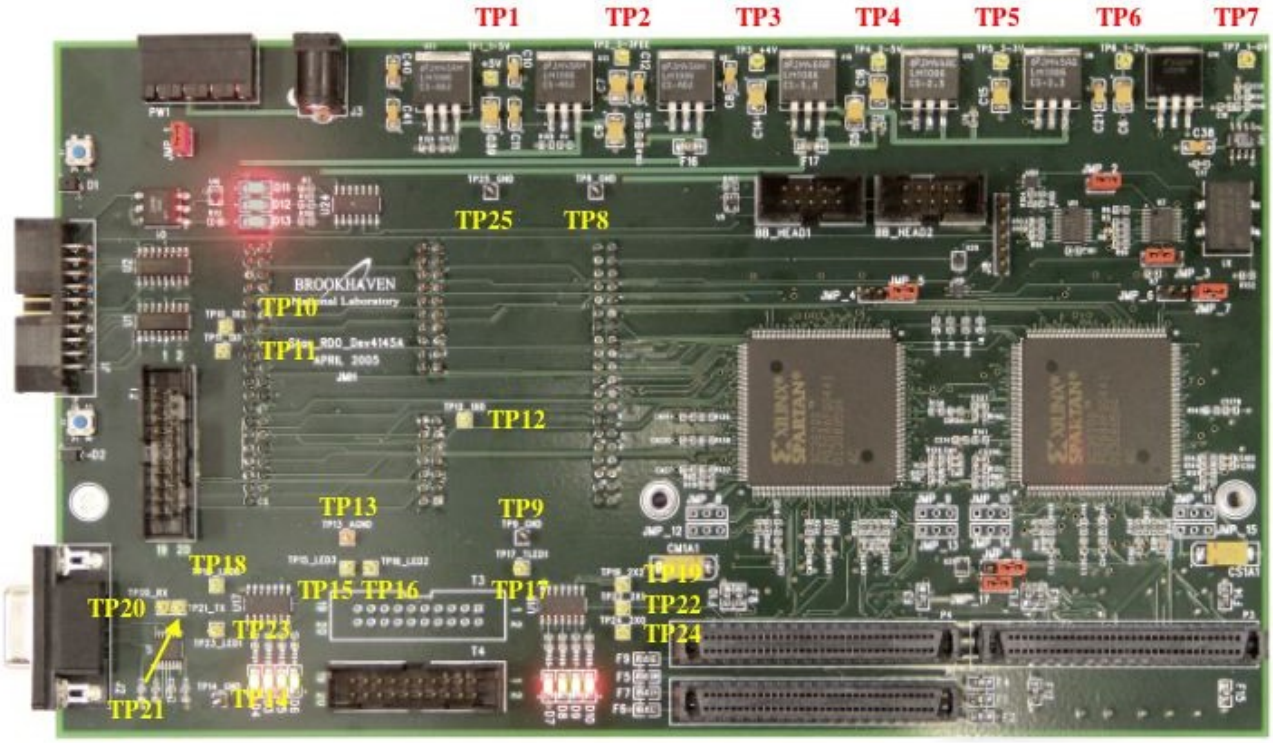
Jumper locations for GTL/TTL option



JMP 8 - 15:

GTL+ **(1-2)**
LVTTL **(2-3)**
Note: these are solder bridges

Test points


TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP25
TP8
TP10
TP11
TP12
TP13
TP9
TP18
TP15
TP16
TP17
TP19
TP20
TP22
TP23
TP24
TP21
TP14
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LEDs

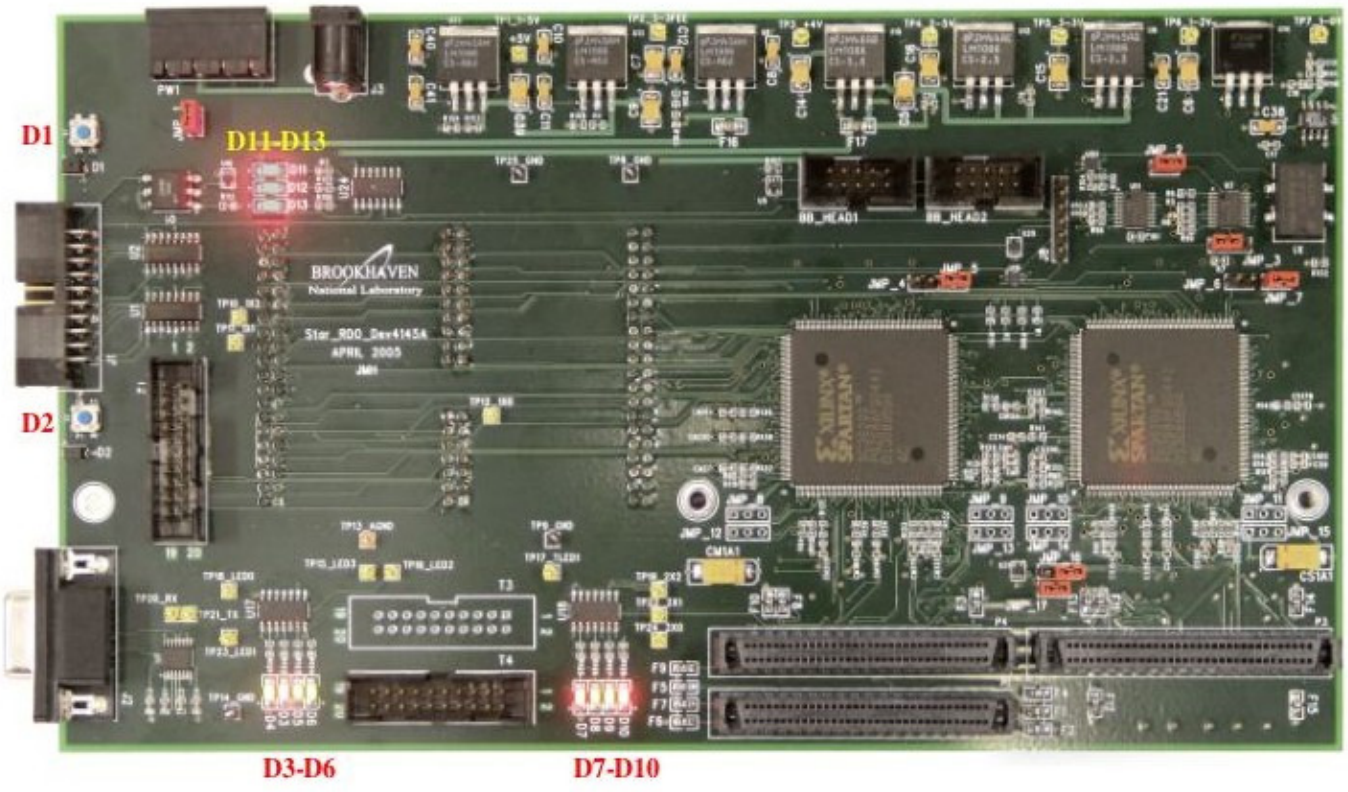
There are four groups of LEDs on the board:

- LED D1 is connected to the Xilinx 1 DONE signal
- LED D2 is connected to the FEE Xilinx DONE signal
- LED D7 is connected to test point TP17 and is not committed
- LEDs D3-D6 are connected to the Altera Stratix and **both** Xilinxes.
- LEDs D8-D10 are connected to the Altera Stratix and Xilinx 2.
- LEDs D11-D13are connected to the Altera Stratix and Xilinx 1.

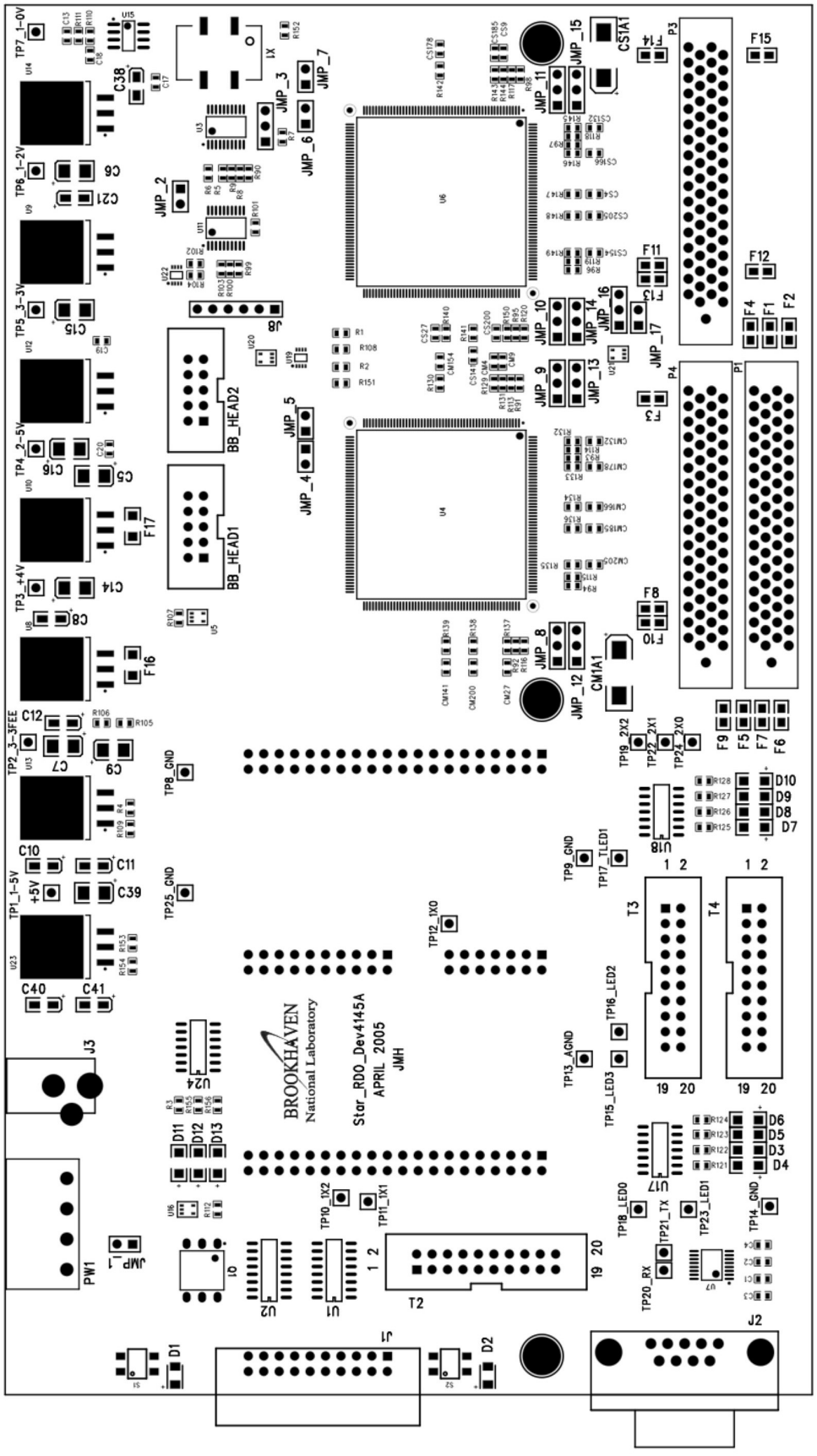
LED label	Function
D1	Done LED for local Xilinxes
D2	Done LED for remote (FEE) Xilinxes

LED label	Stratix pin	Xilinx	Test Point	Net name
D3	P1035	Both	TP23_LED1	RDO_LED1
D4	P1034	Both	TP18_LED0	RDO_LED0
D5	P1036	Both	TP16_LED2	RDO_LED2
D6	P1037	Both	TP15_LED3	RDO_LED3
D7	--		TP17_TLED1	Spare
D8	P1021	2	TP24_2X0	RD0_2X0
D9	P1022	2	TP22_2X1	RDO_2X1
D10	P1024	2	TP19_2X2	RDO_2X2
D11	P1038	1	TP12_1X0	RD0_1X0
D12	P1019	1	TP11_1X1	RDO_1X1
D13	P1020	1	TP10_1X2	RDO_1X2

LED locations



Appendix A: Board drawing



RDO prototype mounted on Microtronix development board