Specification for the
STAR "Cluster-Finder
ASIC

STAR Note 293

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Revision History

REVISION	DATE	COMMENTS
-	**June 2, 1995**	Initial Release
A	**June 9, 1995**	Spec Review Release.
B	**June 15, 1995**	Modifications from spec review. - Many wording changes in entire document - broke mode_cntl register into two - took out the address line control from MEM_ADD - modified interface section to group signals - added timing parameters to all interface diagrams - added testability requirements section
C	**June 20, 1995**	Modifications for status register change. - added bit to status register for END_ACQ - END_ACQ cleared by both CLEAR and CLUSTER_DUMP
D	**June 26, 1995**	Modifications for M. LeVine comments. - added bit to status and pulse register for memory test - Made processor interface signals work whether in test mode or not. - Changed memory initialization so that chip does not have to initialize memory all the way through. - Numerous other wording and clarifications due to ML's comments.
E	**July 3, 1995**	Modifications for M. LeVine comments. - Modified timing on Sequential port - Made Processor DATA bus tri-state when chip not selected - External Memory interface timing defined - Clarified possible MAX_TIMEBIN values - Other wording, meaning clarifications, and formatting. THIS IS THE BASELINE DOCUMENT. DESIGN WILL BEGIN AT THIS POINT. CHANGES TO THIS DOCUMENT WILL BE DONE UNDER CONFIGURATION CONTROL.
F	**August 16, 1995**	Modifications due to VHDL implementation as described in the change description. - Specified the active states on the status register - Expanded and clarified the description of the Pedestal Offset function - Added a processor-accessed register to control external memory wait states - Substantially expanded the description of the sequential

G	**July 29, 1996**	interface, cluster dump processing and cluster list format. - Added note to clarify timing values. - Added PED_OFFSET_CLK timing parameters - Changed Cluster RAM to 4Kx10 - Specified Output drive characteristics - Changed I/O from CMOS to TTL. - Changed DATA_ACK to open-collector active low. - Specified wait states to mean additional beyond two. - Clarified that only 31 cluster lists are stored in TPC mode.

1 Scope. This document describes the functional, interface, testability/diagnostic, and performance requirements for the STAR "Cluster-Finder ASIC. This is meant to be primarily a requirements document. Detailed structural definitions of the hardware are outside the scope of this document.

2 Applicable Documents.

STAR "cluster finder" ASIC Functional specification, ver. 4.3.1, 5/12/95.

3 Functional Requirements. The STAR "Cluster Finder" ASIC (hereafter referred to as STAR or ASIC) is part of the Star Detector Receiver Board Electronics. In general, the ASIC receives event data from an Analog to Digital Converter (ADC), subtracts an offset or "pedestal" from the data, performs a look-up translation and passes the result to a FIFO for eventual readout. Additionally, the STAR performs certain thresholding tests on the data as it passes through the ASIC. Based upon these tests, the ASIC compiles lists of events that meet the thresholding criteria. These lists provide a means of readily identifying significant events. The lists are passed to the processor via the FIFO upon command from the processor or from external logic.

A block diagram of the STAR Receiver Board Electronics is depicted in figure 1. Event data is passed to the receiver board from the readout board via a fiber optic link. At this point, the data has already been digitized by an ADC. The receiver board de-serializes the data, and passes it to a De-multiplexer. The de-multiplexer passes the data to one of 18 ASICs per receiver board, or 6 per mezzanine. The ASIC processes the data and places data into its output FIFO.

The ASIC receives control information from an Intel i960 processor. There is one processor per mezzanine.

3.1 Interfaces

3.1.1 ADC Interface.
The Cluster Finder ASIC receives 10 bit data from an Analog to Digital converter interface. The ADC interface can work in two modes: Normal mode and Test mode. In Normal mode the data passed to the Pedestal Subtraction algorithm comes from the ADC data bus. In Test Mode the data comes from a TEST_VALUE register, set by the processor. The chip is in test mode when the processor sets bit 1 in the COMMAND register.

In Normal Mode, the ADC data is sent from the De-multiplexer. The Demux bus is attached to 9 Cluster ASICs. The data to a single Cluster ASIC is valid and latched once every 150 ns (minimum- data may come more slowly.) Thus the data on the bus changes every 17 ns.

The ADC interface can also be used to load the Pedestal Offset register. The data is on the ADC data bus, and the data is clocked into the register by the PED_OFFSET_CLK signal.

The ADC interface timing diagram is shown in figure 2.

*** NOTE: all timing numbers in this specification assume a clock frequency of 66 MHZ. If that value changes, these numbers will change accordingly**.

Table 1 - ADC Interface Timing Parameters

Parameter	Value		Description
	Min	Max	
Tsadc	10 ns		Setup Time, ADC_DATA valid to DATA_STROBE rising
Thadc	2 ns		Hold Time, DATA_STROBE rising to ADC_DATA invalid.
Tshadc	20 ns		High Time, DATA_STROBE
Tsladc	20 ns		Low Time, DATA_STROBE
Tpwadc	150 ns		Period, DATA_STROBE
Tspadc	10 ns		Setup Time, ADC_DATA valid to PED_OFFSET_CLK rising
Tshadc	20 ns		Hold Time, PED_OFFSET_CLK rising to ADC_DATA invalid
Tphped	20 ns		High time, PED_OFFSET_CLK

3.1.2 Sequential Interface.

The Sequential Interface provides the primary means of data transfer from the ASIC output FIFO. The FIFO is 16 deep by 8 wide. The Sequential Interface is effectively a "Demand Mode" Direct

Memory Access (DMA) interface. Whenever there is data in the FIFO, the ASIC "demands" attention by asserting the V_REQ signal. The Sequential DMA Interface responds by asserting the V_ACK signal. Assertion of V_ACK causes the normally tri-stated V_DATA bus to be driven with the first data value in the output FIFO. The falling edge of V_ACK indicates the value on the V_DATA bus has been latched. The falling edge also causes the FIFO read pointer to decrement, indicating the data byte has been read. Once V_ACK is de-asserted, the V_DATA bus tri-states. A timing diagram for this interface is shown in figure 3, with timing data in Table 2.

Data may be placed in the FIFO in two ways. First data is accumulated in the FIFO via the data pipeline during the data acquisition operation. Second, after acquisition, cluster list data may be dumped into the FIFO by asserting the CLUSTER_DUMP signal after the acquisition phase is completed.

Table 2 - Sequential Interface Timing Parameters

Parameter	Value		Description
	Min	Max	
Tphack	11ns	17 ns	V_ACK high time (NOTE: Tphack + Tplack must be less than or equal to 22 ns)
Tplack	5ns	11 ns	V_ACK low time (NOTE: Tphack + Tplack must be less than or equal to 22 ns)
Tdvdata		5 ns	V_ACK to V_DATA valid
Tdidata		5ns	V_ACK low to V_DATA invalid
Tdra	0 ns		Delay time, V_REQ high to V_ACK high
Tdireq		20ns	Delay time, V_ACK falling to V_REQ invalid

3.1.3 Memory Interface.

The Memory Interface provides all accesses to the external look-up table known as the Pedestal/Translation RAM. The RAM must be accessed by two functional blocks: the Processor Interface and the Data Pipeline. The access via the Processor interface is accomplished via register read/write cycles (for a description of register read/write cycles see the next section.)

The Processor Interface initializes the address bus by writing to the MEM_ADD_HI, MEM_ADD_MID and MEM_ADD_LO registers. The MEM_ADD_HI register controls the upper bits (18:16) of the memory address counter, MEM_ADD_MID controls bits 15:8, and MEM_ADD_LO controls bits 7:0.

The three memory address registers serve as a pre-load to a 19-bit address counter. This counter increments each time a memory read or write cycle is performed via the processor interface. The Processor Interface reads or writes to the Memory Interface by reading from or writing to the MEM_VAL register. The MEM_VAL register provides the data port for Processor Read/Write access to the Pedestal/Translation RAM. When read, this register returns the data value in RAM location pointed to by the RAM address bus. When written, this value in this register is written to the RAM location pointed to by the RAM address bus. Each Read/Write access to this register causes the Pedestal Ram Address Counter to increment.

Memory accesses from the data pipeline take two forms: Pedestal accesses and Translation accesses. These accesses are read-only with respect to the RAM. Pipeline accesses are also affected by the current operating mode (TPC or SVT mode, set by COMMAND[0]).

During TPC mode acquisition, bits 17:16 are driven to logic low at all times. Bit 18 is driven by the data pipeline and determines whether upper memory (Translation RAM : bit 18 =1) or lower memory (Pedestal RAM: bit 18 = 0) is accessed.

During SVT mode acquisition, bits 18:16 are controlled by the data pipeline. The additional pads in SVT mode (256 versus 64) require additional translation memory and therefore, additional address space. In addition to providing additional address space, the Memory Interface provides decoding logic for individual chip enables (CE[3:0]). These chip enables are a decode of address lines 18:17. A truth table for the chip enables is shown below:

Table 3 - Chip Enable Decoding

add (18:17)	ce(0)	ce(1)	ce(2)	ce(3)

00	0	1	1	1
01	0	1	1	1
10	1	0	1	0
11	1	1	0	0

Table 3 defines the relationship between address lines 18:17 and the chip enable outputs. This relationship can be unerstood as follows: If COMMAND (0) is zero the ASIC is in TPC mode. Only a single 128K-Byte RAM is required to service both Pedestal and Translation operations. If COMMAND (0) is a one, then SVT mode is active. In SVT mode, pedestal subtraction requirements are identical to those of TPC mode. Therefore, when bit 18 is low in SVT mode, CE(0) is always active. If bit 18 is high, then Translation RAM is being accessed. In SVT mode, Translation requires multiple RAMs which can be in various configurations. Bit 17 is used to control the CE[3:1] when bit 18 is high as shown in Table 3.

During Pedestal accesses, address bit 18:16 are forced low. The PED_OFFSET register provides an offset for addressing the Pedestal RAM during normal operation. These eight bits are added to the 10 bits comprising the current timebin. This addition is Modulo MAX_TIMEBIN + 1 (i.e. any carry beyond that is truncated). The result of this addition forms the lower 10 bits of the Pedestal RAM address (Note: in TPC mode bits 15:10 are comprised of the current pad number, in SVT mode bits 15:8 are comprised of the current pad number.) The PED_OFFSET register is intended for use in SVT mode. During TPC mode the PED_OFFSET register is typically set to zero.

Translation accesses are similar to Pedestal accesses. Bit 18 is forced high. Bits 17:16 are set to logic low in TPC mode, and set by the data path in SVT mode. Bits 15:10 are comprised of the current pad number in TPC mode bits while in SVT mode 17:10 are comprised of the current pad number. The low order bits are the result of the pedestal subtraction performed in the previous pipeline stage.

The memory interface has a programmable number of wait states. The number of wait states is equal to the value in the WAIT_STATE register plus two. Thus if the WAIT_STATE register is loaded with zero, the cluster finder uses two wait states, and if it is loaded with a 0010

(2), the cluster finder uses four wait states. The WAIT_STATE register is loaded by the microprocessor. Each wait state delays the time the ASIC waits for data to become valid after the address, etc. is valid. A wait state is one clock cycle long.

During all memory accesses from the data pipeline, the MREAD signal is active. A timing diagram of the memory interface is shown in figure 4, with timing data in Table 4.

Table 4 - Memory Interface timing Parameters

Parameter	Value		Description
	Min	Max	
Tmc		25nS	Memory Cycle Time, read or write
Tmad		25nS	Read time, Address valid to Data valid
Tmed		25nS	Read Time, MREAD high to Data valid
Tmsa		0nS	Setup Time, Address valid to write strobe low
Tmsd		10nS	Setup Time, Data valid to write strobe low
Tmha		0nS	Hold Time, write strobe low to Address invalid
Tmhd		0nS	Hold Time, write strobe low to data invalid
Tmwpw		15nS	MREAD low time

3.1.4 Processor Interface.

The Cluster Finder ASIC interfaces to an Intel i960 Cx microprocessor with a 33-MHz bus. The microprocessor has access to registers that control the operation and relay the status of the ASIC. There is bus control logic between the i960 and the ASIC to provide a simplified interface. The interface is memory mapped, with register selected by the REG_SELECT signal.

The processor interface consists of the DATA and REG_SELECT busses, as well as the CHIP_SELECT, READ/WRITE, DATA_REQ and DAT_ACK busses. The REG_SELECT and DATA busses provide address and data information. CHIP_SELECT individually selects the ASIC. READ/WRITE indicates whether a given access is a read or write access. The DATA_REQ and DATA_ACK signals provide a means to insert wait states on certain register accesses. The STAR inserts wait states only for accesses to the MEM_VAL register. The number of wait states inserted depends on the value in the WAIT_STATE register. The total number of wait states for memory accesses is three plus the number in the WAIT_STATE register.

The processor interface to the static RAM is meant to be used only when the chip is not in Data Acquisition mode. If the processor interface is used when the chip is acquiring data, then writes to data have no effect, and read data will not be correct. The memory address counter will still be incremented with either a read or write from the processor during data acquisition. The processor interface to the STATUS, COMMAND, and PULSE shall work correctly at all times. Timing diagrams for the READ and WRITE cycles of the processor interface are given in Figure 5 with timing numbers in Table 5.

Table 5 - Processor Interface timing Parameters

Parameter	Value		Description
	Min	Max	
Tpcsdr	0 ns		Setup time, CHIP_SELECT to DATA_REQ
Tprwdr	0 ns		Setup time, R/W* to DATA_REQ
Tpavdr	0 ns		Setup time, Read or Write Address valid to DATA_REQ
Tpdrda	note 1		Delay time, DATA_REQ rising to DATA_ACK rising (read data valid)
Tpdrh	34 ns		Duration, DATA_REQ high
Tpdrl	34 ns		Duration, DATA_REQ low
Tpha	5 ns		Hold Time, DATA_REQ high to Address invalid
Tpdvdr	0 ns		Setup time, Write Data valid to DATA_REQ
Tphd	5 ns		Hold Time, DATA_REQ high to write data invalid

Note 1: time will vary according to the register being accessed.

3.1.4.1 Register Definition

There are fourteen registers in the processor interface.

3.1.4.1.1 Status Register -

3.1.4.1.1.1 Interface - The status register is a Read register. A read returns the current value of the register.

3.1.4.1.1.2 Bit Pattern - The status register bit pattern is given below:

bit 4	bit 3	bit 2	bit 1	bit 0
BIST_GO	END_ACQ	MPED_ENABLE	FIFO_NOT_EMPTY	OVERRUN

Bit 0 (OVERRUN) - The OVERRUN condition indicates that the ASIC attempted to write data to the FIFO while the FIFO was full. This condition is cleared to a logic low by RESET or CLEAR. A logic high indicates an overrun condition.

Bit 1 (FIFO_NOT_EMPTY) - The FIFO_NOT_EMPTY condition indicates that the FIFO contains data which has not yet been read. This condition is cleared to a logic low by RESET or by CLEAR. A logic high indicates that the FIFOl has data.

Bit 2 (MPED_ENABLE) - The MPED_ENABLE (Master PED_ENABLE) condition indicates that pedestal subtraction has been enabled via the PED_ENABLE input signal or by the PROC_PED_ENABLE bit of the COMMAND register. This condition is affected only by the state of the PED_ENABLE input signal or by the PROC_PED_ENABLE bit of the COMMAND register. A logic high indicates that the pedestal subtraction is enabled.

Bit 3 (END_ACQ) - The END_ACQ condition indicates that the END_ACQ signal has been asserted. Is cleared by either CLUSTER_DUMP or CLEAR. A logic high indicates that the end of acquisition has been reached.

Bit 4 (BIST_GO) - The BIST_GO condition indicates that the status of a Memory BIST operation. A low indicates BIST has passed, a high indicates a failure or that the test is still in progress. The condition is set by initiating Memory BIST (writing a logic 1 to PULSE(4)). It is cleared by either CLEAR or the successful completion of Memory BIST.

3.1.4.1.2 Command

3.1.4.1.2.1 Interface - The Command register is read and written from the processor interface. The register is initialized by RESET (see individual bit descriptions).

3.1.4.1.2.2 Bit Pattern - The Command register bit pattern is given below:

bit 2	bit 1	bit 0
PROC PED_ENABLE	TEST/ DAQ	TPC/ SVT

Bit 0 (TPC/SVT) - The MODE bit determines the operational mode for the ASIC. When MODE is set to 0 the STAR is operating in TPC mode. When mode is a 1 the ASIC operates in SVT mode. This bit is reset to a logic 0, meaning TPC mode.

Bit 1 (TEST/DAQ) - The TEST/DAQ bit causes the incoming ADC value to be replaced by TEST_VALUE. The TEST_DATA register comprises the 8 most significant bits of TEST_VALUE. The lower two bits of TEST_VALUE are always set to 0. The TEST bit allows the microprocessor a convenient means of verifying ASIC operation. This bit is reset to a logic low, meaning the chip is in TEST mode.

Bit 2 (PROC_PED_ENABLE)- The value in bit 2 is logically or■ed with the PED_ENABLE input signal to form an internal Master PED_ENABLE signal. The MASTER PED_ENABLE signal determines if Pedestal subtraction is enabled during data acquisition. This bit is reset to a logic high, meaning pedestal subtraction is enabled.

3.1.4.1.3 PULSE

3.1.4.1.3.1 Interface - The Pulse register is written from the processor interface. The register is initialized by RESET. Writing a logic 1 to the bits in this register caused a one-clock cycle pulse to occur on internal signals. These signals cause the results described below. The bits do not have to be reset between writes.

3.1.4.1.3.2 Bit Pattern - The Pulse register bit pattern is given below:

bit 4	bit 3	bit 2	bit 1	bit 0
MEM BIST	PROC DATA STROBE	PROC RESET	PROC CLEAR	PROC CLUSTER DUMP

Bit 0 (PROC CLUSTER DUMP)- The pulse created by writing a logical one to bit 0 is logically or■ed with the CLUSTER DUMP input signal to form an internal Master CLUSTER DUMP signal. The Master CLUSTER DUMP signal causes the chip to perform a cluster dump operation.

Bit 1 (PROC CLEAR)- The pulse created by writing a logical one to bit 1 is logically or■ed with the CLEAR input signal to form an internal Master CLEAR signal. The Master CLEAR signal causes the chip to perform a CLEAR operation (see section 3.2.5).

Bit 2 (PROC RESET) - The pulse created by writing a logical one to bit 2 is logically or■ed with the RESET input signal to form an internal Master

RESET signal. The Master RESET signal causes the chip to perform a RESET operation (see section 3.2.6).

Bit 3 (PROC DATA STROBE)-The pulse created by writing a logical one to bit 3 is logically or■ed with the DATA STROBE input signal to form an internal Master DATA STROBE signal. The rising edge of the Master DATA_STROBE causes the ADC_DATA bus, or TEST_VALUE, depending on the value of COMMAND(1), to be latched into the input register.

Bit 4 (MEM_BIST)-The pulse created by writing a logical one to bit 4 initiates a Memory BIST operation (see section 5.1).

3.1.4.1.4 Test_Data

3.1.4.1.4.1 Interface - The Test_Data register is read and written from the processor interface. The register is initialized by RESET to all logic lows.

3.1.4.1.4.2 Bit Pattern - The Test_Data register bit pattern is given below:

bit(7:0)
TEST_DATA

Bit (7:0) (TEST_DATA) - The TEST_DATA register comprises the 8 most significant bits of TEST_VALUE. The lower two bits of TEST_VALUE are always set to 0. The TEST_DATA register allows the microprocessor a convenient means of verifying ASIC operation.

3.1.4.1.5 N_Seq_Lo

3.1.4.1.5.1 Interface - The N_Seq_Lo register is read and written from the processor interface. The register is initialized by RESET to all logic lows.

3.1.4.1.5.2 Bit Pattern - The N_Seq_Lo register bit pattern is given below:

bit(3:0)
N_SEQ_LO

Bit (3:0) (N_SEQ_LO) - The N_SEQ_LO register indicates the number of consecutive timebins (1 to 16) where the pedestal-subtracted and translated value must exceed the value in the THRES_LO register to comprise the beginning of a cluster list. The value of N_SEQ_LO is one less than the required number of consecutive timebins. Thus a value of 000 in the N_SEQ_LO register indicates that only one timebin is required to satisfy the criteria of exceeding THRES_LO while a value of 1111 indicates that 16 consecutive timebins must meet this criteria.

3.1.4.1.6 N_Seq_HI

3.1.4.1.6.1 Interface - The N_Seq_Hi register is read and written from the processor interface. The register is initialized by RESET to all logic lows.

3.1.4.1.6.2 Bit Pattern - The N_Seq_Hi register bit pattern is given below:

bit(3:0)
N_SEQ_HI

Bit (3:0) (N_SEQ_HI) - The N_SEQ_Hi register indicates the number of consecutive or non consecutive timebins (1 to 16) where the pedestal-subtracted and translated value must exceed the value in the THRES_HI register to comprise a valid cluster list (Note that the N_SEQ_LO criteria described in the preceding section must also be met during this time). The value of N_SEQ_HI is one less than the required number of timebins. Thus a value of 000 in the N_SEQ_HI register indicates that only one timebin is required to satisfy the criteria of exceeding THRES_HI while a value of 1111 indicates that 16 timebins must meet this criteria.

3.1.4.1.7 Thres_Hi

3.1.4.1.7.1 Interface - The Thres_Hi register is read and written from the processor interface. The register is initialized by RESET to all logic lows.

3.1.4.1.7.2 Bit Pattern - The Thres_Hi register bit pattern is given below:

bit(7:0)
THRES_HI

Bit (7:0) (THRES_HI) - The high threshold value used to define a valid cluster.

3.1.4.1.8 Thres_Lo

3.1.4.1.8.1 Interface - The Thres_Lo register is read and written from the processor interface. The register is initialized by RESET to all logic lows.

3.1.4.1.8.2 Bit Pattern - The Thres_Lo register bit pattern is given below:

bit(7:0)
THRES_LO

Bit (7:0) (THRES_LO) - The low threshold value used to define a valid cluster.

3.1.4.1.9 Ped_Offset

3.1.4.1.9.1 Interface - The Ped_Offset register is read from the processor interface. The register is written either by strobing the value on the ADC_DATA bus with the PED_OFFSET_CLK signal (normal operation) or via the Processor Interface (Test Only). The register is cleared by RESET to all logic lows.

The Ped_Offset value effects only the address to the pedestal RAM. The pedestal offset is not included in the cluster list data or translated data position. Those data assume that the first data recieved is Timebin 0, Pad 0, and increments.

3.1.4.1.9.2 Bit Pattern - The Ped_Offset register bit pattern is given below:

bit(7:0)
PED_OFFSET

Bit (7:0) (PED_OFFSET) - The PED_OFFSET register provides an offset for addressing the Pedestal RAM during normal operation. These eight bits are added to the 10 bits comprising the current timebin. This addition is Modulo MAX_TIMEBIN (i.e. any carry beyond this is truncated). The result of this addition forms the lower 10 bits of the Pedestal RAM address in TPC mode or the lower 8 bits in SVT mode (Note: the upper bits (15:10 in TPC mode, 15:8 in SVT mode) are comprised of the current pad number, while bits 17:16 are logic lows, bit 18 is driven low). The PED_OFFSET register is intended for use in SVT mode. During TPC mode the PED_OFFSET register is typically set to zero.

3.1.4.1.10 Mem_Add_Hi

3.1.4.1.10.1 Interface - The Mem_Add_Hi register is read and written from the processor interface. The register is cleared by RESET to all logic lows.

3.1.4.1.10.2 Bit Pattern - The Mem_Add_Hi register bit pattern is given below:

bit(18:16)
MEM_ADD_HI

Bit (18:16) (MEM_ADD_HI) - The MEM_ADD_HI register provides the initial value of bits 18:16 to the Pedestal RAM Address Counter. The Pedestal Ram Address Counter is used to address the Pedestal/Translation RAM during Processor loading of the RAM. A write to the low byte (MEM_ADD_LO) causes this register to be uploaded to bits 18:16 of the Pedestal RAM Address Counter. A read operation returns the current value of the counter. The counter is incremented at the end of each Processor read/write cycle to the MEM_VAL register.

3.1.4.1.11 Mem_Add_Mid

3.1.4.1.11.1 Interface - The Mem_Add_Mid register is read and written from the processor interface. The register is cleared by RESET to all logic lows.

3.1.4.1.11.2 Bit Pattern - The Mem_Add_Mid register bit pattern is given below:

bit(15:8)

MEM_ADD_MID

Bit (15:8) (MEM_ADD_Mid) -The MEM_ADD_MID register provides the initial value of bits 15:8 to the Pedestal RAM Address Counter. The Pedestal Ram Address Counter is used to address the Pedestal/Translation RAM during Processor loading of the RAM. A write to the low byte (MEM_ADD_LO) causes this register to be uploaded to bits 15:8 of the Pedestal RAM Address Counter. A read operation returns the current value of the counter. The counter is incremented at the end of each Processor read/write cycle to the MEM_VAL register.

3.1.4.1.12 Mem_Add_Lo

3.1.4.1.12.1 Interface - The Mem_Add_Lo register is read and written from the processor interface. The register is cleared by RESET to all logic lows. When this byte is written to by the processor, the chip will load the Pedestal Address counters with the values in Mem_Add_Hi, Mem_Add_Mid, and Mem_Add_Lo.

3.1.4.1.12.2 Bit Pattern - The Mem_Add_Lo register bit pattern is given below:

bit(7:0)
MEM_ADD_LO

Bit (7:0) (Mem_ADD_LO) -The Mem_ADD_LO register provides the initial value of bits 7:0 to the Pedestal RAM Address Counter. The Pedestal Ram Address Counter is used to address the Pedestal/ Translation RAM during Processor loading of the RAM. A write to this register causes the register contents to be uploaded to bits 7:0 of the Pedestal RAM Address Counter. A write to this register also causes the contents of the Mem_Add_Hi and Mem_Add_Mid registers to be uploaded to bits 18:8 of the Pedestal RAM Address Counter. A read operation returns the current value of the counter. The counter is incremented at the end of each Processor read/write cycle to the MEM_VAL register.

3.1.4.1.13 Mem_Val

3.1.4.1.13.1 Interface - The Mem_Val register is read and written from the processor interface. The register is cleared by RESET to all logic lows.

3.1.4.1.13.2 Bit Pattern - The Mem_Val register bit pattern is given below:

bit(7:0)
MEM_VAL

Bit (7:0) (MEM_VAL) - The MEM_VAL register provides the data port for Processor Read/Write access to the Pedestal/Translation RAM. When read, this register returns the data value in RAM location pointed to by the RAM address bus. When written, this value in this register is written to the RAM location pointed to by the RAM address counter. Each Read/Write access to this register causes the Pedestal Ram Address Counter to increment.

3.1.4.1.14 Max_Timebin

3.1.4.1.14.1 Interface - The Max_Timebin register is read and written from the processor interface. The register is cleared by RESET.

3.1.4.1.14.2 Bit Pattern - The Max_Timebin register bit pattern is given below:

bit(7:0)
MAX_TIMEBIN

Bit (7:0) (MAX_TIMEBIN) - The MAX_TIMEBIN register provides the most significant 8 bits of the 10-bit maximum timebin value. The lower two bits are always one. The Maximum timebin is the value at which the timebin counter rolls over to zero. The values loaded into MAX_TIMEBIN will always be a value that conforms to (2**n)-1.

3.1.4.1.15 Wait_State

3.1.4.1.15.1 Interface - The Wait_State register is read and written from the processor interface. The register is set to 0000 binary by RESET.

3.1.4.1.15.2 Bit Pattern - The Wait_State register bit pattern is given below:

bit(3:0)
WAIT_STATE

Bit (3:0) (WAIT_STATE) - The WAIT_STATE register controls the number of additional wait states above 2 used by the External Memory interface. Thus a zero in the register means two wait states are generated.

3.1.4.2 Register Memory Map

Table 6 - Processor Interface Memory Map

MEMORY_SELECT(3:0)	REGISTER	ACCESS TYPE

	ACCESSED	
0000	STATUS	Read
0001	COMMAND	Read/Write
0010	PULSE	Write
0011	TEST_VALUE	Read/Write
0100	N_SEQ_LO	Read/Write
0101	N_SEQ_HI	Read/Write
0110	THRESH_LO	Read/Write
0111	THRESH_HI	Read/Write
1000	PED_OFFSET	Read/Write
1001	MEM_ADD_HI	Read/Write
1010	MEM_ADD_MID	Read/Write
1011	MEM_ADD_LO	Read/Write
1100	MEM_VAL	Read/Write
1101	MAX_TIMEBIN	Read/Write
1110	WAIT_STATE	Read/Write
1111	NOT USED (read returns all ones)	

3.2 Functional Description

3.2.1 Acquisition.

Acquisition is the process of latching data into the data pipeline. Each ADC sample comes once every 150nS. ADC samples are sequential(i.e., in TPC mode, pad samples 1 through 64 arrive sequentially for timebin 1, followed by pad samples 1 through 64 for timebin2, next come pads 1 through 64 for timebin 3, etc.,). In TPC mode there are 64 pads/timebin and up to 1024 time bins. In SVT mode, there are 256 pads/timebin and up to 256 timebins. The ASIC is responsible for keeping track of the current timebin and pad number. These values are latched with the data sample and accompany it through the pipeline.

3.2.2 Pedestal Subtraction.

As each data sample is acquired, the appropriate location in the PEDESTAL RAM look-up table is accessed. The PED_OFFSET register provides an offset for addressing the Pedestal RAM during the Pedestal Subtraction operation.

In TPC mode, the PED_OFFSET is added to the 10 bits comprising the current timebin. This addition is Modulo MAX_TIMEBIN (i.e. any carry beyond this is truncated). The result of this addition forms the lower 10 bits of the Pedestal RAM address (Note: bits 15:10 are comprised of the current pad number, while bits 18:16 are driven low).

In SVT mode, the PED_OFFSET is added to the 8 bits comprising the current timebin. This addition is Modulo MAX_TIMEBIN (i.e. any carry beyond this is truncated). The result of this addition forms the lower 8 bits of the Pedestal RAM address (Note: bits 15:8 are comprised of the current pad number, while bits 18:16 are driven low). The PED_OFFSET register is intended for use in SVT mode. During TPC mode the PED_OFFSET register is typically set to zero.

If the PED_ENABLE signal is active (set to one) or COMMAND(2)=1, the eight bit value obtained from the look-up operation is next subtracted from the ADC sample. The result of this subtraction is passed to the next pipeline stage (Note: if the result of the subtraction is negative, zero is passed to the next stage). If PED_ENABLE = 0 and COMMAND(2)=0, the ADC sample is passed to the next stage unaltered. The operation is summarized below:

```
                Address:  Mode = TPC :
                    1024*PAD_NO+(TIMEBIN+PED_OFFSET)MOD(MAX_TIMEBIN+1)
                      Mode = SVT:
                    256*PAD_NO+(TIMEBIN+PED_OFFSET)MOD(MAX_TIMEBIN+1)
                Action:    Read 8-bit pedestal value
                Result:     ADC  > pedestal value:   NXT_STG <= ADC - pedestal
value                     else:                          NXT_STG<= 0.
```

3.2.3 Translation and Storage.

Like Pedestal Subtraction, Translation involves a look-up operation to the external RAM. The address for the look-up operation is comprised of the result of the pedestal subtraction (bits 9:0) and the current pad number (bits 15:10 in TPC mode, bit 17:10 in SVT mode). In TPC mode, bits 17:16 are driven low and bit 18 is driven high. In SVT mode, bits 17:16 are drive by the extra two bits of pad number and bit 18 is driven high. The value retrieved from the translation table is written to the internal 16-deep by 8-bit FIFO. No attempt is made to regulate writes to the FIFO. It is the responsibility of the external logic to ensure the FIFO does not overflow. The operation is summarized below:

```
  Address:  Mode = TPC :
            1024*PAD_NO+(result of the pedestal subtraction)
          Mode = SVT:
            1024*PAD_NO+(result of the pedestal subtraction)
  Action:    Read 8-bit value from Translation RAM
  Result:    FIFO <= Translation value
```

3.2.4 Cluster Lists.

For a given pad number, the STAR ASIC looks for a series of sequential events (or clusters) that meet certain pre-programmed criteria. As these criteria are met, the ASIC compiles a list of the timebins corresponding to the start and stop point of the events.

In TPC mode, there are 64 such lists (one corresponding to each pad). Each consists of 31 pairs of 10 bit pointers. The pointers correspond to the beginning and ending timebin for each sequential event. If less than 31 events meet the pre-programmed criteria for a given pad, the remaining pointer pairs are set to all ones. If more than 31 events meet the pre-programmed criteria for a given pad, only the first 31 events are stored.

In SVT mode, there are 256 lists (one corresponding to each pad). Each consists of 8 pairs of 8 bit pointers. However, externally these pointers are treated as 10-bit values. This means that two bytes for each pointer must be written to the FIFO. In the case of valid pointers, the most significant byte is set to all zeros. In the case of invalid pointers, the most significant byte is set to all ones. The pointers correspond to the beginning and ending timebin for each sequential event. If less than 8 events meet the pre-programmed criteria for a given pad, the remaining pointer pairs are set to all ones. If more than 8 events meet the pre-programmed criteria for a given pad, only the first 8 events are stored.

Valid clusters must meet the following criteria. The N_SEQ_LO register indicates the number of consecutive timebins (1 to 16) whose pedestal-subtracted, translated value must exceed the value in the THRES_LO register to comprise a valid cluster. The value of N_SEQ_LO is one less than the required number of consecutive timebins. Thus a value of 000 in the N_SEQ_LO register indicates that only one timebin is required to satisfy the criteria of exceeding THRES_LO while a value of 1111 indicates that 16 consecutive timebins must meet this criteria. Additionally, the N_SEQ_HI register indicates the number of consecutive or non consecutive timebins (1 to 16) which must exceed the value in the THRES_HI register to comprise a valid cluster list (Note that the N_SEQ_LO criteria must also be met during this time). The value of N_SEQ_HI is one less than the required number of timebins. Thus a value of 000 in the N_SEQ_HI register indicates that only one timebin is required to satisfy the criteria of exceeding THRES_HI while a value of 1111 indicates that 16 timebins must meet this criteria. For example (see figure 6), assume that N_SEQ_LO is set to 10, and THRES_LO is set to 8. Further assume that N_SEQ_HI is set to 5 and THRES_HI is set to 16. Now assume that for a given pad, we get the series shown in figure 6. Timebin 2 exceeds the value THRESH_LO, and Timebin 3 exceeds the value THRESH_HI. But Timebin 4 is below THRESH_LO, therefore this is not a valid cluster. Now, Timebin 5 is again above THRESH_LO. 16 consecutive timebin values do not drop below THRESH_LO, therefore the N_SEQ_LO criteria is met. Now, in order for this list to be a valid cluster, at least 5 of these values (not necessarily consecutive) must be above THRESH_HI. There are 8 values which are above this threshold, therefore the data starting with timebin 5 and ending with timebin 20 is a valid cluster.

The pointers stored in the cluster list correspond to the first and last timebin whose values exceed THRES_LO. If a sequence begins and satisfies all criteria, but does not end before MAX_TIMEBIN, then the second pointer in the list is set to MAX_TIMEBIN. Similarly, a sequence may begin with timebin 0.

Cluster lists are stored in a 4Kx10-bit internal Cluster RAM. Bits 9:0 correspond to a pointer value. It should be noted that 11 bits are sent to the sequential interface. The eleventh bit is a valid signal generated by cluster processing. In SVT mode, timebins are only 8 bits wide but pointers are still treated as 10 bit values; therefore, bits

9:8 are forced low. When a valid pointer is written, bit 10 is forced to zero. The ASIC is responsible for ensuring that the valid cluster lists are contiguous in the low section of the pad RAM, followed by at least one invalid pointer. The external logic will know that the first invalid pointer received is the end of valid cluster lists for a given pad, and skip to the next pad. In TPC mode, address bits (11:6) correspond to the pad number of a given list and address bits (5:1) correspond to the pointer-pairs for each list, while address bit 0 differentiates between a beginning and ending pointer. In SVT mode, address bits (11:4) correspond to the pad number of a given list and address bits (3:1) correspond to the pointer-pairs for each list, while address bit 0 differentiates between a beginning and ending pointer.

When the end of an acquisition has been encountered, i.e. the last pad of the last timebin has been processed, the END_ACQ signal is asserted. The END_ACQ is cleared by CLUSTER_DUMP or CLEAR.

The Cluster RAM is accessed via the sequential interface. Upon receipt of the CLUSTER_DUMP signal or PULSE(0), the ASIC begins writing the contents of the Cluster RAM to the output FIFO. The Cluster RAM is read out from address 0 to address xFFF. Thus the 32 pointer-pairs for pad 1 are read out first, followed by the pointers for pad 2 and so on. Since pointers are 10-bit values, it requires two FIFO locations to store a single pointer. bits 7:0 are written first. Bits 9:8 are then written to bits 1:0 of the next available FIFO location. Bits 7:2 get the value of bit 10 of the pointer indicating that a pointer is valid (bits 7:2 are all zeros) or invalid (bits 7:2 are all ones). The ASIC puts the first byte into the FIFO. At that time the V_REQ signal is asserted, telling the external logic that there is data available. The ASIC then places the cluster pointer lists into the FIFO as they are read out. If the FIFO is full, the ASIC will wait until it is not full. At that point it will write in the next byte. This continues until the entire Cluster RAM contents have been read out. As soon as the FIFO is empty, the V_REQ signal is de-asserted. It is the responsibility of the external Processor to ensure that all acquisition processing is complete before issuing the DUMP_CLUSTER signal.

A sample data format assuming two valid clusters for Pad 0 is shown in Table 7. Note that the timebin data is independent of the Pedestal Offset. The values in the cluster lists cannot be guaranteed to reflect the format unless all data has been recieved for a given acquisition. If fewer data peices have been recieved, none of the data transmitted by the ASIC after a cluster dump will be valid.

Table 7 - Sequential Inteface Data Format

TPC mode		SVT mode	
Byte #	Contents	Byte #	Contents
0	Pad 0, Event 0 beginning timebin low byte	0	Pad 0, Event 0 beginning timebin low byte
1	Pad 0, Event 0 beginning timebin high byte	1	Pad 0, Event 0 beginning timebin high byte
2	Pad 0, Event 0 ending timebin low byte	2	Pad 0, Event 0 ending timebin low byte
3	Pad 0, Event 0 ending timebin high byte	3	Pad 0, Event 0 ending timebin high byte
4	Pad 0, Event 1 beginning timebin low byte	4	Pad 0, Event 1 beginning timebin low byte
5	Pad 0, Event 1 beginning timebin high byte	5	Pad 0, Event 1 beginning timebin high byte
6	Pad 0, Event 1 ending timebin low byte	6	Pad 0, Event 1 ending timebin low byte
7	Pad 0, Event 1 ending timebin high byte	7	Pad 0, Event 1 ending timebin high byte
8	Don’t Care (will be ignored)	8	Don’t Care (will be ignored)
9	Invalid (bits 7:2 are logic high)	9	Invalid (bits 7:2 are logic high)
10-127	Don’t Care	10-31	Don’t Care
128	Pad 1, Event 0 ending timebin low byte	32	Pad 1, Event 0 ending timebin low byte
129	Pad 1, Event 0 ending timebin high byte	33	Pad 1, Event 0 ending timebin high byte
etc.		etc.	

3.2.5 Clear.

The pulse created by writing a logical one to PULSE(1) is logically or’ed with the CLEAR input signal to form an internal Master CLEAR signal. The Master CLEAR signal indicates that a new acquisition process is ready to begin. Master CLEAR will always be asserted (by the external logic applying a logic 0 to the CLEAR signal or by writing a logical one to PULSE<1>) prior to an acquisition sequence. Assertion of the Master CLEAR initiates a CLEAR operation. During a CLEAR operation, the following initialization is performed:

Pedestal offset is pre-loaded into the timebin counter
Cluster logic is re-initialized
Cluster RAM write pointers are re-initialized
Data acquisition state machines and logic are re-initialized.
Overrun is reset
FIFO pointers are reset
END_ACQ is cleared

All processor interface registers are unaffected. The ASIC must be ready for data acquisition within 200 ns of beginning a CLEAR operation.

3.2.6 Reset.

The pulse created by writing a logical one to bit 2 is logically or'ed with the RESET input signal to form an internal Master RESET signal. The Master RESET signal causes the chip to perform a RESET operation The RESET operation causes all internal registers to be set to their initial states.

4 Interface Requirements. The STAR ASIC includes the following signal and supply pins. Each signal or related signal group includes a description, conditions under which it serves as primary input and/or output, current source and sink requirements, and conditions under which a transaction occurs on the signal.

4.1 ADC Interface signals

ADC_DATA(9:0)		Data input from the Front-End Receiver Electronics.
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	The rising edge of DATA_STROBE causes the ADC_DATA bus to be latched into the input register. Alternatively, the rising edge of PED_OFFSET_CLK causes the lower eight bits of the ADC_DATA to be latched into the PED_OFFSET register and TIMEBIN counter.

DATA_STROBE		Data Strobe indicates the arrival of the next ADC value
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	The rising edge of DATA_STROBE causes the ADC_DATA bus to be latched into the input register.

CLUSTER_DUMP		Initiates transfer of cluster pointer array.
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	

PED_OFFSET_CLK		Strobe to latch the PED_OFFSET register.
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	The rising edge of PED_OFFSET_CLK case the lower eight bits of the ADC_DATA bus to be latched into the PED_OFFSET register.
PED_ENABLE		Pedestal Subtraction Enable
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	Enables the pedestal subtraction function.
CLEAR		Clear.
	Input:	Always
	Active State:	Low
	Signal Type:	TTL
	Transaction:	CLEAR prepares the ASIC for the next ADC data stream by initializing all counters and resetting the FIFO pointers to an "EMPTY condition. The PED_OFFSET register is also cleared. All other programmable registers retain their state. The CLEAR must be asserted for a minimum of 34 ns.

4.2 External Memory Interface

ADDRESS(18:0)		Address to the pedestal/translation RAM.
	Output:	Always
	Active State:	High
	Signal Type:	8 ma TTL
	Transaction:	Address to external look-up RAM. Values come from the acquisition logic or the memory address counter.

MDATA(7:0)		Data Bus to the pedestal/translation RAM.
	Output:	MREAD = ✇0’
	Input:	MREAD = ✇1’
	Active State:	High
	Signal Type:	TTL/8 ma TTL output
	Transaction:	Data Bus to the pedestal/translation RAM.

MREAD		Read Strobe to the pedestal/translation RAM.
	Output:	Always
	Active State:	High
	Signal Type:	8 ma TTL
	Transaction:	Read Strobe to the pedestal/translation RAM.

CHIP_ENABLE(3:0)		External RAM enables
	Output:	Always
	Active State:	Low
	Signal Type:	8 ma TTL
	Transaction:	Used to enable multiple RAMs on the external interface. When one of the CHIP_ENABLEs is low, the RAM associated with it is the active one. Only one external memory chip is enabled at a time;

however, more than one chip enable may be active at once.

4.3 Processor Interface

CHIP_SELECT		Processor interface chip select.
	Input:	Always
	Active State:	Low
	Signal Type:	TTL
	Transaction:	When CHIP_SELECT is asserted, DATA_REQ is high and READ/WRITE is high the data from the register selected by REG_SELECT is driven onto the DATA bus. If read/write is low, the data on the DATA bus is valid on the rising edge of DATA_REQ.

DATA(7:0)		Data bus from the micro processor.
	Output:	READ/WRITE = ✇1’ AND CHIP_SELECT =✇0’ AND DATA_REQ = ✇1’
	Input:	CHIP_SELECT = ✇0’ AND ((READ/WRITE =✇0’) OR (READ/WRITE = ✇1’ AND DATA_REQ =✇0’))
	High Impedance:	CHIP_SELECT = ✇1’
	Active State:	High
	Signal Type:	TTL/8 ma TTL Output
	Transaction:	Data bus from the microprocessor.

REG_SELECT(3:0)		Address bus to internal registers.
	Input:	Always
	Active State	High
	Signal Type:	TTL
	Transaction:	Selects one of fourteen internal registers. See section 3.1.4.2 for a register map.

READ/WRITE		Read/Write Control.
	Input:	Always
	Active State:	High

	Signal Type:	
TTL		
	Transaction:	When CHIP_SELECT is asserted, DATA_REQ is high, and READ/WRITE is high the data from the register selected by REG_SELECT is driven onto the DATA bus. If read write is low, the data on the DATA bus is valid on the rising edge of DATA_REQ.
DATA_REQ		Data Bus Request Signal.
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	Initiates a Data Bus Transfer Cycle. The rising edge of DATA_REQ means the REG_SELECT is valid. On a write cycle, it also means DATA is valid.
DATA_ACK		Data Acknowledge
	Output:	Always
	Active State:	Low
	Signal Type:	Open Collector
	Transaction:	Acknowledges (terminates) a data bus transfer. For a read cycle, it means the DATA is valid. For a write cycle, it means the DATA has been clocked into the register corresponding to REG_SELECT.
END_ACQ		End of Acquisition
	Output:	Always
	Active State:	High
	Signal Type:	8 ma TTL
	Transaction:	Asserted when the end of an acquisition has been encountered, i.e. the last pad of the last timebin has been processed. Cleared by CLUSTER_DUMP or CLEAR.

4.4 Sequential Interface

V_ACK Video Ram Acknowledge

Input: Always

Active State: High

Signal Type: TTL

Transaction: Acknowledges (terminates) a sequential port data transfer. When V_ACK goes Active, the data pointed to by the FIFO read pointer is driven onto the V_DATA Bus. When V_ACK goes inactive, the V_DATA bus is tri-stated and the FIFO read pointer is incremented.

V_DATA(7:0) Video Ram Data bus.

Output: When V_ACK is active.

Inactive State: Tri-Stated

Signal Type: 8 ma TTL

Transaction: When V_ACK goes Active, the data pointed to by the FIFO read pointer is driven onto the V_DATA Bus. When V_ACK goes inactive, the V_DATA bus is tri-stated and the FIFO read pointer is incremented.

V_REQ Video Ram Data Request.

Output: Always

Active State: High

Signal Type: 8 ma TTL

Transaction: Signals data available from the sequential port.

4.5 Miscellaneous Signals

Hi-Impedance		Active-high hi-impedance control
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	When asserted, STAR turns all primary outputs to the hi-impedance state, or to default value when no hi-impedance state is available. All bi-directional signals are turned to input mode.
RESET		RESET
	Input:	Always
	Active State:	Low
	Signal Type:	TTL
	Transaction:	RESET causes all ASIC registers to be reset to their initial state. RESET must be asserted for a minimum of 34 ns.
CLOCK		System Clock (Max. Freq : 66 MHZ)
	Input:	Always
	Active State:	High
	Signal Type:	TTL
	Transaction:	Primary clock input for all logic. Duty cycle is 50% +/- 17%.
VDD		11 +5.0 volt supply pins.
VSS		12 ground supply pins.

5 Testability Requirements

Because of the cost sensitive nature of the STAR full scan and JTAG will not be used. However, the structure of STAR's circuitry will accommodate vectors that achieve a high fault coverage. Other circuitry will be designed with controllability and observability in mind. Test vectors will be written so that fault coverage will be a minimum of 85%. The microprocessor has access to most of the functionality within the chip, allowing a high level of controllability and observability.

5.1 Memory test

Cluster Memory will be the only area which will have a Built-In-Self test module associated with it. This will perform the following functions:

1. Walking ones.
2. Walking zeros.
3. Address line Test.
4. Data line Test.

In each case the results are read back into the BIST controller, compared to the known good pattern, and translated to a go/no-go flag. The memory BIST is initiated by the RESET signal.

Memory BIST is initiated by writing a logical 1 to PULSE(4) via the Processor Interface. Test results are available in bit 4 of the status register (BIST_GO).

6 Performance Requirements.

STAR is required to meet the following performance specification:

Power Supply :	5V+/-5%	VDD
CLK frequency:	66	MHz
Temperature:	0 to +70	degrees C