The STAR DAQ
Mezzanine Board User Manual and Reference

Version 1.0

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General Information

Introduction

The STAR DAQ Mezzanine Board (MZ) is a custom built printed circuit board which functions as a *Daughter* Mezzanine board for the STAR DAQ Receiver Board. Three Mezzanines fit on one Receiver Board.

The Mezzanine Board is used for the readout of the two main STAR detectors: **TPC** and **SVT**. Each of these detectors uses a number of these boards (144 X 3 and 24 X 3 respectively) on the receiving end of the fiber-optic data chain which transfers the digital detector data from the detectors on the experimental platform to the STAR DAQ in the DAQ room. The Mezzanine Boards receive the detector data through the Receiver Board and perform intelligent processing of the data for further Level 3 Triggers and later data storage and online review.

Board Overview

Each Mezzanine is an intelligent data and I/O processor with an Intel I960HD microprocessor equipped with SDRAM memory, 6 STAR DAQ ASICs which facilitate data processing, VRAM memory for event buffering and a local⇔PCI bridge. The later bridge chip enables the Mezzanine to function as a PCI bus device.

The Mezzanine is both a PCI master and a slave. As a master it responds to commands from the central VME Crate Controller (through the Receiver Board's VME⇔ PCI interface) and ships processed data out to VME while as a slave it receives commands from the Crate Controller and other Mezzanines in the Receiver Board.

The Mezzanine's PCB can accustom two different SRAM flavors depending on the Mezzanine mode. The larger, 512 kB, SRAM is used in the SVT versions of the Mezzanine while the smaller, 128 kB, is used in the TPC version. The PCB itself is the same since the two device footprints exist in parallel and it only depends on the stuffing of the PCB which version will be used.

Features

- 1 custom connector for interfacing with Receiver Board's Local data bus
- PCI device with 2 custom connectors which connect to the Receiver Board
- Intel I960HD Microprocessor
- 4 MB of Video RAM (VRAM) for event storage (8 X IBM025161LG5D-60)
- 4 MB local SDRAM memory as working memory for the CPU (2 X Toshiba TC59S1616AFT)
- PLX PCI 9080 Bus Master Interface Chip for the PCI interface to the CPU bus
- 6 STAR DAQ ASIC's for cluster finding and early data processing
- 6 associated SRAMs for pedestal and gain table storage for the ASICs
- 3 Lattice programmable ISP CPLDs
  - 1 Memory Controller
  - 1 Sequential VRAM port Controller
  - 1 Register Controller and Local Bus Arbiter
- 1 test pod connector for debugging operations

Functional Description

The Mezzanine performs three main functions:

1. provides buffer storage for up to 12 events
2. calculates the 2-dimensional cluster positions as the first step in further Level 3 Trigger processing
3. formats the detector data for later storage and online review

As each event gets passed to the Mezzanine the following operations are typically performed:

1. pedestal subtraction (ASIC with SRAM)
2. gain correction with 10-to-8 bit compression (ASIC with SRAM)
3. peak finding in the 1-dimensional “time” direction (ASIC)
4. data reordering so that the CPU “sees” the data organized in compact pads/anodes (Fast switch and ASIC-VRAM Controller)
5. buffering in VRAM (VRAM and ASIC-VRAM Controller)
6. 2-dimensional cluster finding (CPU)
7. formatting and zero-suppression (CPU)
8. shipping the data and/or clusters to a VME host (PLX DMA)

The Mezzanine additionally performs:

1. Pedestal Calculation
2. Gain Calibration

when necessary.

Architectural Overview

The general architecture of the board may be subdivided between three different sections: the ASIC section, the CPU section and the PCI bus section.

The ASIC section contains:

- 6 ASICs and associated 6 SRAMs
- 2 fast data switches (QSwitch) and the ASIC-VRAM Controller
- ASIC Register Interface
- sequential ports of the 8 VRAM devices

The CPU section contains:

- Intel I960HD CPU with the CPU bus
- SDRAM and VRAM memories
- control registers
- local bus arbitration
- interrupt routing to the CPU and the PLX

The PCI bus section deals mostly with the PLX PCI9080 PCI bus bridge.

ASIC Bus

ASICs and SRAMs

The STAR DAQ ASIC is a custom developed ASIC which facilitates detector data processing. Each ASIC accepts a 10 bit data stream asynchronously strobed by a separate data strobe from the Receiver Board.
The ASIC performs:

1. pedestal subtraction
2. gain correction and 10-to-8 bit compression
3. peak finding in the one-dimensional “timebin” direction.

The pedestals are calculated for every data strobe while the gain corrections are applied equally to every timebin of a given pad/anode. The pedestals and the gain tables are stored in associated SRAM where the CPU can perform writes/reads through an ASIC register interface to store the calculated values.

The SVT versions of the Mezzanine have one single 512 kB SRAM chip while the TPC versions have one 128 kB SRAM chip associated with each ASIC. The Mezzanine PCB provides 2 different footprints for the two SRAM flavors so a decision as to which Mezzanine flavor will be produced must be made before board stuffing.

The ASIC operates in two modes for each event. First the event is readout in the “ADC” mode which provides the 8bit ADC data after pedestal subtraction and gain correction. After the whole input ADC stream is processed the ASIC enters the “CPP” mode (under CPLD control) which is used for the readout of the Cluster Pointer Pairs (CPP) from the internal ASIC’s memory. Once this readout completes an interrupt (ASIC_DONE) is issued to the CPU which is used to start the 2-dimensional cluster finding.

Each ASIC has a set of 16 8bit registers for status/control which can be read/written by any master on the local bus. For details consult the DAQ ASIC documentation.

Data Switch and VRAM

The data arrives at each ASIC in pad/anode order i.e. the data for all pads in timebin 0 is sent first followed by all the pads in timebin 1 etc. until the last timebin. The 2-dimensional cluster finding as well as later data processing prefers to see the data in timebin order i.e. in increasing CPU addresses the data corresponds to timebins 0,1,2,… for pad N after which follows the same timebin sequence for pad M.
To provide this feature the data is scrambled at the output of the ASIC through a set of dedicated switches (QSwitch) before it is strobed to the sequential port of the VRAM. All this is handled by code running in an CPLD and is transparent to the CPU.

Under control of the ASIC-VRAM controller the scrambled data is sent in order to the associated VRAM through the 16 bit sequential port of the VRAM device.

The whole ASIC bus is subdivided in two banks each consisting of three ASICs associated with 4 VRAM chips and one QSwitch device. The data sequence is controlled in parallel for both banks through one ASIC-VRAM CPLD running at 66 MHz.

Intel I960 Bus

General

The local bus is a general Intel I960 “CA” standard bus with separate 32 bits wide address and data buses running at 33 MHz.

The local bus is shared among the two bus masters: the CPU and the PLX bridge with each supporting burst accesses, READY# and BTERM# protocols.

Intel I960HD CPU

The CPU runs at 33 MHz bus speed and 66 MHz core speed. It's has a pipelined, superscalar architecture with 4 kB of data cache and 4 kB of instruction cache. The CPU supports many context switch latency enhancing features as well as 2 kB of super-fast on-chip RAM for use by commonly used variables and general data storage.

The CPUs core runs on 3.3 V although the CPU is 5 V compliant. Refer to the CPU's data sheets and manuals for additional information.

SDRAM

The board supports 4 MB of SDRAM memory used as the working memory of the CPU. The SDRAM supports bursts up to 1 kB long and will terminate a burst on every 1 kB boundary. The wait state pattern is 1-0-0-0 for writes and 2-0-0-0 for reads while running at 33 MHz.

The SDRAM is a 3.3 V device so it had to be interfaced to the main data/address bus with 5⇔3.3 V limiters/drivers.

VRAM

The board supports 4 MB of EDO VRAM used as the buffer memory for detector events. This size accommodates storage for 12 full events which makes the software fully pipelined up to that depth.

The VRAM features a 16 bit wide sequential RW port which is filled with the event data by the ASIC-VRAM controller during the event acquisition phase. The writing of the data to the sequential port is completely transparent to the CPU and to other users and is handled by the ASIC-VRAM and the VRAM controller.

The address lines are scrambled when presented to the VRAM chips in such a way to make the data look like it was packed in compact pad/anode order.

The VRAM accepts bursts of four beats long which will be terminated on each 16-byte boundary due to the way the data is presented to the CPU. The wait state pattern for the VRAM is 2-1-1-1 for writes and 3-1-1-1 for reads while running at 33 MHz.

Control and ASIC Registers

The Register Controller CPLD includes the following registers:

1. ASIC Interrupt Status
2. VRAM WPBM cycle generator
3. Serial Clear Register
4. ASIC Buffer Register

The same CPLD also facilitates the handshakes for the communication with the ASIC registers with each of the 6 ASICs supporting 15 registers.

All the registers are at most 8 bits wide.
See the "Registers" section for further details.

Local Bus Arbitration

The local bus has two bus masters: the CPU and the PLX bridge chip which necessitates local bus arbitration. A round-robin scheme was implemented in a CPLD with additional deadlock protection with the bus backoff functions in both the CPU and the PLX. Refer to the CPU and PLX documentation for further details.

Interrupt Routing

The only Interrupt Handler on the Mezzanine is the CPU which handles all interrupt sources.

Source	CPU IRQ#
PLX Doorbell/Mbox	0
PLX Error	1
FE Event End	2
FE Fault	3
FE Watchdog Timer	4
FE Abort	5
ASIC Done	6
unconnected/unused	7

CPU Interrupt Map

PCI Bus

The interface to the PCI bus is the PLX bridge chip. The PLX is PCI 2.1 compliant and runs with the same frequency as the PCI CLOCK. The current board design only supports the 33 MHz PCI bus/local clock.

The board connects to the PCI bus over two non-standard connectors which additionally provide the 3.3 V power necessary for the CPU and the SDRAM.

PLX PCI9080

The PLX is a high performance PCI⇔I960 bus bridge chip which contains additional features:

- 2 DMA channels
- 32 input doorbell bits/32 output doorbell bits with interrupt capabilities both on the local and on the PCI side if the bridge
- 8 32bit mailbox registers out of which 4 of them have direct interrupt capabilities to the local side of the bus

The device offers three PCI slave and one local bus slave window. The window sizes and attributes are fully programmable by the user.

The PLX offers a DMA engine for fast data moves between the local and the PCI bus. The engine supports chaining (scatter/gather) and has interrupt capabilities to the local CPU side.

The doorbell bits and the mailboxes facilitate the interprocessor communication throughout the Receiver Board as well as the communication with the Crate Controller.

VxWorks Real-Time Operating System

The I960 CPU runs the VxWorks 5.3 Real-Time Operating System. The Board Support Package was custom developed for the Mezzanine taking into account that the Mezzanine has no usual I/O i.e. no serial port, no network etc.

The Crate Controller must copy the kernel bootable image (‘bootlet’) in the appropriate place in CPU’s memory after which it takes the CPU out of reset. Once the CPU boots and runs the bootlet code it downloads its kernel image from Crate Controller’s memory and starts initializing the full-blown vxWorks kernel and user software.

A pseudo-console device was implemented using the doorbell interrupt functionality of the PLX which enables the user to connect via a network to the Crate Controller after which the user’s console gets routed to the particular Mezzanine’s pseudo-console.

Initialization and Configuration

Upon power-up or PCI RST# the Mezzanine enters the default state:

- the CPU is left in the RESET state
- local arbiter disables the CPU
- all the CPLDs are reset
- all the ASICs are reset
- the PLX’s registers are reset to the power-on state

After a successful VME Auto-Id cycle from the Receiver Board the Crate Controller performs these steps for each Mezzanine in the Receiver Board:

1. initializes the PLX bridge chip, opens all the necessary slave and master windows with their associated attributes
2. loads a small piece of boot code (called a ‘bootlet’) to a particular location in the CPU SDRAM
3. loads the correct IMI to the correct place in the CPU SDRAM (refer to I960HD documentation for more details)
4. takes the CPU out of RESET by resetting a bit in the PLX’s control register which in turn drive the CPU RESET# line high
5. waits for the CPU to respond with a series of writes to predetermined mailbox locations to confirm the CPU’s health and code correctness

The bootlet code in the CPU loads the vxWorks kernel binary image from a location in Crate Controller’s memory (visible on VME) and jumps to the first vxWorks instruction after which the vxWorks kernel takes control, reinitializes in the usual vxWorks manner and starts running the user code. Refer to vxWorks documentation for further details.

The programming of the slave images and attributes as well as the various configuration registers of the PLX9080 is up to the user. However, due to the very complex nature of bridge chips as well as some limits in the various slave window sizes, offsets and relative offsets a canonical map is given below.

The map pertains to the case of Mezzanine 1 but any other boards should be configured similarly with the same offsets but with different PCI base addresses. Refer to the document “The STAR DAQ Crate Controller Memory Map” for a full description of the memory map of the whole crate.

PCI Slave Map

	PCI	local	cycle	
PLX Cfg. Slave	1800	-	cfg	
Memory	1080.0000	E000.0000	mem	
VRAM	1080.0000	E000.0000	mem	
SDRAM	10C0.0000	E040.0000	mem	
Local Registers	1201.0000	C000.0000	mem	
PLX Registers	1205.0000	A000.0000	mem	1

1) This image doesn't actually initiate transactions on the local bus since the PLX's registers take priority.

PCI Master Map

The Mezzanine has only one PCI master image which may be opened from 0x0000.0000 to 0xA000.0000.

Appendix A - Registers

The registers are located at base address 0xC000.0000.

The address range from offset 0x0000 to offset 0x0180 is occupied by the 16 ASIC registers for all six ASICs. Each register occupies an address range of 4 bytes although it's only 8 bits wide. Each register looks like the following:

ASIC_n_REG_m	**Offset: xx**
Bits	**Function**
31-24	Ignored
23-16	Ignored
15-08	Ignored
07-00	VALUE

Name	Type	Function
VALUE	RW	whatever

The offsets of the 6 ASICs are given in the following table:

ASIC number	Offset
0	000
1	040
2	080
3	0c0
4	100
5	140

For the function of each register refer to the ASIC documentation.

ASIC_BUFFER	Offset: 200

Bits	Function	
31-24	Ignored	
23-16	Ignored	
15-08	Ignored	
07-00	Ignored	ASIC_BUFFER

Name	Type	Function
ASIC_BUFFER	RW	The number of the VRAM buffer where the next event will be stored

ASIC_INT	Offset: 204

Bits	Function	
31-24	Ignored	
23-16	Ignored	
15-08	Ignored	
07-00	Ignored	ASIC_INT

Name	Type	Function
ASIC_INT	R/Write to reset	1=ASIC Done 0=ASIC Idle

VRAM_WPBM	Offset: 400

Bits	Function
31-24	MASK
23-16	MASK
15-08	MASK
07-00	MASK

Name	Type	Function
MASK	WO	Must write 0xFFFF.FFFF for correct VRAM initialization!

A write to this register with a value of 0xFFFF.FFFF *must* occur before an attempt to use the VRAM. See the VRAM data sheet for further information. A read value is undefined.

SER_CLEAR	Offset: 404

Bits	Function	
31-24	Ignored	
23-16	Ignored	
15-08	Ignored	
07-00	Ignored	SER_CLR

Name	Type	Function
SER_CLR	WO	any=clear sequential logic and ASICs

Any write to this location clears the sequential logic of the VRAM controller as well as resets the ASICs and makes them ready for the next event. A read value is undefined.

Appendix B - Mechanical and Electrical Characteristics

The Mezzanine is a 4 inches high by 14 inches deep PCB. It's an eight layer double sided printed circuit board comprised of four signal layers with two separate power and two separate ground planes.

It uses 3 non-standard connectors which provide I/O signals to/from the Receiver Board as well as +5V and +3.3V power.

Appendix C - Signals and I/O

Refer to the document "STAR DAQ Receiver Board User Manual and Reference" for signal specifications and pinouts since they are common to both boards.

Additional Appendices

The following is a set of additional pages inserted later i.e. schematics, exact pinouts of various connectors etc. in no particular order.