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1: Module   CHERST2
2: Title    'Status Gate and Error latches for CHERII frontend logic'
3: "
4: "-----"
5: " This CPLD is used by CHERII and contains the following logic  "
6: " 1)The Status gate for up to three 8bit words                    "
7: " 2)A latch for any type of Link error [LNKELED#]                "
8: " 3)A latch for the Watch dog timer [WDTELED#]                  "
9: " 4)A latch if any fault occurs [FAULT]                          "
10: " PATH:stardaq/home2/bob/powerview/cher2 cherst2.abl            "
11: " Added latch for end of event time out signal to mezz board    "
12: "   (1/29/98)                                                    "
13: "-----"
14: "
15: " Inputs
16:
17: FE_CLR    PIN;"Pulse to reset after a normal event"
18: ST00      PIN;"State bits for status readback"
19: ST01      PIN;
20: ABORTP    PIN;"Signal used to flush current unwanted event"
21: FE_OE0    PIN;"Select one of three status registers"
22: FE_OE1    PIN;" from front end logic"
23: !LINKRDY  PIN;"GLINK status"
24: HPERR     PIN;"Error signal from HP Glink part"
25: !HBAD     PIN;"Latched bad Header length"
26: !BSYERR   PIN;"Latched busy error(Event start while still Busy)"
27: !SFTBSYA  PIN;"Soft busy from ASIC board 'A'"
28: !SFTBSYB  PIN;"Soft busy from ASIC board 'B'"
29: !SFTBSYC  PIN;"Soft busy from ASIC board 'C'"
30: !WDTDLY   PIN;"Delay time of Watch dog timer from Event start"
31: EOFEVNT   PIN;"End of Event latch is set"
32: EOFEVNTD  PIN;"Event should be processed before this times out"
33: CLRBSY    PIN;"Three clear busys from cherst1 'ored'"
34: PLSI PROPERTY 'Y1_as_reset on';
35:
36: "!MRST  PIN_29; used for powerup reset, this gets 'ored' with FE_CLR"
37: "          and ABORT at the GLB level"
38:
39: " Outputs
40: [STAT7..STAT0] pin istype 'com,buffer';
41: LNKELED  pin istype 'com';
42: WDTERR   node istype 'reg,buffer';
43: BUSYLAT  node istype 'reg,buffer';
44: BUSY     pin istype 'com';
45: BSYLED   pin istype 'com';
46: FLT_IRQ  pin istype 'com';
47: WDTE     pin istype 'com';
48: EENDWDT  pin istype 'com';
49: EENDW    node istype 'reg,buffer';
50: MRESET   node istype 'com';
51: STATREG  node istype 'com';
52: ERR_REG  node istype 'com';"
53: "STATREG3 node istype 'com';"
54: LNKERR   node istype 'reg,buffer';
55: SOFTBSY  node istype 'com';
56: FAULT    node istype 'reg,buffer';

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57:
58: equations
59:
60: MRESET = FE_CLR # !ABORTP;
61:
62: " FE_CLR is the normal clear of busy and status flags after an event."
63: " ABORT is a pulse received over the link if the event needs to be terminated"
64: " for some reason. There is also a pulse on ABORT at powerup or on front"
65: " panel reset to clear all status conditions."
66:
67: [STAT7..STAT0].OE =FE_OE0 # FE_OE1;
68: STATREG = FE_OE0 & !FE_OE1;" Register selection."
69: ERR_REG = !FE_OE0 & FE_OE1;"
70: "STATREG3 = FE_OE0 & FE_OE1;"
71:
72: STAT7 = ( LINKRDY & STATREG # LNKERR & ERR_REG);
73: STAT6 = ( !BUSY & STATREG # BSYERR & ERR_REG);
74: STAT5 = ( 0 & STATREG # WDERR & ERR_REG);
75: STAT4 = ( 0 & STATREG # HBAD & ERR_REG);
76: STAT3 = ( 0 & STATREG # 0 & ERR_REG);
77: STAT2 = ( !EOFEVNT & STATREG # 0 & ERR_REG);
78: STAT1 = ( ST01 & STATREG # 0 & ERR_REG);
79: STAT0 = ( ST00 & STATREG # 0 & ERR_REG);
80:
81: " Master Busy Latch "
82: SOFTBSY = SFTBSYA # SFTBSYB # SFTBSYC;
83: BUSYLAT.D = 1;
84: BUSYLAT.CLK = ST00 & LINKRDY;
85: BUSYLAT.AR = MRESET;
86: BUSY = !(BUSYLAT # !LINKRDY # SOFTBSY # CLRBSY # LNKERR);
87: BSYLED = BUSY;
88:
89: " Link Error Latch "
90: LNKERR.CLK = !LINKRDY # HPERR;"This latch will allow link glitches to be detec
91: LNKERR.D =1;
92: LNKERR.AR = MRESET;
93: LNKELED = !(LNKERR # !LINKRDY);
94: " Fault Latch "
95: FAULT.CLK = BSYERR # HBAD # LNKERR # WDERR; "This latch is the error flag to
96: FAULT.D = 1; "boards when any error occurs."
97: FAULT.AR = MRESET;
98: FLT_IRQ = !FAULT;
99:
100: " Event arrival timeout Latch "
101: WDERR.CLK =!WDTDLY; "This latch is used with an external one_shot to forc
102: WDERR.D = ST00 # ST01; "if the event doesn't finish"
103: WDERR.AR = MRESET;
104: WDTE = !(WDERR # !LINKRDY);
105:
106: " Event process timeout latch "
107: EENDW.D = BUSYLAT;
108: EENDW.CLK = EOFEVNTD;
109: EENDW.AR = MRESET;
110: EENDWDT = !EENDW;
111: end
112:

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