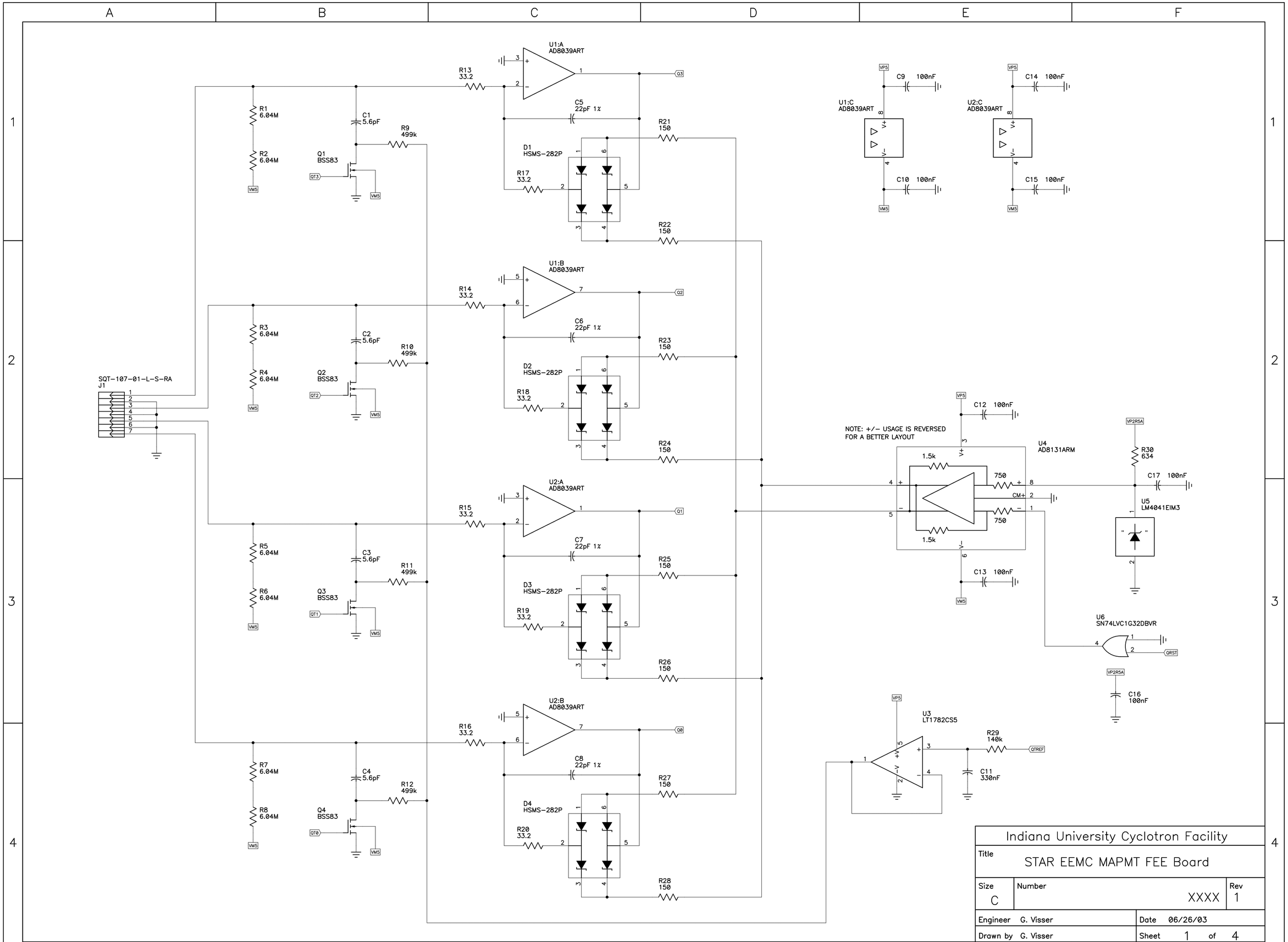
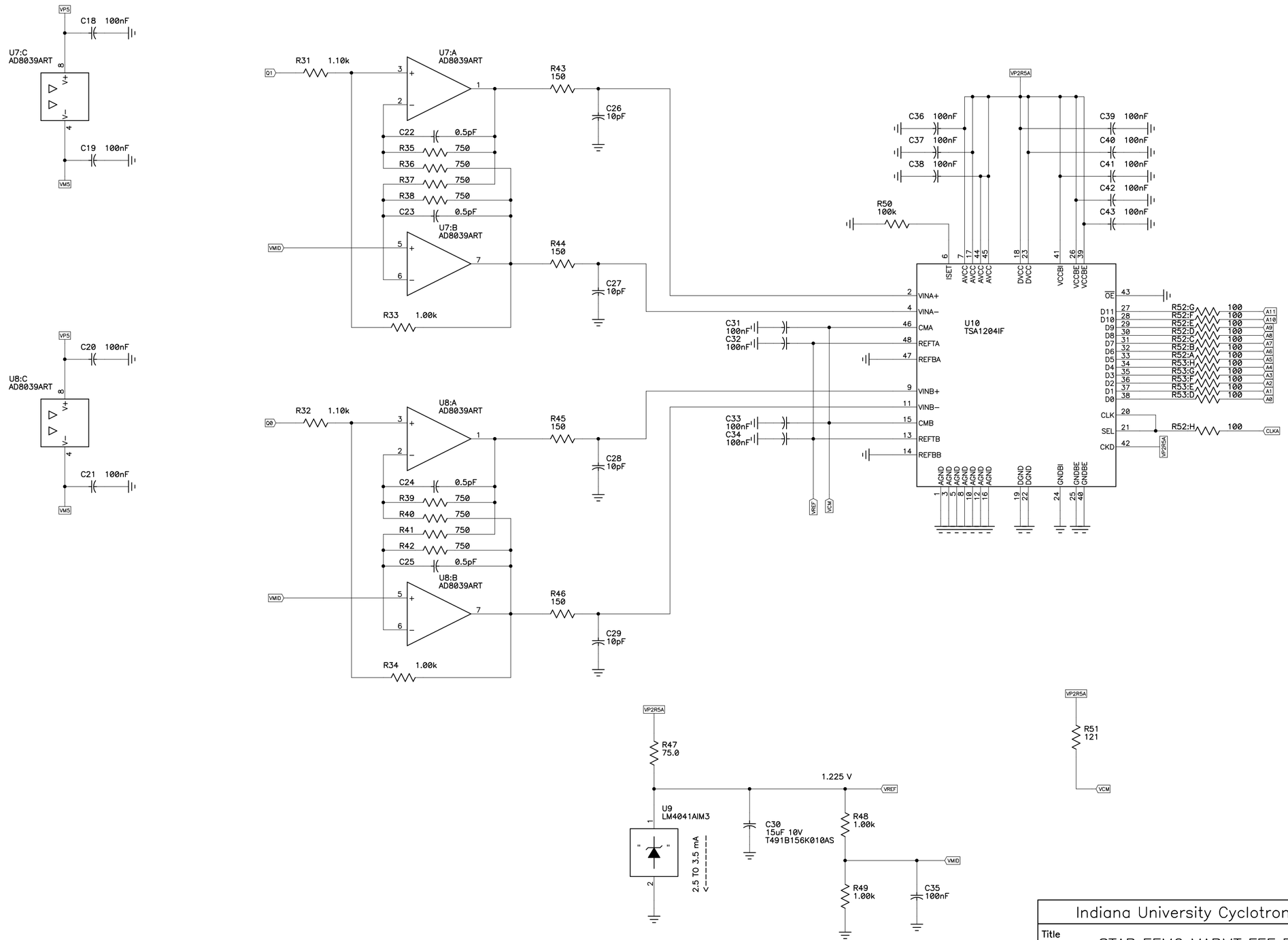
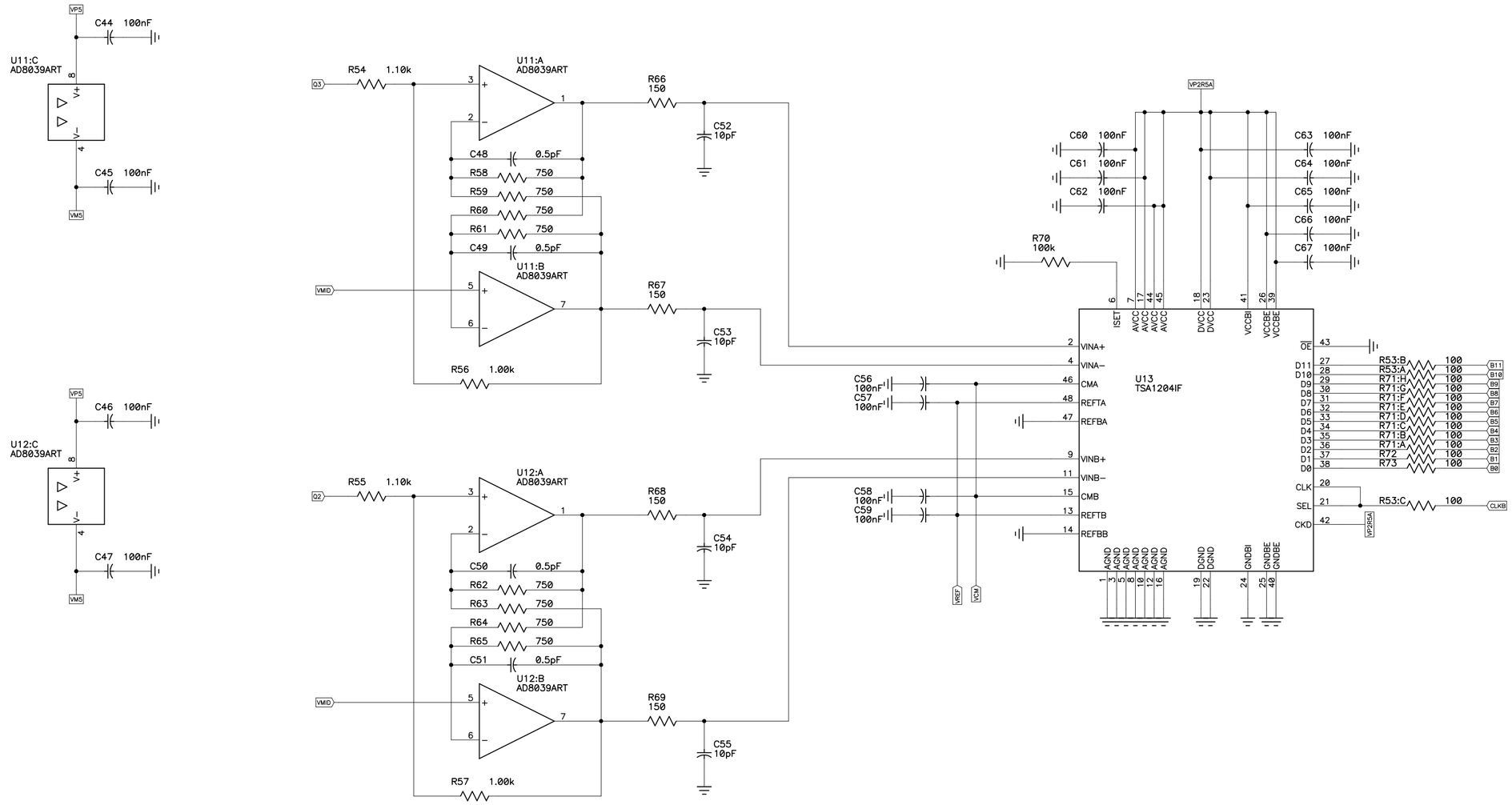


Indiana University Cyclotron Facility	
Title	STAR EEMC MAPMT FEE Board
Size C	Number XXXX
Rev 1	
Engineer G. Visser	Date 06/26/03
Drawn by G. Visser	Sheet 1 of 4



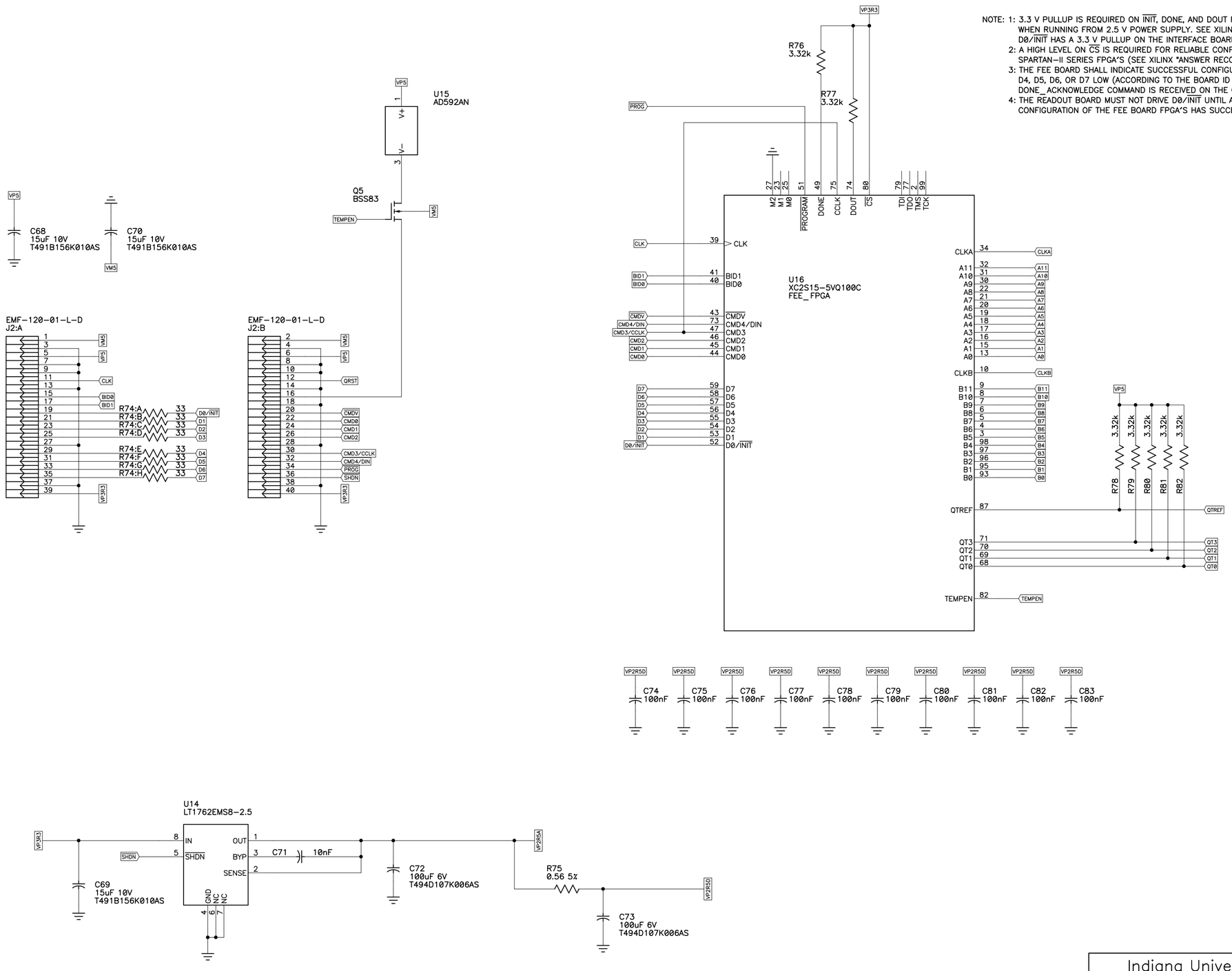
NOTE: TSA1204IF CLK INPUT MUST BE ACTIVE FOR EXTERNAL REFERENCE TO BE RECOGNIZED. IF CLK IS NOT ACTIVE, INTERNAL REFERENCE BUFFER WILL DRIVE VREF AND VOLTAGE WILL BE OUT OF SPECIFICATION. IN PARTICULAR, THIS WILL BE THE CASE IF THE FPGA IS NOT CONFIGURED.

Indiana University Cyclotron Facility		
Title: STAR EEMC MAPMT FEE Board		
Size: C	Number: XXXX	Rev: 1
Engineer: G. Visser	Date: 06/26/03	
Drawn by: G. Visser	Sheet 2 of 4	



Indiana University Cyclotron Facility		
Title: STAR EEMC MAPMT FEE Board		
Size: C	Number: XXXX	Rev: 1
Engineer: G. Visser	Date: 06/26/03	
Drawn by: G. Visser	Sheet 3 of 4	

NOTE: 1: 3.3 V PULLUP IS REQUIRED ON $\overline{\text{INIT}}$, DONE, AND DOUT FOR CONFIGURATION WHEN RUNNING FROM 2.5 V POWER SUPPLY. SEE XILINX APP. NOTE #176. D0/$\overline{\text{INIT}}$ HAS A 3.3 V PULLUP ON THE INTERFACE BOARD.
2: A HIGH LEVEL ON $\overline{\text{CS}}$ IS REQUIRED FOR RELIABLE CONFIGURATION OF SPARTAN–II SERIES FPGA'S (SEE XILINX "ANSWER RECORD" #8022).
3: THE FEE BOARD SHALL INDICATE SUCCESSFUL CONFIGURATION BY PULLING D4, D5, D6, OR D7 LOW (ACCORDING TO THE BOARD ID SELECTION), UNTIL THE DONE_ACKNOWLEDGE COMMAND IS RECEIVED ON THE CMD BUS.
4: THE READOUT BOARD MUST NOT DRIVE D0/$\overline{\text{INIT}}$ UNTIL AFTER CONFIGURATION OF THE FEE BOARD FPGA'S HAS SUCCEEDED.



Indiana University Cyclotron Facility	
Title	STAR EEMC MAPMT FEE Board
Size C	Number XXXX Rev 1
Engineer G. Visser	Date 06/26/03
Drawn by G. Visser	Sheet 4 of 4