STAR EEMC MAPMT FEE Design Review

Agenda

- Introduction
- Review of requirements and interfaces
- Block diagrams
- Specifications
- Schematics & FPGA design details
- Test results
- Production issues

Summary of Specifications

Some Features

• All FPGA's configure at power-up from a single configuration memory chip on the readout board; the configuration memory can be remotely reprogrammed in ≈ 1 minute via HDLC, and this can be done regardless of whether the FPGA's are programmed

• All FPGA's can be forced to reprogram via HDLC

• Box-specific initialization data may also be stored in the configuration memory and automatically executed at power-up *(not implemented yet)*

• Box phase, as well as internal reset phase and duration, are programmable using RC-delay circuits with ≈ 100 ps resolution

• Individual charge injection test pulser on each channel, amplitude set on a per FEE board basis *(not fully implemented yet)*

• "Reset-skipping" mode provides long integration capability for gamma source calibrations, and also allows for leakage current measurements

• Histogram mode builds histograms in FEE FPGA's for gamma source calibrations *(not implemented yet)*

• 12-bit monitor ADC watches all supply input currents & voltages, regulated +3.3 and +5 V supplies on readout board, center plate temperature, readout board temperature, and optional FEE board temperatures (sensors may not be installed on all boards)

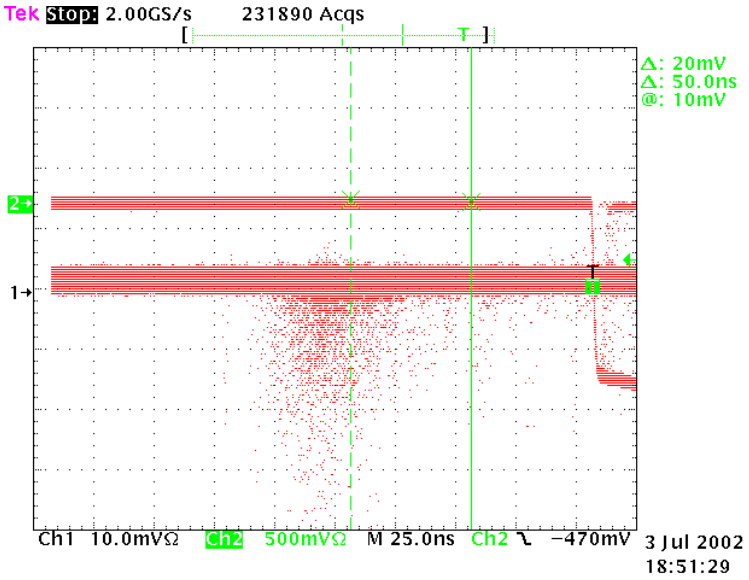
• Hardware power trip upon overtemperature at center plate or overvoltage on regulated +3.3 V supply (must cycle power to reset); status bit available to HDLC; HDLC board power is not cut

• Sequenced power-on of FEE assemblies for "soft start"

• Individual powerdown control bit for each FEE assembly; readout and control bus isolated through buffer chips at each FEE assembly; should allow for operation of rest of box if a FEE assembly is defective

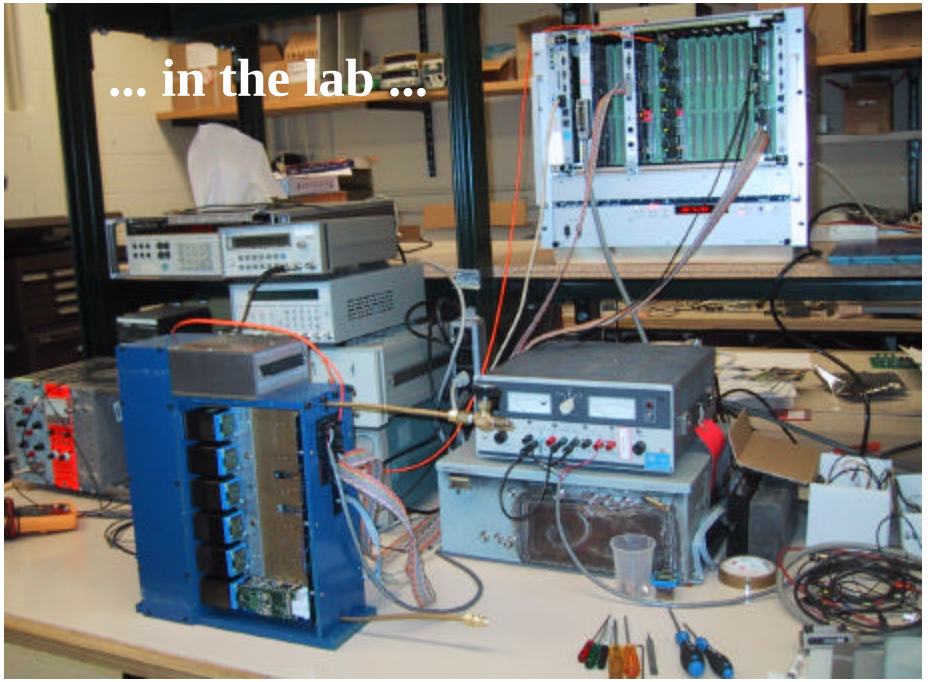
• FEE assemblies bolt directly to liquid-cooled center plate and rely only on conductive cooling

SMD / MAPMT Cosmic Ray pulses

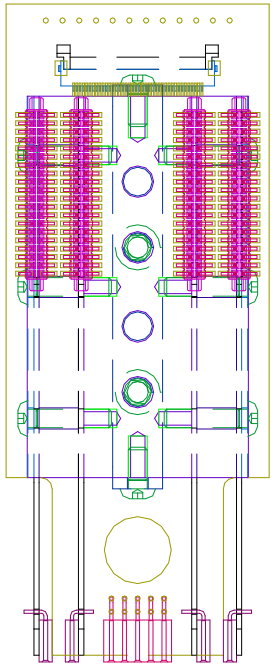


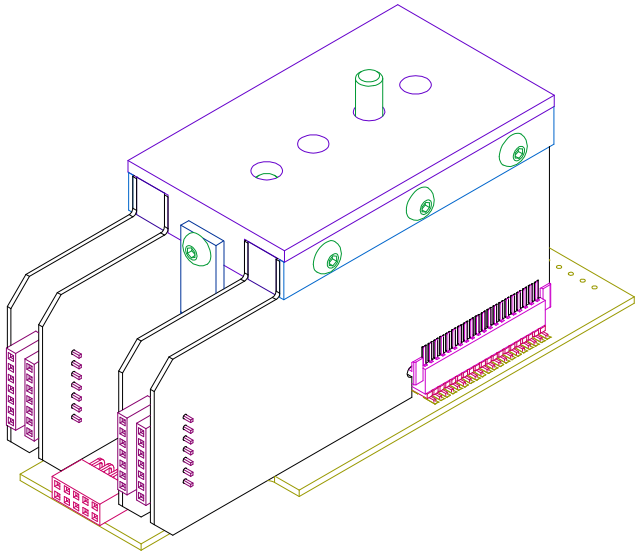
Note: The MAPMT is here connected with resistive base and 300 ns delay lines.

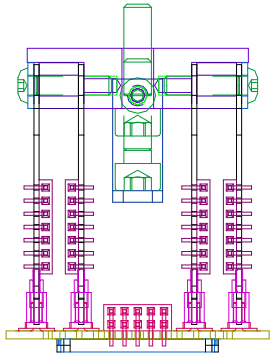
The box ...

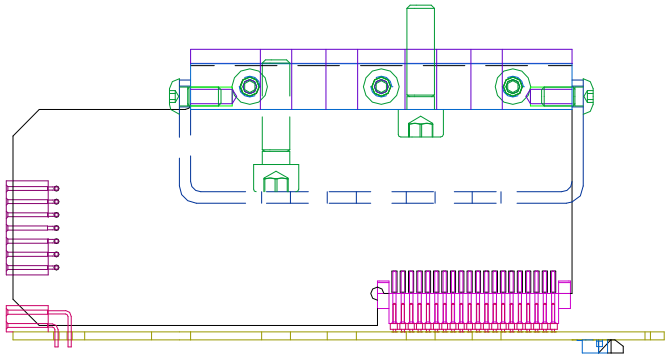


FEE Assembly (MAPMT and CW Base Sold Separately...)

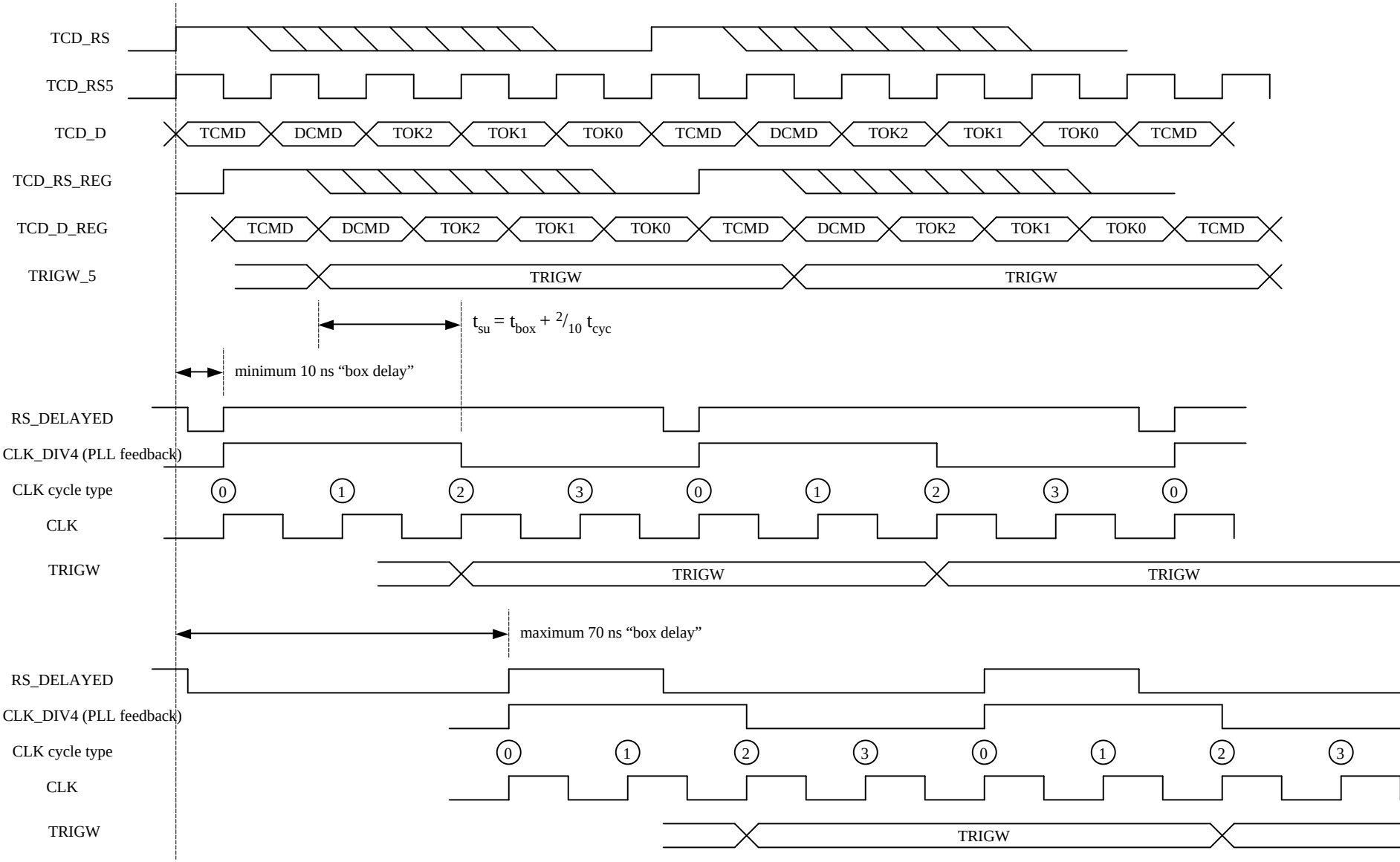




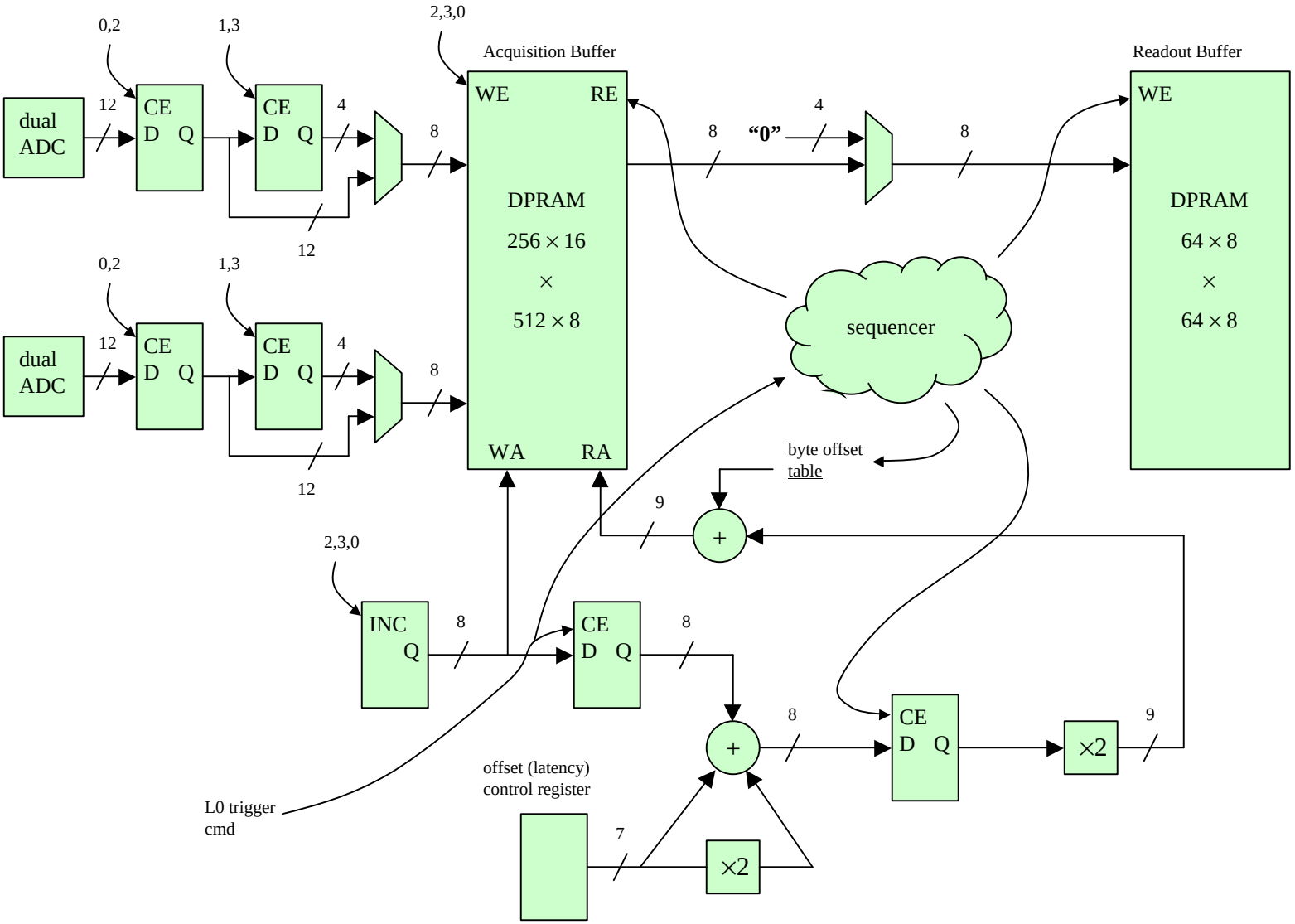




TCD Receiver Timing



FEE Data Handling



FEE Board Buffer Data Formats

ACQUISITION BUFFER (CIRCULAR BUFFER)

512 × 8, 6 bytes written on every RHIC cycle

(Actually written as three 16-bit words)

X	CH3[7:0]	
X+1	CH1[7:0]	
X+2	CH3[11:8]	CH2[11:8]
X+3	CH1[11:8]	CH0[11:8]
X+4	CH2[7:0]	
X+5	CH0[7:0]	

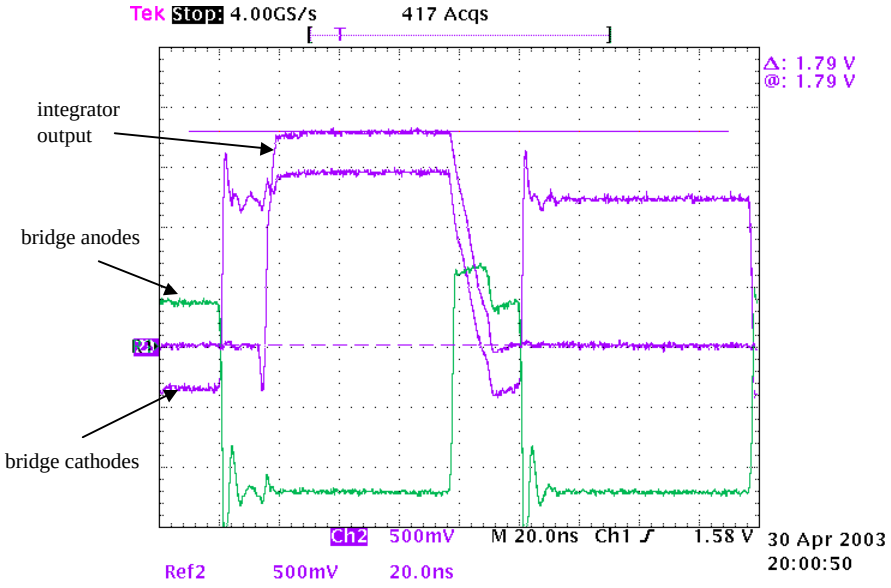
(X is the current value of the pointer for the first write of that cycle)

READOUT BUFFER

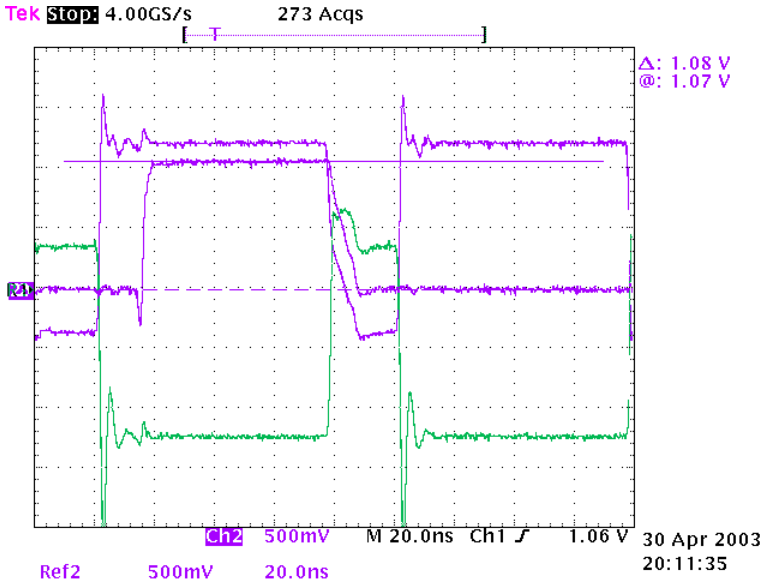
512 × 8, 8 bytes written on every L0 trigger

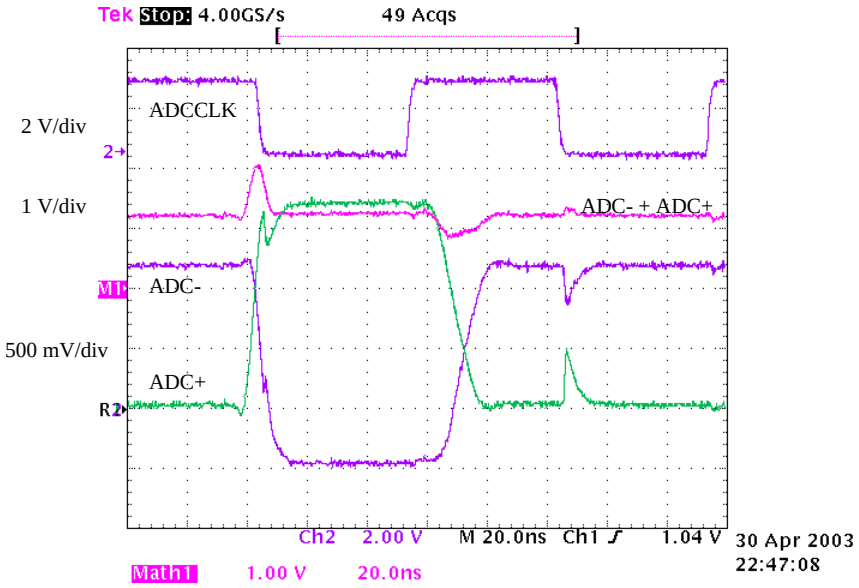
0	CH0[7:0]	
1	0000	CH0[11:8]
2	CH1[7:0]	
3	0000	CH1[11:8]
4	CH2[7:0]	
5	0000	CH2[11:8]
6	CH3[7:0]	
7	0000	CH3[11:8]

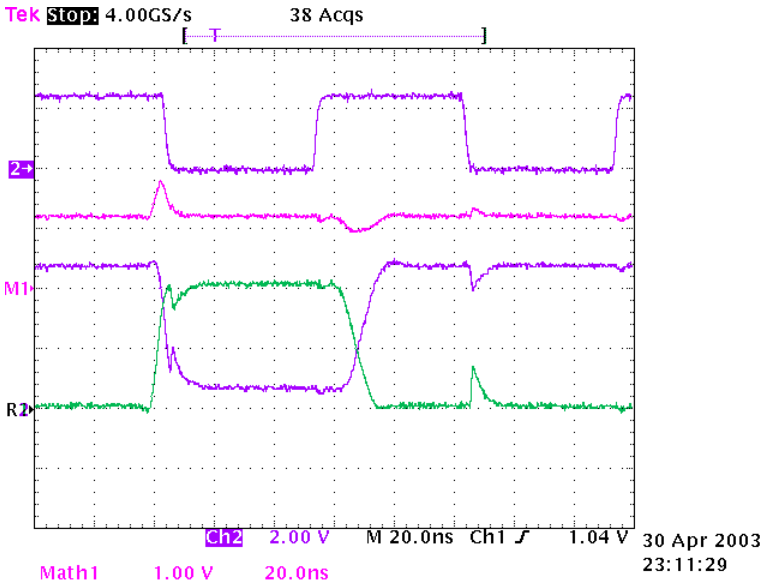
10 V (39 pC) event

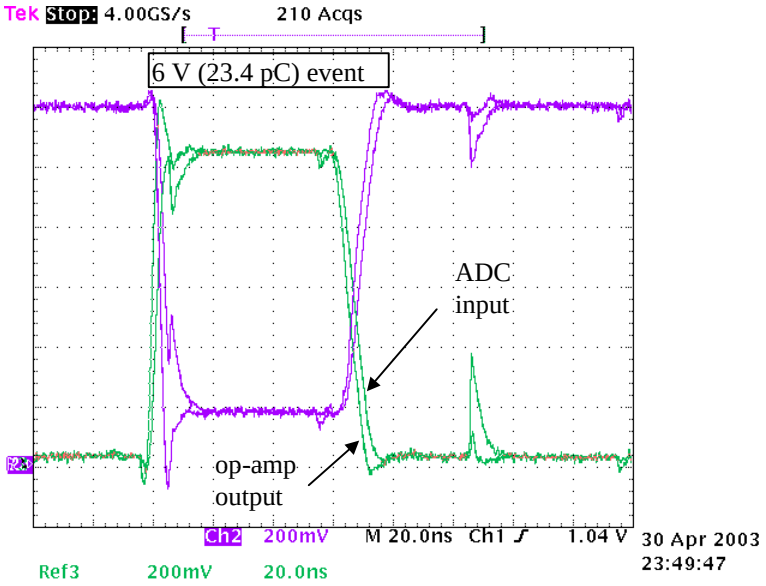


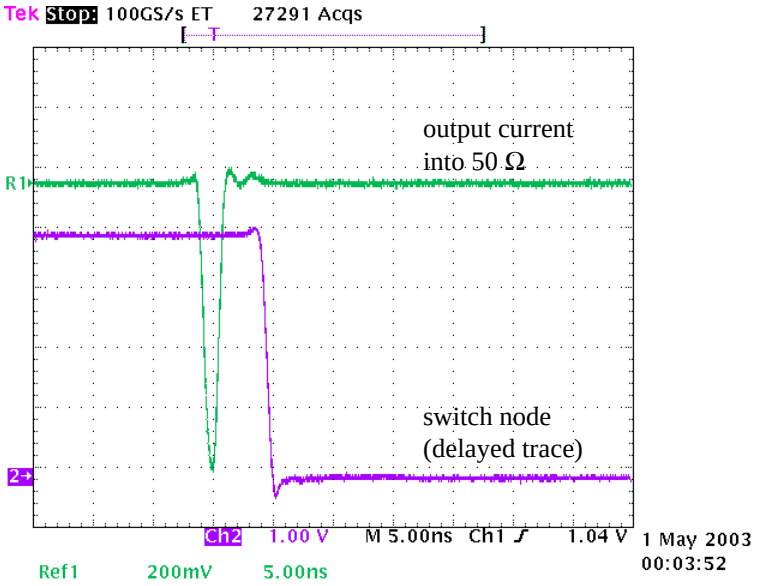
6 V (23.4 pC) event

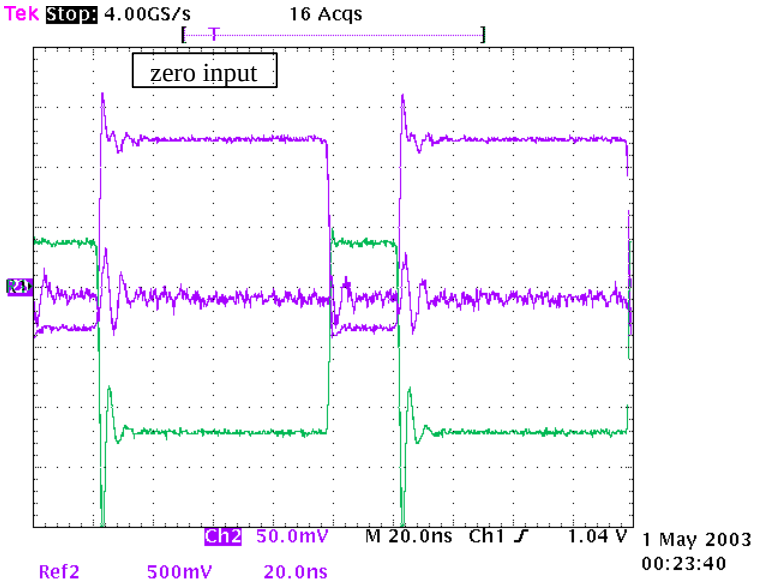


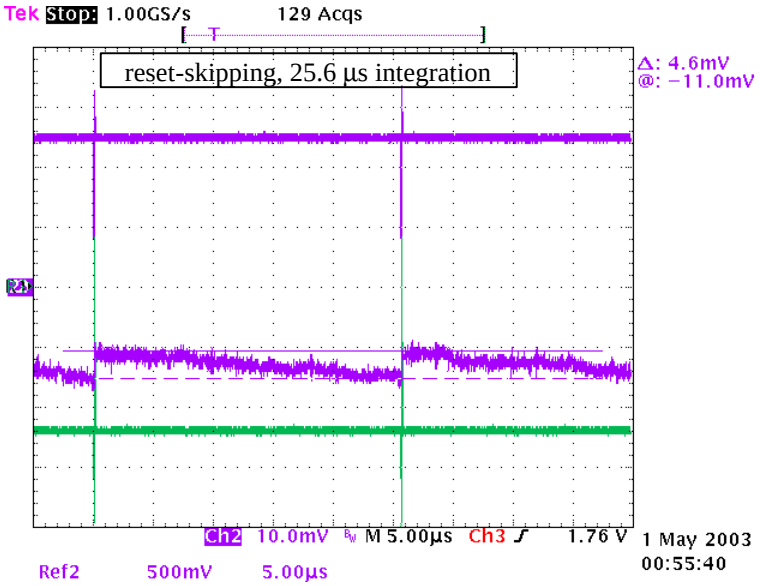






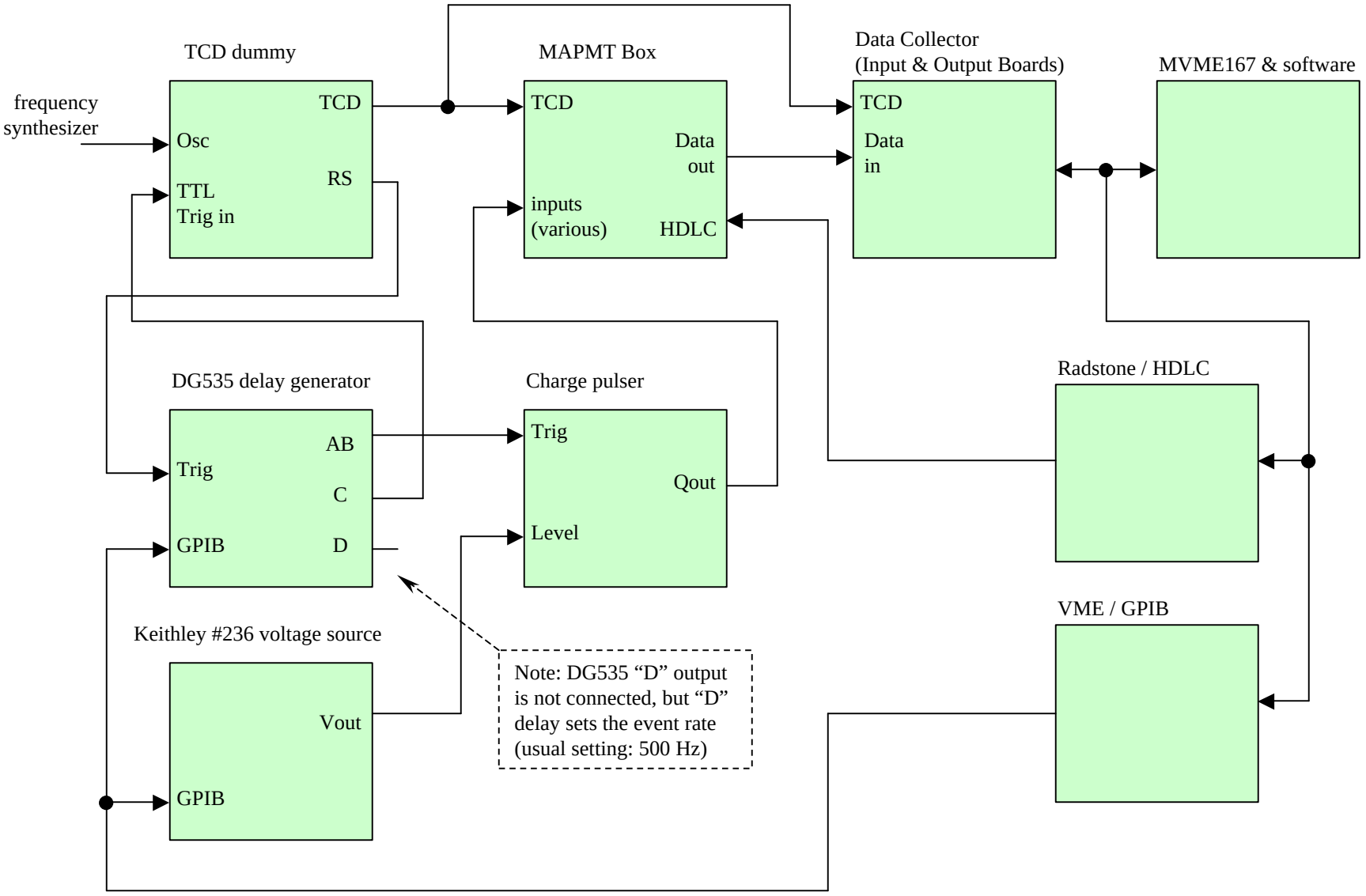


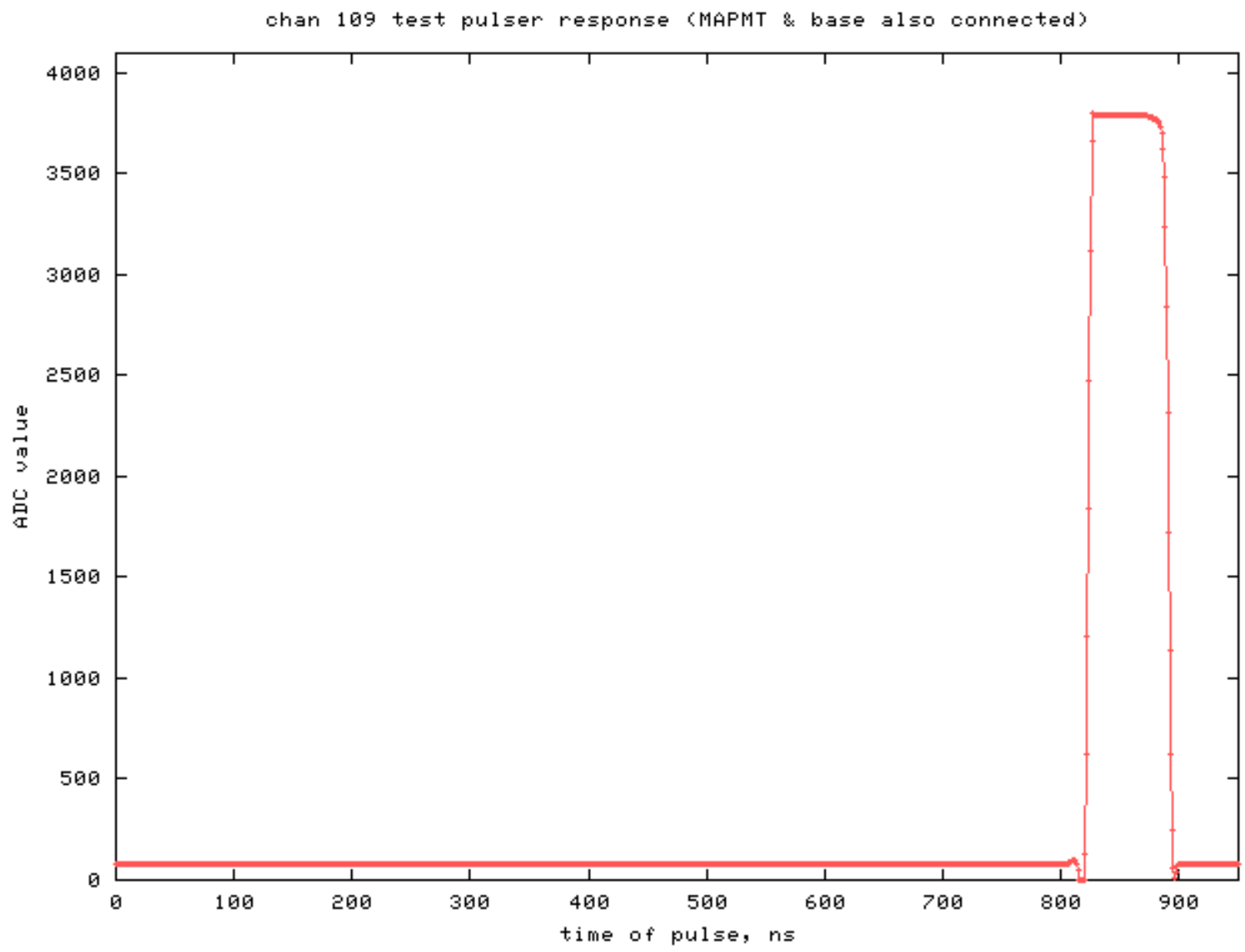


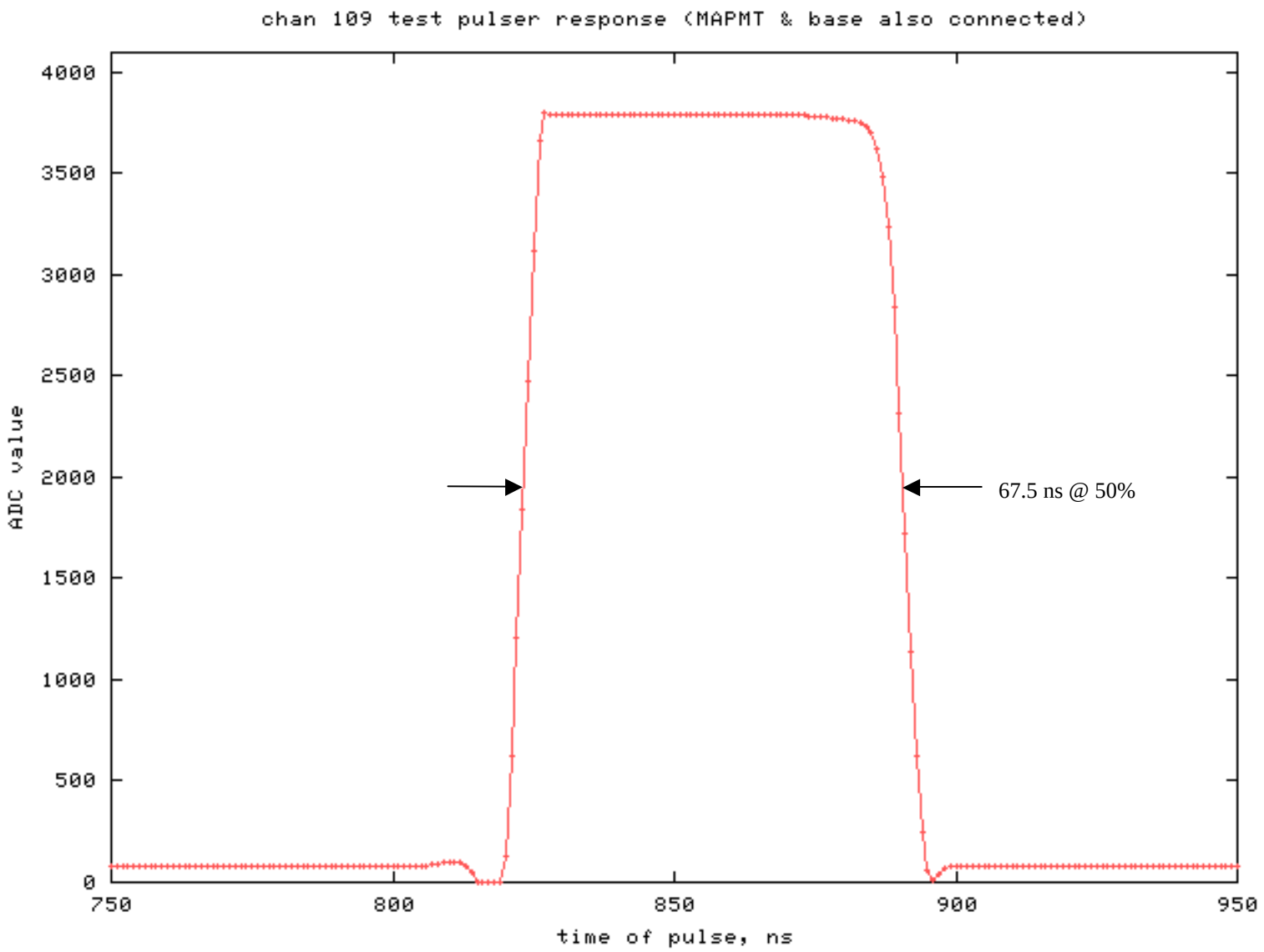


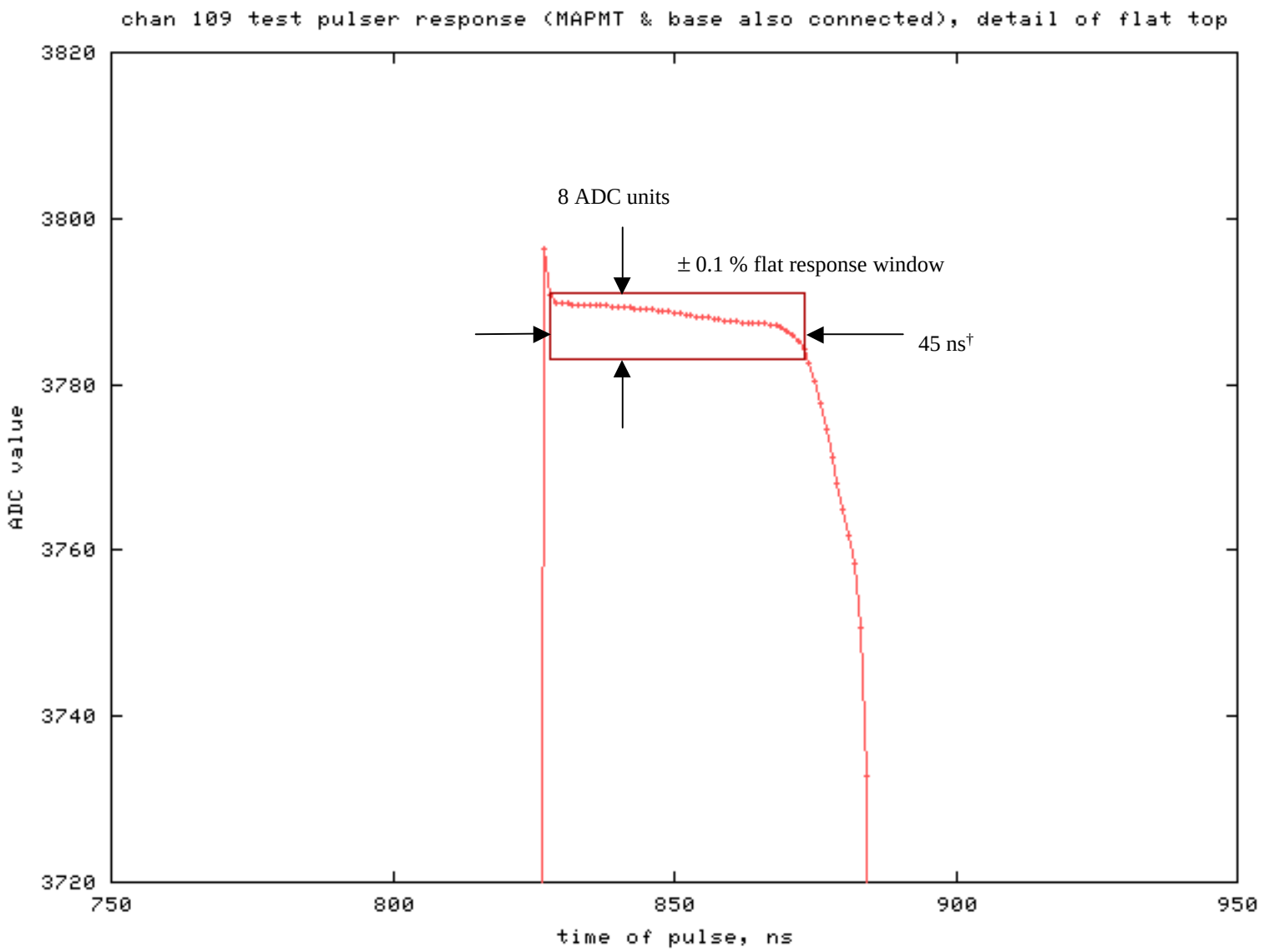
4.6 mV × 22 pF / 25.6 µs = 4 nA (expect ± tens of nA)

MAPMT Box Test Pulser Setup

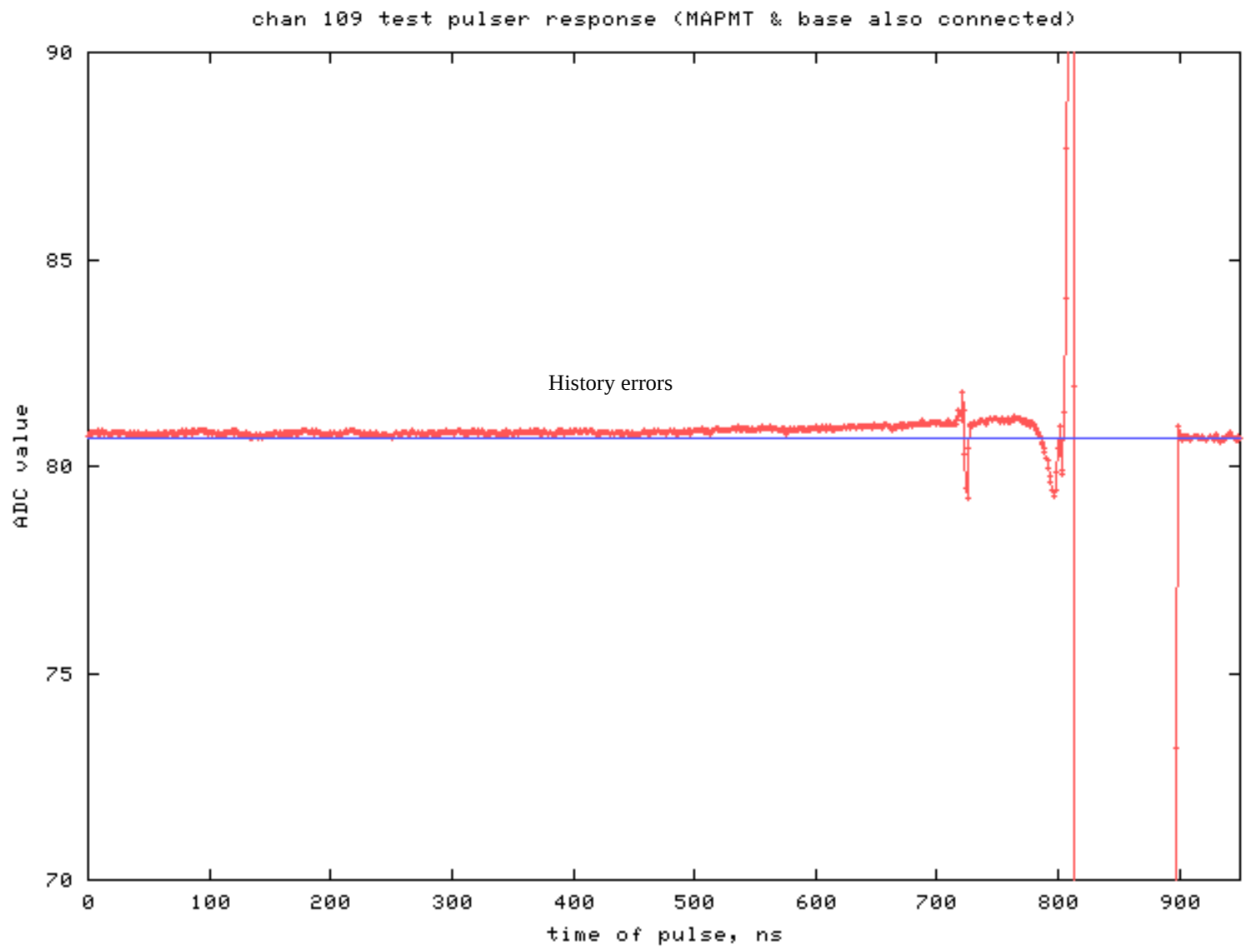


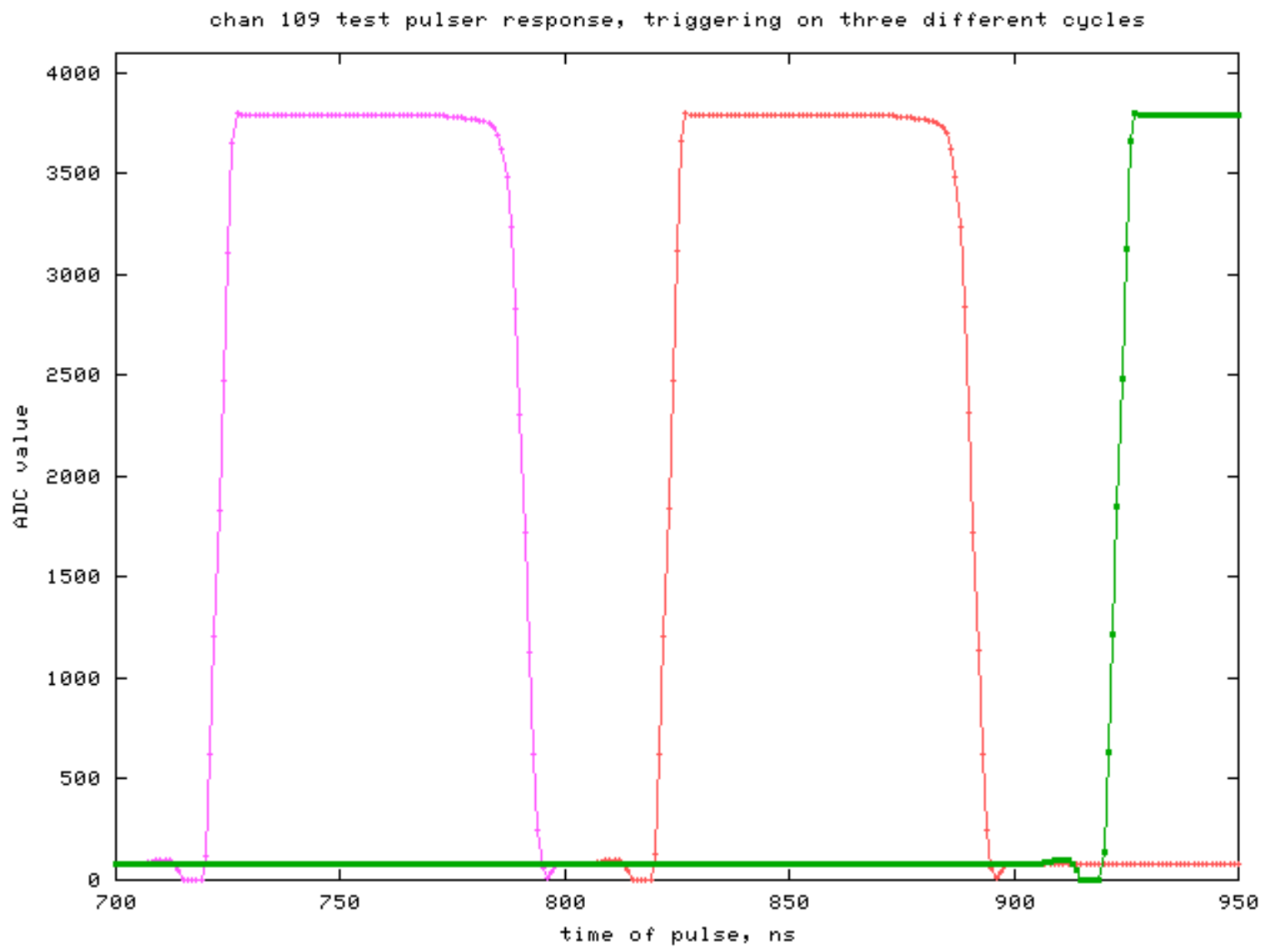

chan 109 test pulser response (MAPMT & base also connected)
ADC value
time of pulse, ns
0
500
1000
1500
2000
2500
3000
3500
4000
0
100
200
300
400
500
600
700
800
900

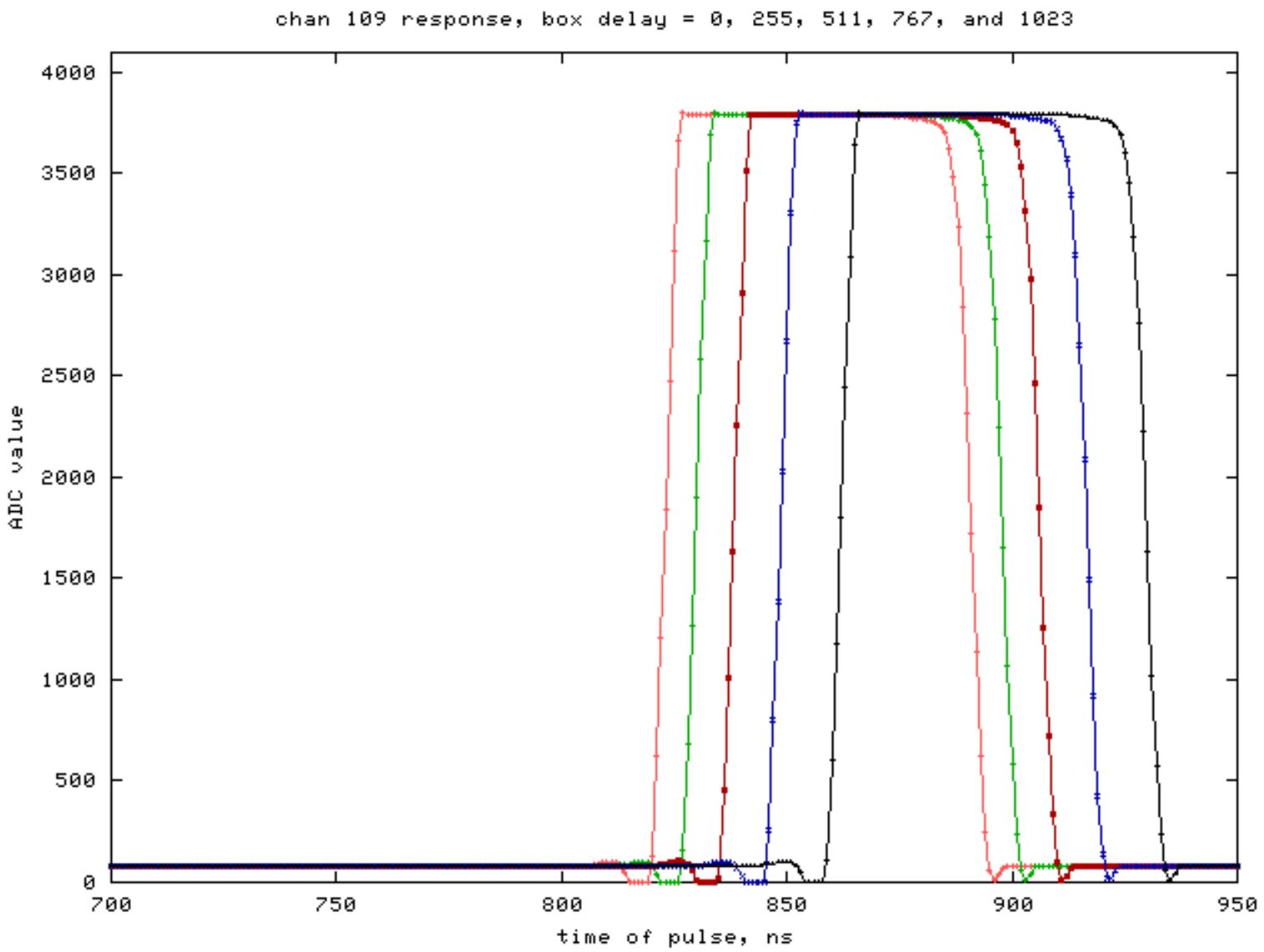

chan 109 test pulser response (MAPMT & base also connected)
ADC value
time of pulse, ns
4000
3500
3000
2500
2000
1500
1000
500
0
750
800
850
900
950
67.5 ns @ 50%

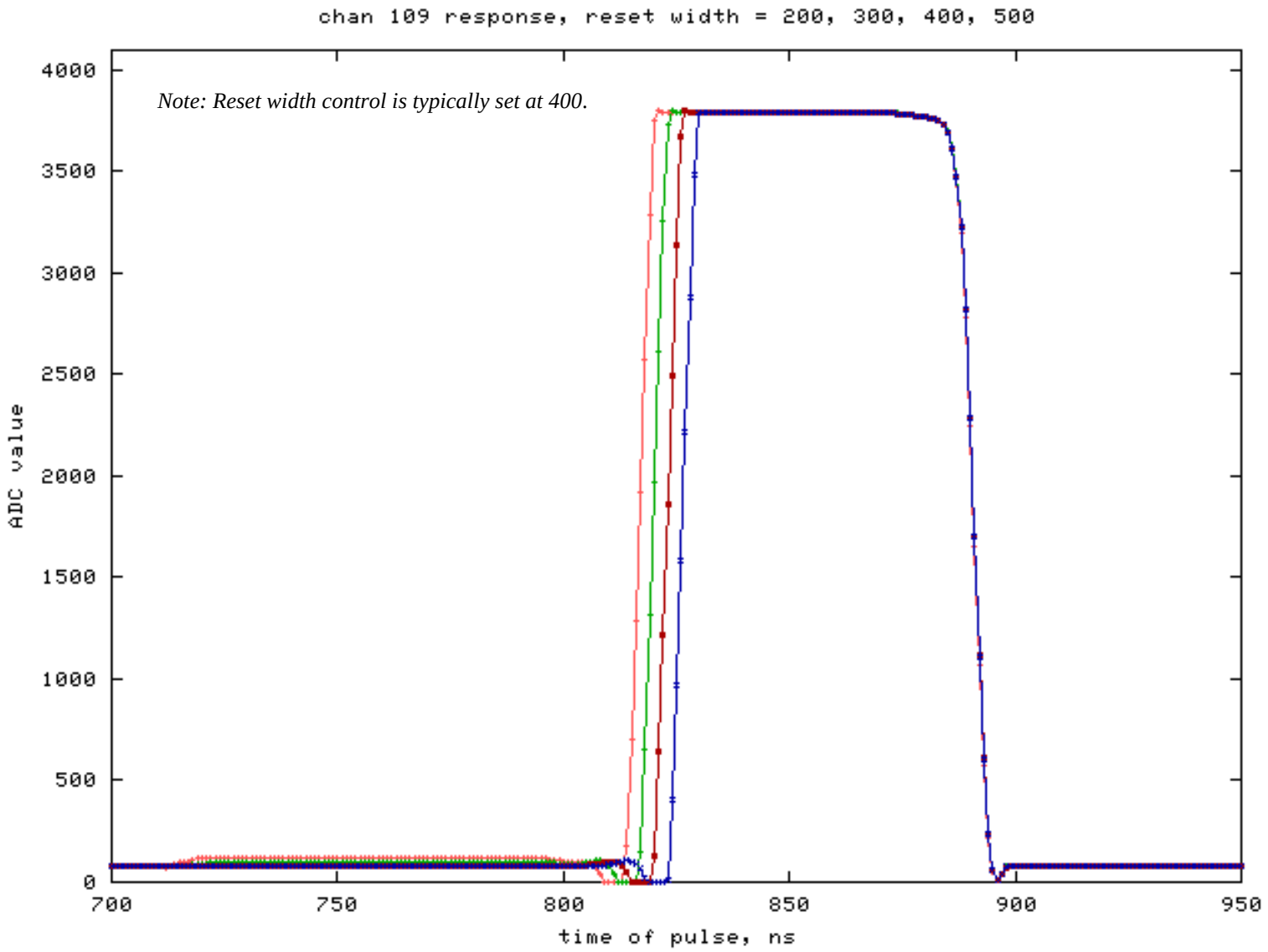


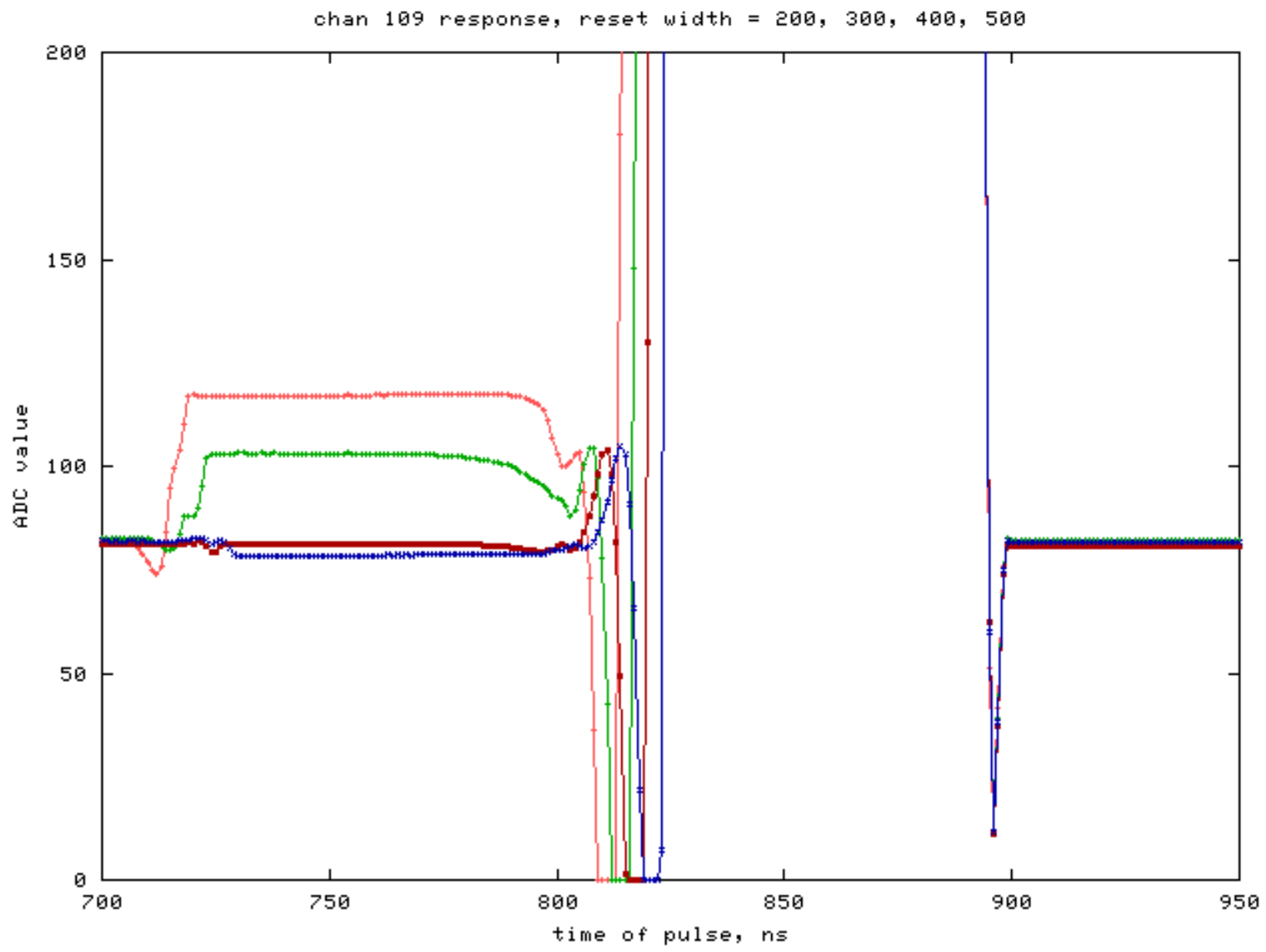
†Note: A 100 ns cycle is used here, so correspondingly there is a 52 ns flat-top @ RHIC cycle time

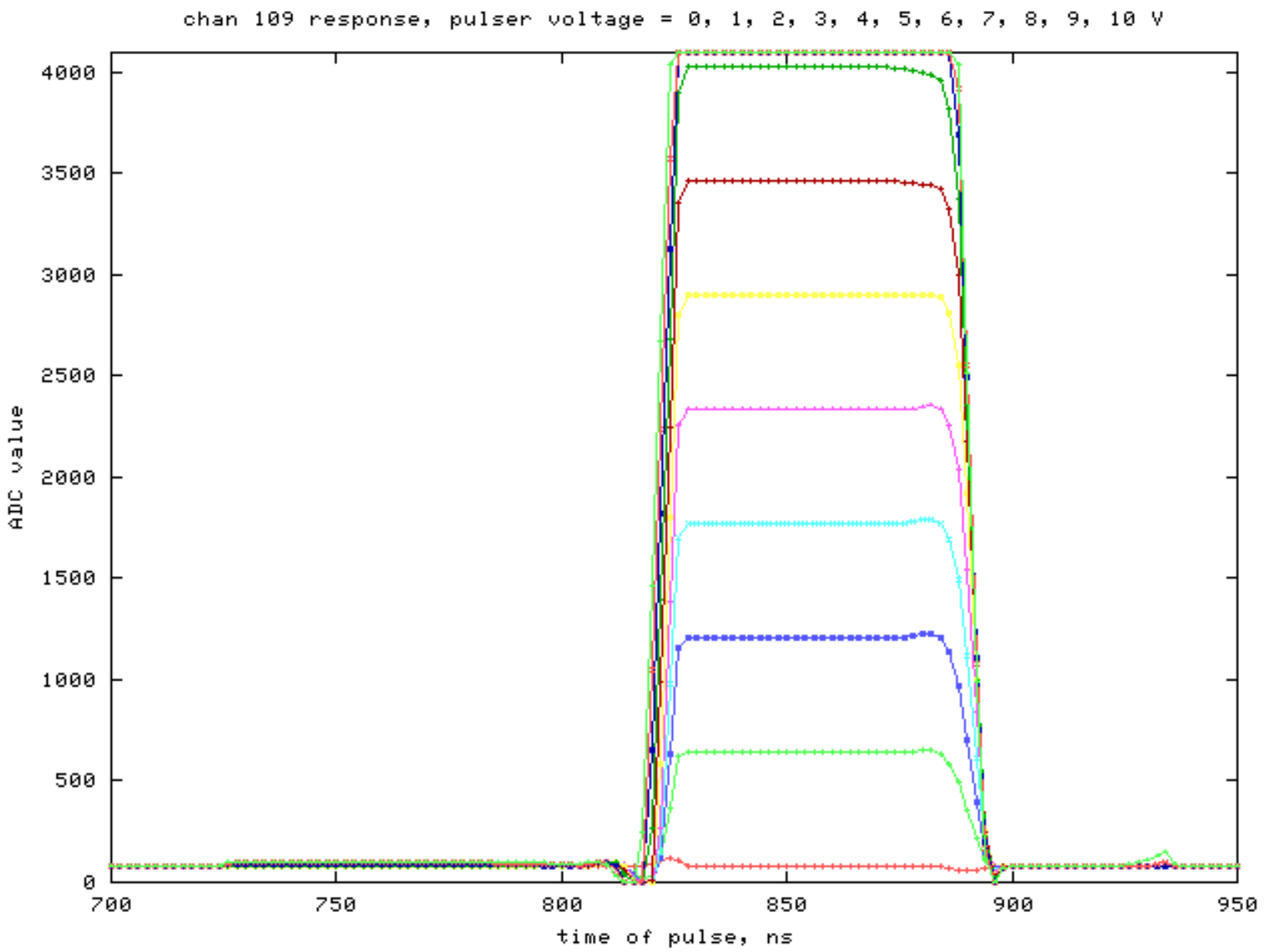

chan 109 test pulser response (MAPMT & base also connected)
History errors
ADC value
time of pulse, ns
90
85
80
75
70
0
100
200
300
400
500
600
700
800
900

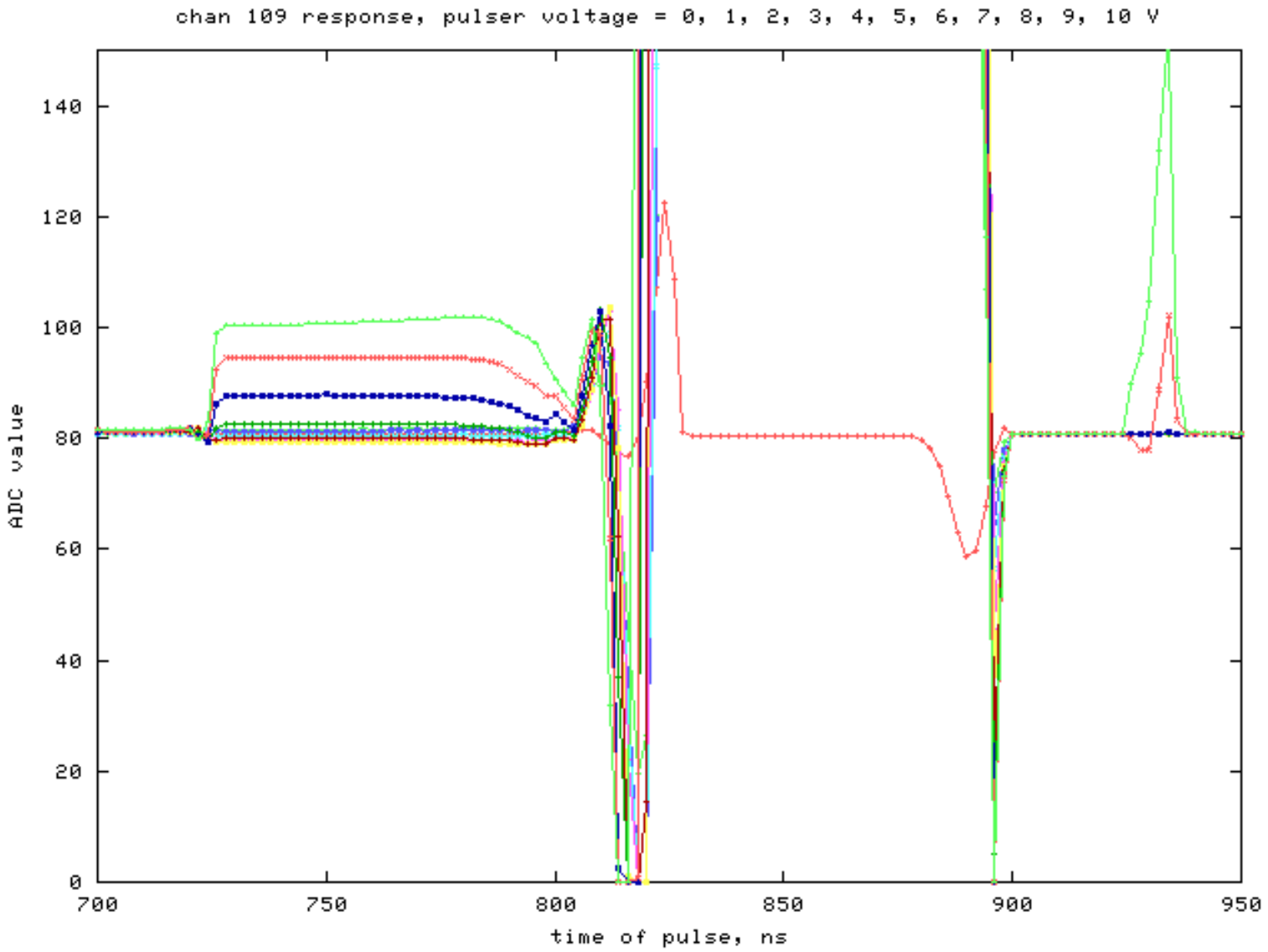

chan 109 test pulser response, triggering on three different cycles
ADC value
time of pulse, ns
0
500
1000
1500
2000
2500
3000
3500
4000
700
750
800
850
900
950

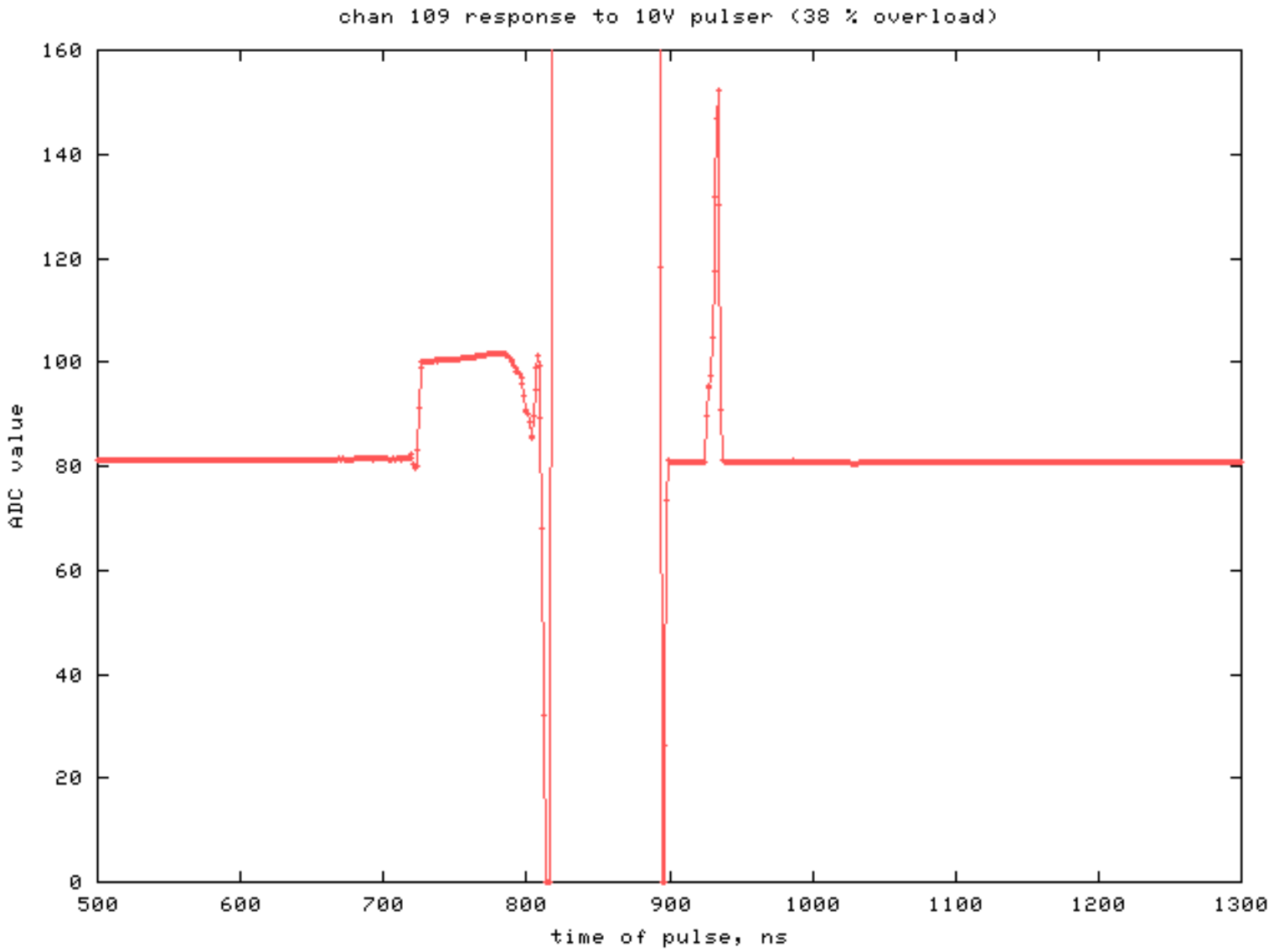

chan 109 response, box delay = 0, 255, 511, 767, and 1023
ADC value
time of pulse, ns
4000
3500
3000
2500
2000
1500
1000
500
0
700
750
800
850
900
950

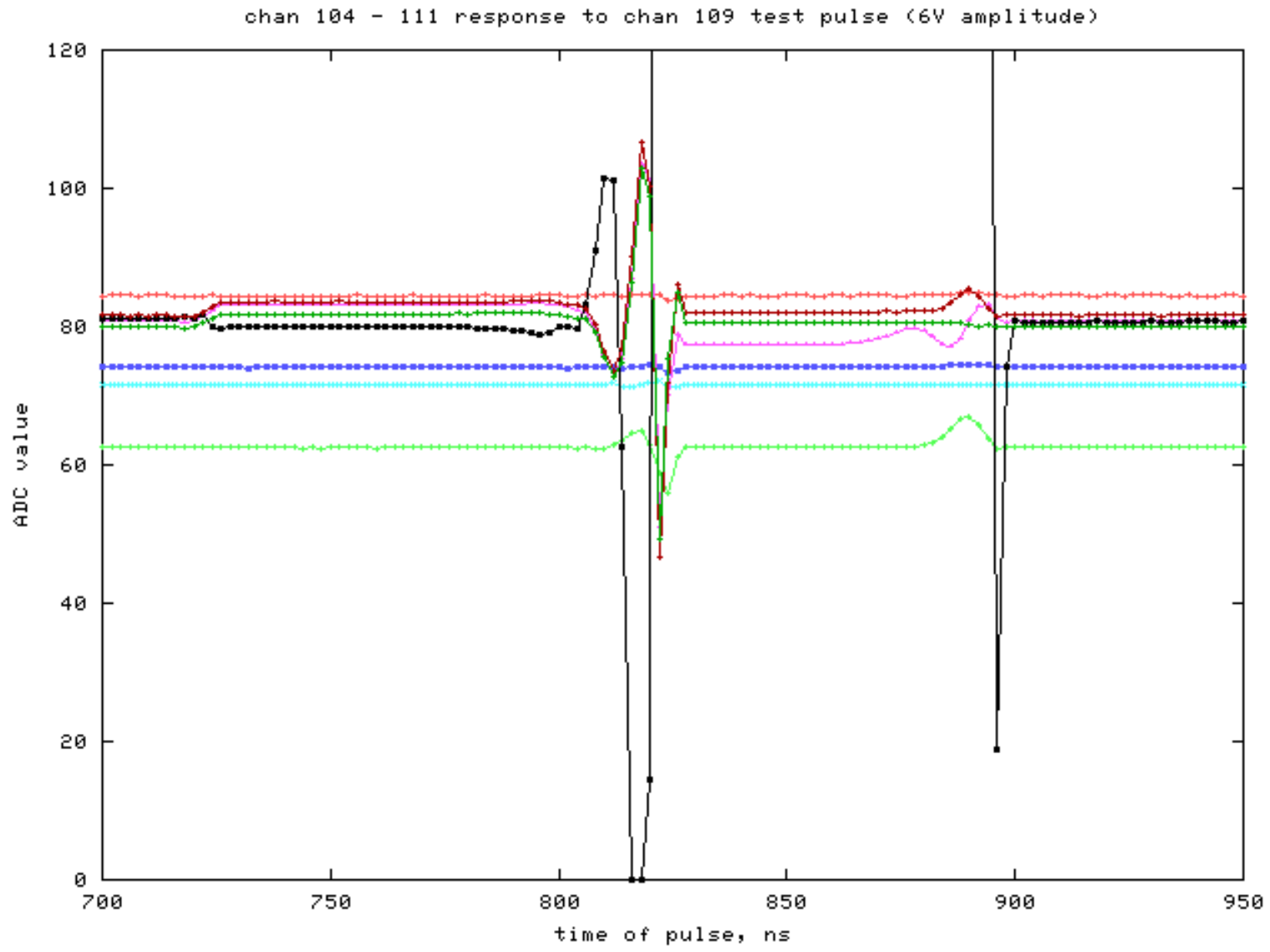

chan 109 response, reset width = 200, 300, 400, 500
Note: Reset width control is typically set at 400.
ADC value
4000
3500
3000
2500
2000
1500
1000
500
0
700
750
800
850
900
950
time of pulse, ns


chan 109 response, reset width = 200, 300, 400, 500
ADC value
time of pulse, ns
200
150
100
50
0
700
750
800
850
900
950

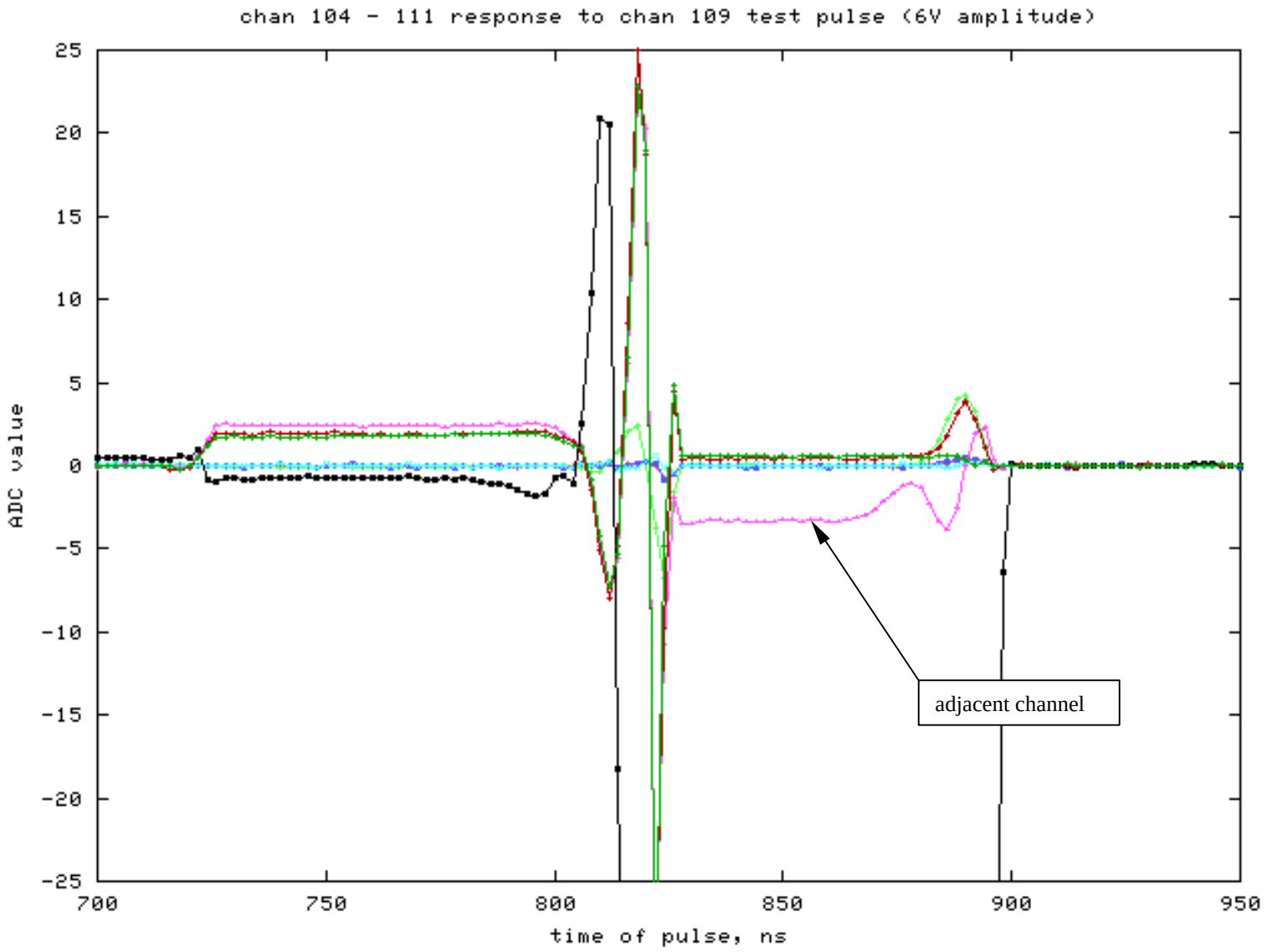

chan 109 response, pulser voltage = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 V
ADC value
time of pulse, ns
0
500
1000
1500
2000
2500
3000
3500
4000
700
750
800
850
900
950


chan 109 response, pulser voltage = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 V
ADC value
time of pulse, ns
0
20
40
60
80
100
120
140
700
750
800
850
900
950


chan 109 response to 10V pulser (38 % overload)
ADC value
time of pulse, ns
0
20
40
60
80
100
120
140
160
500
600
700
800
900
1000
1100
1200
1300


chan 104 - 111 response to chan 109 test pulse (6V amplitude)
ADC value
time of pulse, ns
120
100
80
60
40
20
0
700
750
800
850
900
950

Pedestal subtracted



- the CM slow controls access snafu...
- [RDO board] QRST delay flip-flop reset early due to mistake in logic design (QRSTEN not actually connected as a “clock enable” input as I had somehow convinced myself it was...) Fixed by tying *S to *Q instead of tying high. This has the desired effect since *R has priority over *S (??check that statement...) Easy change, to implement in next board revision.
- [FEE assembly] CLK rise/fall pretty slow – may be trouble... (seems not to be...)
- [RDO FPGA] DTACK was sometimes not released due to duplicated flip-flop with asynchronous input... This caused intermittent errors with slow controls transactions (once every few hundred transactions). (Apparently the mezzanine board happily starts the next transaction even if DTACK is already asserted – something to remember... I would have hoped for a bus error!) Fixed the problem by rearranging logic to avoid the hazard of duplicated flip-flops with asynchronous inputs.
- [Box] Bolts for insertion/extraction fixture on first prototype MAPMT box may intersect pcb’s. The hole locations have been modified for future boxes.
- [RDO board] Longer wait needed before FPGA master serial configuration (probably because of the time required for the serial flash memory chip’s internal reset). Fixed this by adding a 200 ms reset generator IC to the *INIT line.
- [System] I noticed that a dead short on +3.3 supply anywhere in box (even in FEE module) will take out the whole box, because of supply overcurrent timeout shutdown. I overlooked this... wanted to have the box immune to failures within any one FEE assembly... what to do?
- [System] On thinking about it, I see also now that we are NOT protected against a short between the +6 supply and the +3.3 regulated supply. This will probably destroy stuff if it were to happen. Should have had the OVP cut out all the supplies, not just the +4V input.
- [RDO board] Monitor signal multiplexor does not block signal currents on “off” channels if they drift outside of common mode voltage range. The current runs through (at least partially) to the output anyway. I overlooked this in the design (thought the “off” signal currents would go to the supply rails only). Fixed by adding clamp diodes to ground on all susceptible input signals.

MAPMT FEE Protype Build Results

- Hand-assembled at IUCF: 4 boards
- Machine-assembled at EMS Inc.: 54 boards
    - 46 are complete
    - 8 missing FPGA and/or ADC's owing to short supply
    - connectors hand-assembled by EMS Inc. technicians
- Yield: 36 tested good out of 46; problems are:
    - 10 "whisker" solder bridges on 6 different boards
        - 8 at AD8039ART (op amp in 8-lead "SOT-23")
        - 1 at TSA1204IF (the ADC)
        - 1 at XC2S15-5VQ100C (the FPGA)
        - we suspect some problem like moisture in the solder paste...
    - 2 cracked AD8039ART on 2 different boards
    - 1 connector was mis-placed (a mechanical problem only, electrical test ok)
    - 1 wrong part used (LT1782CS5 in place of SN74LVC1G32DBVR)
    - 1 very skew capacitor (mechanical problem only)
    - 1 cracked ceramic capacitor (solder joint was cracked as well), cause is not clear...
    - 1 board simply re-tested ok with no rework... cleaned & returned to service...
- 1 board apparently failed since initial testing, op-amp gone bad