Design and Test of a CMOS Low-Power Mixed-Analog/Digital ASIC for Radiation Detector Readout Front Ends

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Abstract

A new CMOS low-power mixed A/D ASIC for radiation detector readout front ends is presented[*] . First, we recall the principle of radiation detection system before describing the whole architecture of the circuit. The discussion is then focused on the low-power issue. By means of an innovative 128:1 analog multiplexer, we show how we drastically reduced the mean power consumption without sacrificing constraining specifications such as the input range and the readout rate. Testing mixed A/D, but strongly analog IC is also a big issue which is addressed here. Specific built-in test analog sub-circuits have been implemented in the ASIC, along with a JTAG module used to choose the type of test to perform. This module is also used to control and tune the biasing currents of the circuit. Finally, test results are presented and show that all the specifications are satisfied.

I.- Introduction

In elementary particle physics, the front end amplifying system of figure 1 is widely used to measure the energies of radiation particles [1]. A fully depleted diode acts as the particle detector. When a particle thouroughly crosses the diode, a quantity of electron-hole pairs, proportional to the absorbed energy, is generated. The high electric field taking place in the diode collects this generated charge Q which gives birth to a current pulse δI. A charge sensitive amplifier (CSA) integrates δI onto the small feedback capacitance C_f and provides a step voltage signal of an amplitude equal to Q/C_f. This step signal enters a CR-RC band-pass filter, often known as a pulse shaper, mainly to optimize the S/N ratio of the system and also to eliminate the pile-up phenomenon occurring at the output of the CSA when successive radiation events appear in a short period of time. Finally, a pulse processing unit starts to process the analog signal before sending data to the end-caps of the whole particle detector where the processing is completed. The CR-RC filter shapes the signal in such a way that the peaking time of the resulting pulse remains constant. So, very often, the first processing unit is limited to a storage of the analog signal onto a capacitance, signal which will be read afterwards by means of a predetermined readout cycle.

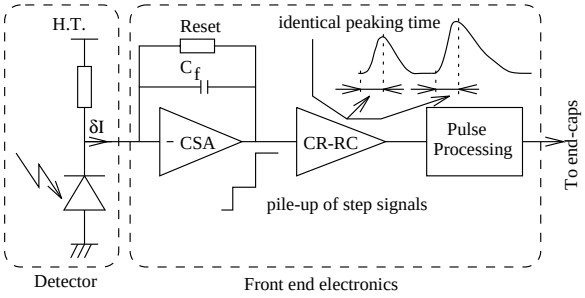

Fig. 1 : Front end amplifying system principle

The number of identical channels will drastically increase in the future detectors at CERN (European Center for Nuclear Research). For example, in the ALICE experiment [2], foreseen to run in 2004, the Internal Tracking System (ITS) silicon strip layers will contain approximately 2.6 million channels. Obviously, keeping in mind the silicon strip detectors (SSD) temperature which has to be maintained around 30°C, the mean power dissipated per channel must be kept very low, namely under 1mW/channel. This is one of the main issues we addressed with ALICE128C, the ASIC presented here. The solution used to minimize dissipation is presented in the next section. Control and testability were the other issues to address. Due to transistor parameter dispersions, the biasing of all the analog blocks must be remotely adjustable. Furthermore, during the span of the particle physics experiment (typically 10 years), the circuit has to be tested periodically in order to check if no channel is out of order or so as to compensate some deviations for the

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gain and/or for the shaping time. Section 3 deals with the methodology we chose to address these issues. Finally, section 4 provides first test results.

II.- Circuit design

A.- Circuit description

Figure 2 gives the block diagram of ALICE128C. It is a 128 channels chip designed with the AMS 1.2µm CMOS technology (die size : 6mm x 8.5mm). Each channel amplifies, shapes and stores onto the capacitance C_{HOLD} the charge deposited on a strip of the detector. This storage is triggered by the external HOLD logic signal which arises τs seconds after the radiation event. This shaping time (τs) is adjustable from 1.4µs to 1.8µs. An analog multiplexer allows a sequential readout of the data at a rate of 10MHz through a tristate output buffer shared by the 128 channels. The output buffer has been designed to drive an external link with a 100Ω characteristic impedance in parallel with a capacitance up to 20pF. The tristate property of the output buffer allows a daisy chain of several ALICE128C chips onto the same external link. A slow control mechanism compatible with the ‘‘JTAG IEEE1149.1” standard is used to accurately bias the different analog blocks and to control the shaping time. It also controls an internal test pulse generator which provides a variable current pulse emulating a deposited charge up to ± 15MIPs (MIP : Minimum Ionizing Particle ; 1MIP=22000e^-).

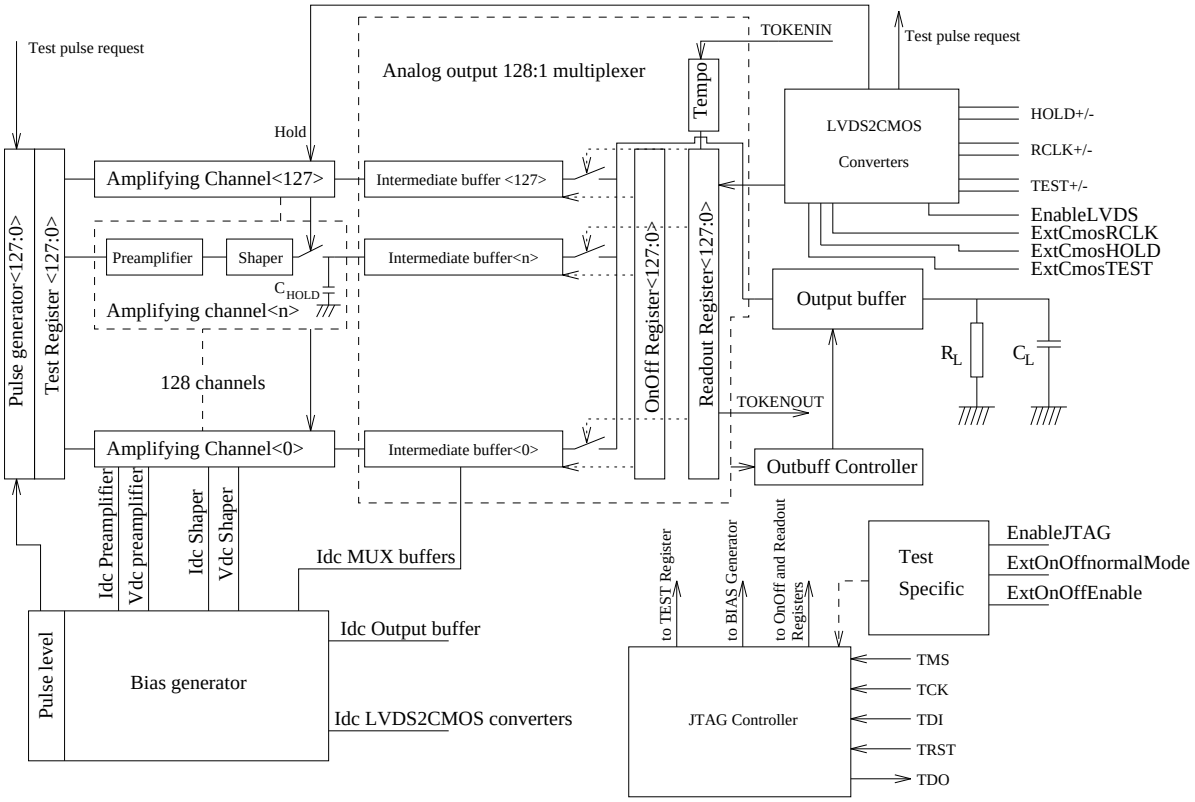

Fig. 2 : Block diagram of ALICE128C

The relevant specifications of the circuit are summarized in table 1. A description of each block has been given yet in [3]. So we now focus our discussion on the main issue which is the reduction of the mean power dissipated per channel.

B.- Low-power issue

Due to noise considerations, the CSA and the shaper dissipate 200µW and 90µW respectively [3]. Keeping in mind the 100Ω characteristic impedance of the external link and the ±1V range of the output voltage (a conservative ±20 MIPs is assumed at the input), the maximum output current is 10mA. Assuming the ±2V power supply, the minimum power the output buffer dissipates at full range is 20mW. Due to linearity constraints, the output buffer implemented in ALICE128C dissipates more than this minimum value. Using a class AB output stage, its power dissipation is quite constant over the whole input range with a value of 33.8mW, which means 264µW per channel (buffer always switched on).

Name	Specification
Input range	±13 MIPs
ENC	≤ 400 e^-
Readout rate	10 MHz
Power	≤ 1mW / Channel
Gain	≈ 50 mV/MIP
Shaping time	1.4 μs ≤ τs ≤ 1.8 μs

Table 1 : ALICE128C main specifications

The last main source of power dissipation takes place into the analog 128:1 multiplexer. The signal stored onto C_{HOLD} enters an intermediate buffer which drives the parasitic capacitance at the output of the 128:1 multiplexer. This parasitic capacitance is high (≈ 1pF) due to the number of channels. In addition, the 1°/oo settling time of the intermediate buffer has been chosen equal to 30ns in relationship with the 10MHz readout rate. These two constraints lead to a buffer which dissipates around 7.5mW. Obviously, this value is definitely incompatible with the 446μW/channel remaining to satisfy the 1mW/channel specification of table 1. Consequently, the intermediate buffers are switched on only during the readout of their corresponding channel. More accurately, in order to speed up the 1°/oo output settling in respect to the 10MHz readout rate, and to reduce the noise induced by the on/off switching mechanism, the adjacent buffers «n-1» and «n+1» are kept on during the readout of channel «n» while the buffer «n-2» is switched off and the buffer «n+2» switched on. So, during the readout cycle, only four intermediate buffers are dissipating power.

This on/off switching mechanism would be a very noisy system if no particular care were taken during the design. To reduce crosstalk between adjacent channels, a guard ring is placed around each channel (from the CSA to the output of the 128:1 multiplexer). This guard ring contributes to reduce the on/off switching noise. Nevertheless, it is not sufficient because of a harmful parasitic coupling taking place through the biasing sub-circuit common to all the 128 intermediate buffers. When a buffer is switched off, by switching off its biasing current, a voltage spike occurs into the biasing sub-circuit. The spike amplitude is about 90mV and disturbs the output voltage provided by the buffer of the channel being read. So, four identical but independent biasing sub-circuits were implemented. The first one bias the set of buffers corresponding to the set of channels 0+4n, the second one bias the set of buffers 1+4n,..., up to the last one which bias the set of buffers 3+4n. In such a way, during the readout cycle, the couple of buffers which are switched (one switched on and the other switched off) is connected onto the same biasing line. Switching noise occurs on this line with voltage spikes of about 90mV too. In return, the buffer of the channel being read is not disturbed since it is not connected to the same biasing line. The SPICE simulations performed with this biasing system don't show any noticeable parasitic coupling. Nevertheless, to ensure a perfect rejection of the switching noise, the four biasing lines were also shielded.

Thanks to this switching mechanism, the mean power dissipation per channel were drastically reduced to 340μW/channel, assuming a typical readout period of 1ms [3]. This value is well below the best value (around 1.2mW/channel) proposed by industrial products dedicaded to the same radiation measurement applications [4].

III.- Control and testability

For a readout front end chip used during almost ten years in high energy spectrometers, the capability to check periodically the functionality of the circuit, to adjust the analog parameters in case of harmful deviations, and also to disconnect a circuit out of order from the readout daisy chain, is obviously important. This must be done remotely and without requiring a lot of links since the circuit is situed into the heart of the spectrometer. So, in order to minimize the number of interconnections, all the chips are connected serially according to the JTAG-IEEE 1149.1 protocol [5].

ALICE128C is mainly an analog circuit, the digital part including only the JTAG module and the readout controller. In order to test the analog part, we added a current pulse generator (one per channel). Its principle is shown on figure 3. The current Ipulse is switched from the right branch of the differential stage to the left one to produce a positive current pulse δI entering the CSA. Respectively switching Ipulse from the left branch to the right one provides a negative current pulse. The pulse level of this built-in test module can be chosen by writing into a 8 bits D2A converter. This pulse is used to test one channel selected by means of the test shift register (Fig. 2). In a same way, the channel to be read is defined in the readout register. All these registers are addressed by means of the JTAG controller. The test pulse D2A converter and

those used to set the biasing currents of the analog modules are also chained together as a scan register.

The capability to remotely control the circuit biasing and to easily test it by means of the standard industrial JTAG protocol is a new feature among the circuits dedicated to similar applications [4].

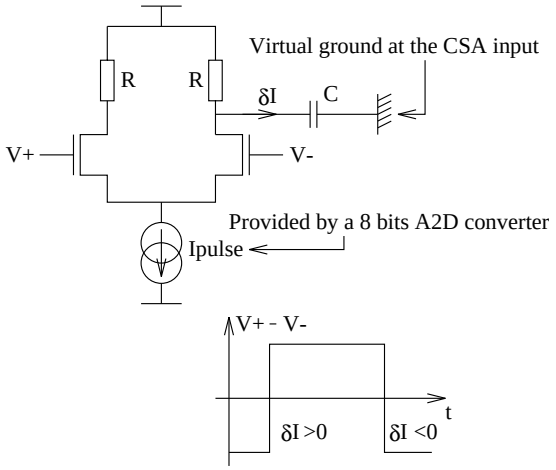

Fig. 3 : Current pulse generator principle

In order to be used as a test module, the current pulse generator has to be characterized before. Its calibration was performed by injecting successive external amplitude known current pulses onto a selected channel, then by measuring the corresponding analog signals at the channel output and finally by comparing these results with these obtained with the internal generator.

The same technique can be used to calibrate the generator of each channel. But this would be very tedious and time consuming. So to characterize the current pulse channel to channel deviation, the power supply current deviation were measured while successively setting the same current Ipulse in each generator. A deviation smaller than 1% was obtained. This could be expected since this deviation is mainly due to mismatching between the current mirrors used to provide Ipulse. The other sources of deviation come from mismatching between the resistances and the capacitances. Nevertheless we can expect a mismatching of the same order than the one for the mirrors. So the current pulse channel to channel deviation is 1 or 2 %, which is sufficiently accurate to allow the use of this module to test the amplifying channel. Still one must note that, during the high energy physics experiment, this pulse generator will be mainly used to check if the channel is out of order so as to bypass the circuit if necessary.

In the normal mode, the analog readout of the 128 channels is done sequentially, started by a token provided by the previous chip. In order to disconnect a chip out of order, the readout register is bypassed by connecting the token input to the token output. On reset, the token is bypassed and a JTAG instruction has to be sent to enable the readout.

IV.- First test results

By means of a HP82000 IC evaluation system for generating/acquiring digital signals and a home data acquisition system for acquiring analog signals, a test set-up were developed. All the functional blocks of ALICE128C have been tested with success. The specifications of table 1 are all satisfied.

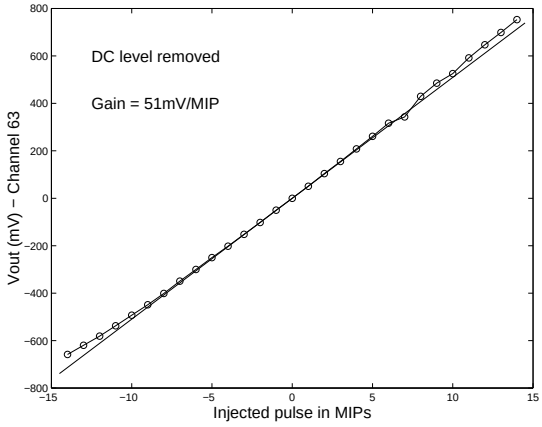

Fig. 4 : Transfer characteristic of channel 63

After the electrical characterization of the internal current pulse generators, the transfer characteristic of an arbitrary channel, $V_{OUT} = f(Q_{MIPS})$, has been measured. Here, we chose the sixty third channel. Setting all the biasing currents at their nominal values (values obtained by simulation), a typical readout cycle (internal current pulse injection + hold signal after 1.5µs + readout) is performed every 10ms with a readout rate of 10MHz. At each new readout cycle, the injected current pulse level is increased by 1 MIP (22000e$^-$). Figure 4 shows the transfer characteristic. A linear regression performed on the full input range gives a gain of 51mV/MIP, slightly higher than the specification of table 1. The actual transfer characteristic has to be shifted by $V_{OUT}0 = 288$mV since the output DC level, named also base line, has been removed for convenience.

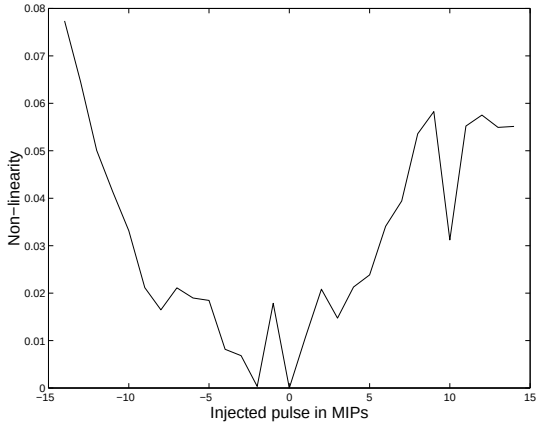

Fig. 5 : Transfer characteristic non-linearity

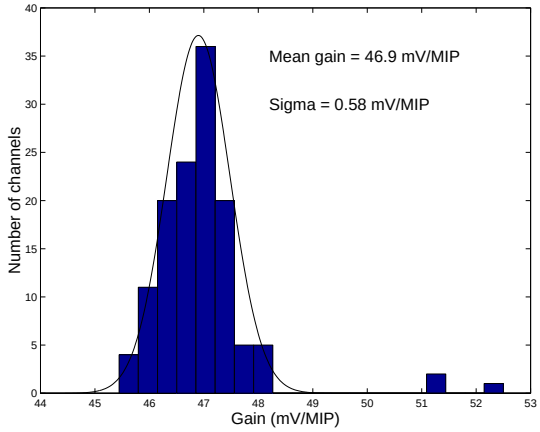

Fig. 6 : Gain distribution

The deviation from the fitted linear curve is presented on figure 4. As expected by simulation [3], the non-linearity is below 2% in the range of ± 5MIPs and below 8% in the full range.

Using the same method, but setting together 32 channels (the internal pulse is injected at the same time into 32 adjacent channels), the gain and the base line of each channel were measured. Figure 6 shows the gain distribution. It can be seen as a gaussian distribution with a mean value of 46.9mV/MIP and a standard deviation of σ = 0.58mV/MIP. Note that the mean gain is very close to the simulated value which was equal to 47.9mV/MIP [3]. The base line is distributed more randomly with a mean value of 295mV and a standard deviation of 4.9mV.

V.- Conclusion

ALICE128C, a new ASIC for radiation detection front ends has been presented. Assuming typical conditions of use, its mean power dissipation was drastically reduced to 340µW/channel, by switching off all the analog buffers when they are not used. Particular attention was paid to eliminate the noise induced by this on/off switching mechanism. Great effort has been carried out to enable remote circuit test and control through JTAG, during the span of the high energy particle experiment. This is mandatory because the circuit is situated into the heart of the spectrometer which is not a readily accessible place. Finally, test results are very close to the expected electrical characteristics, so the circuit should be used in its first and actual version inside the ALICE spectrometer.

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