ELECTRICAL CHARACTERIZATION OF ALICE128C : A LOW-POWER CMOS ASIC FOR THE READOUT OF SILICON STRIP DETECTORS

M. Ayachi, J.D. Berst, J.P. Blondé, G. Clauss, C. Colledani, G. Deptuch, W. Dulinski, Y. Hu, L. Hébrard, W. Kucewicz
Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux
LEPSI - IN2P3/CNRS - ULP
23, rue du Loess - BP 20, 67037 Strasbourg Cedex 02 - France
Email : hebrard@lepsi.in2p3.fr

J.R. Lutz and al. - ALICE/STAR group from IReS (Strasbourg - France)
and
S. Bouvier and al. - ALICE/STAR group from Subatech (Nantes - France)

ABSTRACT

ALICE128C is a new low-power CMOS ASIC dedicated to the readout of Silicon Strip Detectors (SSD) for the ALICE [1] and STAR [10] experiments. The architecture of the circuit and the main simulation results have been presented already [2]. This paper presents the electrical characterization results according to the procedure used to test the circuit. All functional blocks were tested with success, and all electrical specifications are satisfied. Especially, in the case of a 10MHz readout rate with a mean readout cycle every 1ms, i.e. for typical conditions of use, the mean power dissipated per channel is kept very low, around 340µW/channel. Specific functionalities were added in ALICE128C to control, to test and to characterize the circuit [2][3]. They have been used extensively during the characterization and they will provide efficient testing capabilities after mass production and during the ALICE and STAR experiments.

I. INTRODUCTION

ALICE128C is a 128 channels chip designed with the AMS1.2µm CMOS technology (die size 6mm x 8.5mm) [2]. Each channel amplifies, shapes and stores as a voltage signal onto the capacitance C_{HOLD} the charge deposited on a strip of the detector. This storage is triggered by the external HOLD logic signal which arises τ_s seconds after the radiation event. The shaping time (τ_s) is adjustable from 1.4µs to 2µs. An analog multiplexer allows a sequential readout of the data at a rate up to 10MHz through a tristate output buffer shared by the 128 channels. The output buffer has been designed to drive an external link with a 100Ω characteristic impedance in parallel with a capacitance up to 20pF. The tristate property of the output buffer allows a daisy chain of several ALICE128C chips connected onto the same external link. A slow control mechanism compatible with the « JTAG IEEE1149.1 » standard [4] has been added to accurately bias the different analog blocks and to tune the shaping time. It also controls an internal test pulse generator which provides a variable current pulse emulating a deposited charge up to ±11MIPs (MIP : Minimum Ionizing Particle; 1MIP ≈ 25000 electrons).
The next section develops the specific testing functionalities added to ALICE128C. Then, a short description of the test set-up used to characterize the circuit is given. Section IV describes the procedure used to test the circuit and gives the main results of characterization. Finally, section V concludes the paper.

II. CIRCUIT TESTABILITY

ALICE128C is mainly an analog circuit since the digital part includes only the JTAG module and the readout controller. Testing efficiently such a circuit is a challenge. So one of our efforts in designing ALICE128C was to add specific testability features into the chip. These features address three goals : the circuit electrical characterization, the circuit test after mass production and the on-site circuit test during the experiment.
After prototyping, the circuit has to be electrically characterized. In particular, the amplifying channel gain is measured by injecting a calibrated current pulse at the input. But it would be very tedious, time consuming and error prone to connect every 128 channels, or successively each channel, of a prototype to an external charge injection system in order to measure the corresponding gains. So, in front of each channel, a current pulse generator has been integrated (figure 1). It switches a current, I_{pulse}, from one branch of a differential stage to the other one, to produce a

step voltage across a double polysilicon capacitance C, connected to the input of the preamplifier [3]. Such a system emulates a charge Q, deposited on the detector by a radiative particle which value is $Q=I_{pulse}.R.C$. By writing into a 8 bits current D2A converter, I_{pulse} is then varied to set the test pulse level.

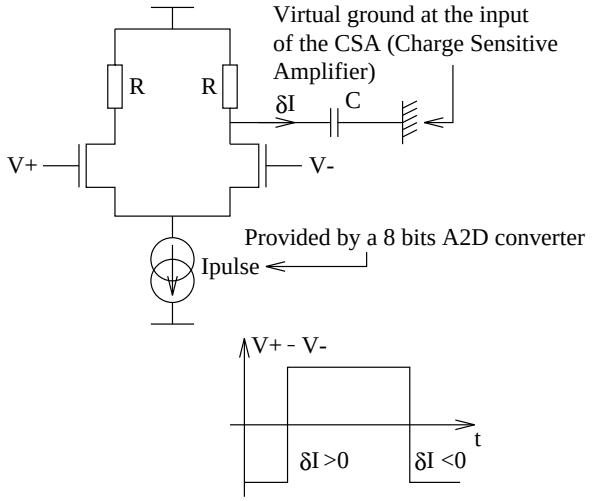

Fig. 1 : Current pulse generator

The channels where the pulse has to be injected are selected through a shift register. At the output, depending on the kind of test to perform, it is possible to read sequentially all the signals stored on the C_{HOLD} capacitances (normal readout cycle) or to select one particular channel through the output shift register. In this later case, the external HOLD logic signal is set to 0 and we see through the corresponding channel from the input to the output. This allows for example to visualize the shape of the signal at the output of the shaper in order to measure/set the shaping time. Of course, to be used for characterization, the pulse generators have to be calibrated. We will see how it is done in section IV. All the different testing configurations and the pulse level, thus all the registers, are addressed by means of the JTAG controller.

After mass production, the circuits are sorted in order to throw out the possible wrong products. This sorting is based on simple trials which involve the measurement of some power supply DC currents for example. But more complicated measurements can be considered. In this case, one can take advantage of the specific testing functionalities of ALICE128C. A channel out of order can be easily detected by using the internal pulse generator. Of course, these kinds of test have to be performed before bonding the silicon strip detector to the chip, and the use of TAB bonding [5] can also become an advantage.

During the long range experiment (around 10 years), it could be essential to check periodically the functionality of the circuit, to adjust the analog parameters in case of harmful deviations, and also to disconnect an ill circuit from the readout daisy chain. The specific testing and control functionalities of ALICE128C are mainly added for such a purpose. Furthermore, these controls and tests must be done remotely and without requiring a lot of links since the circuit is situated into the heart of the spectrometer. Thus, in order to minimize the number of interconnections, all the chips are connected serially according to the JTAG.IEEE1149.1 protocol [4]. In the normal mode, the analog readout of the 128 channels is done sequentially, activated by a token from the previous chip. In order to disconnect a chip out of order, the readout register is bypassed by connecting the token input to the token output. Note that on reset, the token is bypassed and a JTAG instruction has to be sent to enable the readout.

III. TEST SET-UP

The test set-up used to characterize ALICE128C is presented on figure 2.

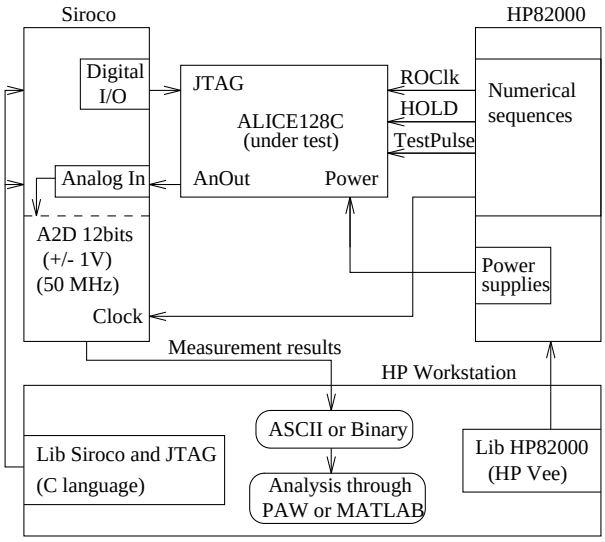

Fig. 2 : Test set-up

On one side, a HP82000 IC evaluation system is used to generate specific digital stimuli as the Read-Out-Clock, the external HOLD signal, the Test Pulse Request and some configuration signals (Reset,...). On the other side, a home data generation/acquisition system (a Siroco) [6], dedicated to Strip Detectors Read-Out Systems, is used to send the JTAG sequences and to acquire the analog output signal provided by ALICE128C. This hardware testing system is controlled by means of a unix workstation with specific softwares written in C to drive the Siroco and in HP Vee to drive the HP82000. Finally, the digital stimuli and the resulting analog signals are stored in ASCII or Binary files which can be analysed

through PAW [7] or MATLAB [8]. Thanks to this set-up the different testing configurations can be selected very fast and many electrical measurements were performed to characterize ALICE128C.

IV. TEST RESULTS

IV.1 Internal Pulse Generator Calibration

Prior to stimulating the circuit by means of the internal pulse generator, one must calibrate the generator. The ALICE128C prototype was mounted on a specific PCB with an external current pulse injection system connected on channel 39. This external generator is made up of a capacitance which value is accurately known, a voltage pulse generator, and a 50Ω resistance in order to adapt the voltage generator output impedance. By tuning the voltage amplitude, the injected charge can be varied accurately. In order to calibrate the internal pulse generator, the transfer characteristic $V_{out} = f(Q_{MIPs})$ of channel 39 obtained by means of the external injection should be compared with the characteristic obtained using the internal injection. Due to parasitics added by the external injection system, this former characteristic has to be measured after disconnecting the external system. Nevertheless, this is mechanically too complicated and the transfer characteristic of channel 39, obtained with external injection, was compared with the characteristic obtained by internal injection on another channel, here channel 63. As we will see later, this approximation is good since the channel to channel gain dispersion is small, less than 1%.

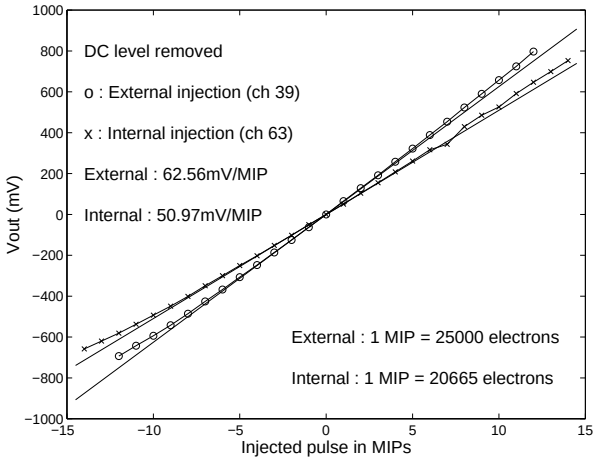

Fig. 3 : Pulse generator calibration

The measurements performed on channels 39 and 63 are shown on figure 3. For the external injection system, the MIP is taken equal to 25000 electrons. In this case, the amplifying channel begins to saturate over +12 MIPs, so the amplitude of the curve was restricted to ± 12 MIPs. A linear fitting performed on the full input range gives a gain of 62.56mV/MIP which is also the actual gain of channel 63 ! By means of the 8 bits D2A current converter, the internal generator is assumed to be able to provide ±14 MIPs. In this case, the linear fitting of the transfer characteristic gives a measured gain of 50.97mV/MIP. Assuming that the actual gain is 62.56mV/MIP, this means that, here, one MIP corresponds to 20368 electrons, or that the internal generator actual amplitude is of ±11.4 MIPs (1MIP = 25000 electrons). *From now, 1 MIP will be assumed equal to 25000 electrons !*

This is a good calibration procedure only if the 8 bits D2A I_{pluse} current converter is linear. In order to verify this characteristic, the power supply current was measured as a function of the converter digital input when changing only I_{pulse}. The curve obtained (not shown) is linear with a correlation factor of 0.99 !

IV.2 Amplifying channel gain and linearity

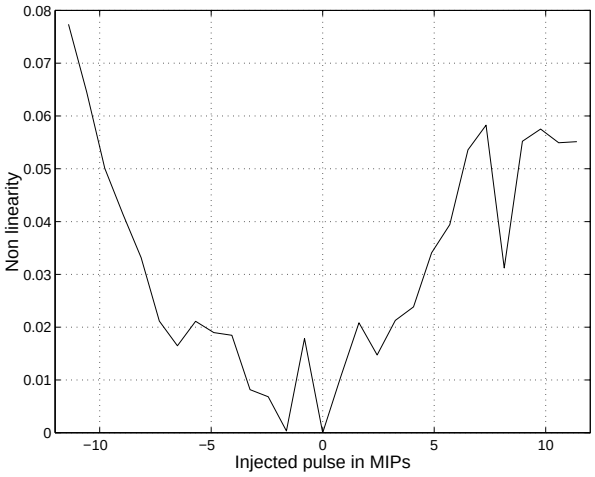

Fig. 4 : Transfer characteristic non linearity

Setting all the biasing currents at their nominal values (values obtained by simulation), the transfer characteristic of channel 63 was measured by performing a typical readout cycle (internal current pulse injection + HOLD signal after 1.5µs + readout) every 10ms with a readout rate of 10MHz. In order To remove harmful noise, the measurement is performed thousand times and the average value is retained. At each new readout cycle, the injected current pulse level is increased by 1 MIP. This measurement procedure provides the transfer characteristic of figure 3. The actual transfer characteristic has to be shifted by the output DC level, here 288mV since the base line has been removed for convenience. As mentioned before, the linear regression performed on the full input range gives a gain of 62.56mV/MIP which is

slightly higher than the gain required by the specifications [2] (50mV/22000.e^- = 56.8mV/MIP).
The deviation from the fitted linear curve is presented on figure 4. It was calculated as the ratio of the difference between the measured and the fitted values at the corresponding point with the fitted value. As expected from simulation [2], the non linearity is lower than 2% in the range of ±4 MIPs and 8% over the full range.

IV.3 Channel to channel gain dispersion

Using the same measurement procedure, but injecting the internal pulse at the same time into 32 adjacent channels, the gain and the base line of each channel were measured. The choice of injecting simultaneously on 32 channels was taken to save time during the test (each measurement is performed thousand times and its average value is retained as the right measurement !). Figures 5 and 7 show the resulting distributions.

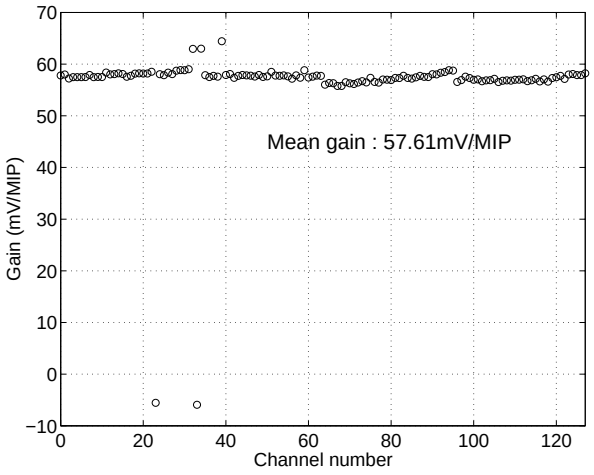

Fig. 5 : Channel to channel gain

Two channels, channels 23 and 33, are out of order. This is certainly due to ESDs (ElectroStatic Discharge) which have destroyed the gate oxide at the input of the charge sensitive amplifier (CSA) during the bonding of the chip on the test PCB. Note that the channel input nodes have no protection diodes since noise has to be kept at a minimum level on these nodes. The gains of channels 32 and 34 are slightly higher than the mean gain. This must be again due to damage occurred during the bonding. Furthermore, the gain of channel 39 is higher than the other gains because of the parasitics induced by the external injection system connected to this channel.
By looking at the global channel to channel gain distribution (figure 5), a cluster phenomenon is clearly observed. The gains are clustered by sets of 32 corresponding to the 32 channels where the pulse is injected. On the other hand, the gain seems to increase inside a cluster from the first to the thirty second channel ! An accurate analysis has to be carried out in order to explain in details this phenomenon. Nevertheless it is due to small resistive voltage drops occurring on the Vss power line and resulting in a discrepancy between the reference current provided by the internal 8 bits D2A current converter and the I_{pulse} copy of this current into each current pulse generator.
Since these generators are equally spaced in front of the chip, the small voltage drops are linearly distributed over the 32 channels, resulting in the observed cluster phenomenon.
The mean amplifying gain, 57.61mV/MIP, is reduced in comparison to the gain measured on channel 63, 62.56mV/MIP, when only one pulse is injected (figure 3). This comes again from the same cause acting globally on the 32 current pulse generators and resulting in a decrease of the mean gain.

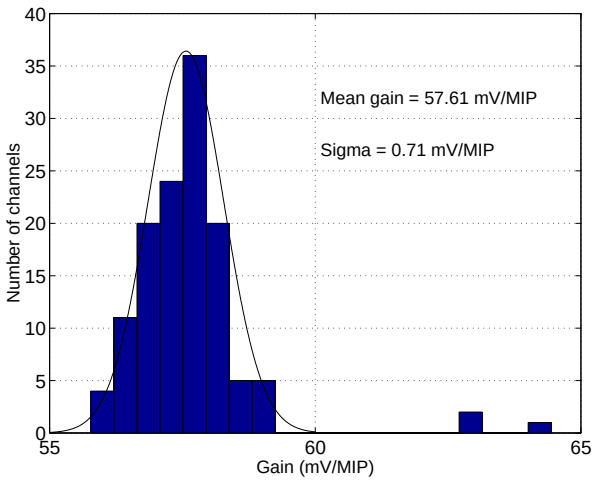

Fig. 6 : Gain distribution

Figure 5 shows the gain distribution. It can be seen as a gaussian distribution with a 57.61mV/MIP mean value and a standard deviation of σ=0.71mV/MIP. The two channels out of order were removed and channels 23, 33 and 39 were not considered in calculating the distribution gaussian fitting. The channel to channel gain dispersion σ, is then of the order of 1.2%. On one hand, this dispersion comes from the dispersion of the integrated component electrical characteristics. On the other hand, it comes from the clustering phenomenon described previously. One can expect that the main source of dispersion is due to the clusters. So the 1.2% dispersion can be seen as a pessimistic value.
This result shows that our assumption on gain dispersion in performing the pulse generator calibration was justified.

IV.4 Base line distribution

The base line is distributed randomly with a mean value of 296mV and a 7mV standard deviation, i.e. only 11.2% of one MIP as base line dispersion. Note that the base line is not disturbed by the cluster phenomenon since it is determined for 0MIP injected .

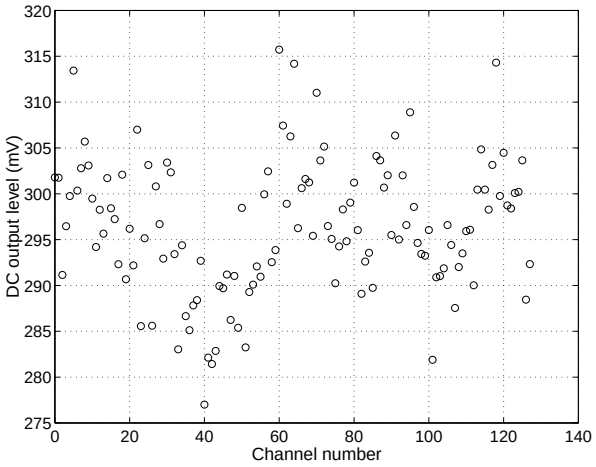

Fig. 7 : Channel to channel DC output level

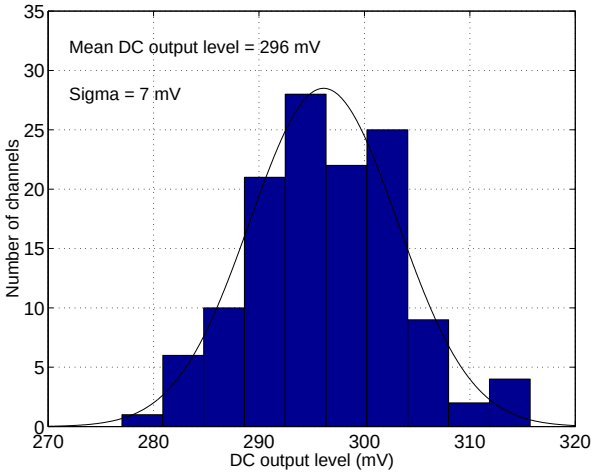

Fig. 8 : DC output level distribution

IV.5 Noise

For such front end amplifying system, the Equivalent Noise Charge (ENC) at the input is proportional to the detector capacitance. So the ENC was measured with the SSD bonded to the chip [9]. A value of 300 electrons was obtained for a detector capacitance around 5pF. This is in the range of the specifications (<400 electrons) [1][2].

IV.6 Power consumption

Until now all the measurements were carried out after biasing the circuit by the nominal currents obtained by simulation. So, for a 10MHz readout rate, the mean power consumption per channel is given by [2] :

$$\langle P \rangle = 328 + 10.53 \times T_C$$

where T_C, the period between two readout cycles is expressed in milliseconds and <P> is expressed in microwatts. For a typical readout cycle every 1 ms, the mean power consumption per channel is then kept to the very low value of 340 µW/channel.

V. CONCLUSION

This paper has presented the electrical characterization of ALICE128C. Thanks to the specific testability features added to ALICE128C, the characterization procedure was made easier and a lot of measurements possible. The main results are given and show that all required electrical specifications are satisfied. ALICE128C has been mounted with success into a global detecting prototype system and is expected to be used for the ALICE and STAR experiments [9].

REFERENCES

[1] « ALICE : Technical Proposal for A Large Ion Collider Experiment at the CERN LHC », CERN/LHCC/95-71, LHCC/P3, December 1995

[2] L. Hébrard and al., « ALICE128C : A CMOS Full Custom ASIC for the Readout of Silicon Strip Detectors in the ALICE Experiment », Proc. of the third workshop on electronics for LHC experiments, Imperial College, London, September 22-26, 1997, pp. 173-177

[3] L. Hébrard, J.P. Blondé, C. Colledani, G. Clauss, « Design and Test of a CMOS Low-Power Mixed-Analog/Digital ASIC for Radiation Detector Readout Front Ends », Proc. of the 11th Annual IEEE International ASIC Conference, ASIC'98, Rochester, New York, September 13-16, 1998, pp.

[4] H. Bleeker, P. Van den Eijnden and F. De Jong, « BOUNDARY SCAN TEST - A Practical Approach », Kluwer Academic Publishers, 1993

[5] S. Bouvier and al., « TAB packaging technology for the Si-strip front end detector assembly », Proc. Of the 4th workshop on electronics for LHC experiments, Rome, September 21-25, 1998

[6] G. Clauss, W. Dulinski, A. Lounis, « Strip Detectors Read-Out System user's guide », LEPSI - IReS (CRN), CNRS-IN2P3/ULP, Internal Note CRN 96-33, 1996

[7] R. Brun, O. Couet, C. Vandoni, P. Zanarini, « PAW - Physics Analysis Workstation », CERN Computer Center, Q121/CERN.

[8] « MATLAB - Version 5 », User's guides, The MATH WORKS Inc., 1996

[9] J.R. Lutz and al., « Detector and Front End Electronics for ALICE and STAR Si-strips layers », Proc. Of the 4th workshop on electronics for LHC experiments, Rome, September 21-25, 1998

[10] Star Technical Proposal, « Proposal for a Silicon Strip Detector for STAR (SSD) », SUBATECH (Nantes), IReS (Strasbourg), LEPSI (Strasbourg), Physics Department of Wayne State University (Detroit - USA), 1998