ALICE128C : A CMOS Full Custom ASIC for the Readout of Silicon Strip Detectors in the ALICE Experiment

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Abstract

The mixed-signal integrated circuit described in this paper was designed to fulfill the requirements of the readout electronics for the Silicon Strip Detectors (SSD) of the ALICE experiment. It is a 128 *channels chip designed with the AMS*1.2μm *CMOS technology. Each channel amplifies, shapes and stores as a voltage signal the charge deposited on a strip of the detector. The shaping time is adjustable from* 1.4μs *to* 1.8μs. *An analog multiplexer allows a sequential readout of the data at* 10MHz *rate through an output buffer shared by the* 128 *channels. The output buffer has been designed to drive an external link with a* 100Ω *characteristic impedance in parallel with a capacitance up to* 20pF. *A slow control mechanism compatible with the "JTAG IEEE1149.1-1990" standard is used to bias accurately the different analog blocks and to control the shaping time and a test pulse generator. The pulse generator provides a variable current pulse which emulates a deposited charge up to* $\pm 15MIPs$. *Our efforts were focused on reducing the power consumption to decrease it to a mean value around* 340$\mu W/Channel$. *The circuit has been sent to manufacturing at the end of June and its return is foreseen at the end of September.*

1 Introduction

The approximately 2.6 million channels of the Iternal Tracking System (ITS) silicon strip layers must dissipate less than $3kW$ in order to maintain an acceptable size and weight of the cooling system [1]. As a consequence, the mean power consumption of the front end electronics must be below $1mW/Channel$. Such a specification would be easy to fulfill if the range of the input signal were small and the readout rate low. Unfortunately, the large energy deposition of slow particules expected in the ALICE experiment requires the front-end circuit to accept input signals up to $\pm 13MIPs$ ($1MIP = 22000e^-$ deposited), and the huge number of channels imposes a fast serial readout rate since parallel readout has to be rejected to minimize the number of links between the front-end and the end-caps of the ITS.

Name	Specification
Input range	$\pm 13MIPs$
ENC	$\leq 400e^-$
Readout rate	$10MHz$
Power	$\leq 1mW/Channel$
Gain	$\simeq 50mV/MIP$
Shaping time	$1.4\mu s \leq t_s \leq 1.8\mu s$
Test pulse	$\pm 15MIPs$

Table 1 : ALICE128C main specifications

The relevant specifications the circuit has to fulfill are summarized in table 1. The next section gives an overview of the architecture used to implement ALICE128C and outlines some new design choices we made to satisfy the most stringent requirements of table 1, especially in respect to the power consumption issue. The third section presents the physical implementation of ALICE128C and we conclude

by showing some relevant simulation results obtained taking into account all the parasitics due to layout.

2 Circuit description

Figure 1 gives the block diagram of ALICE128C. Each block is now briefly described.

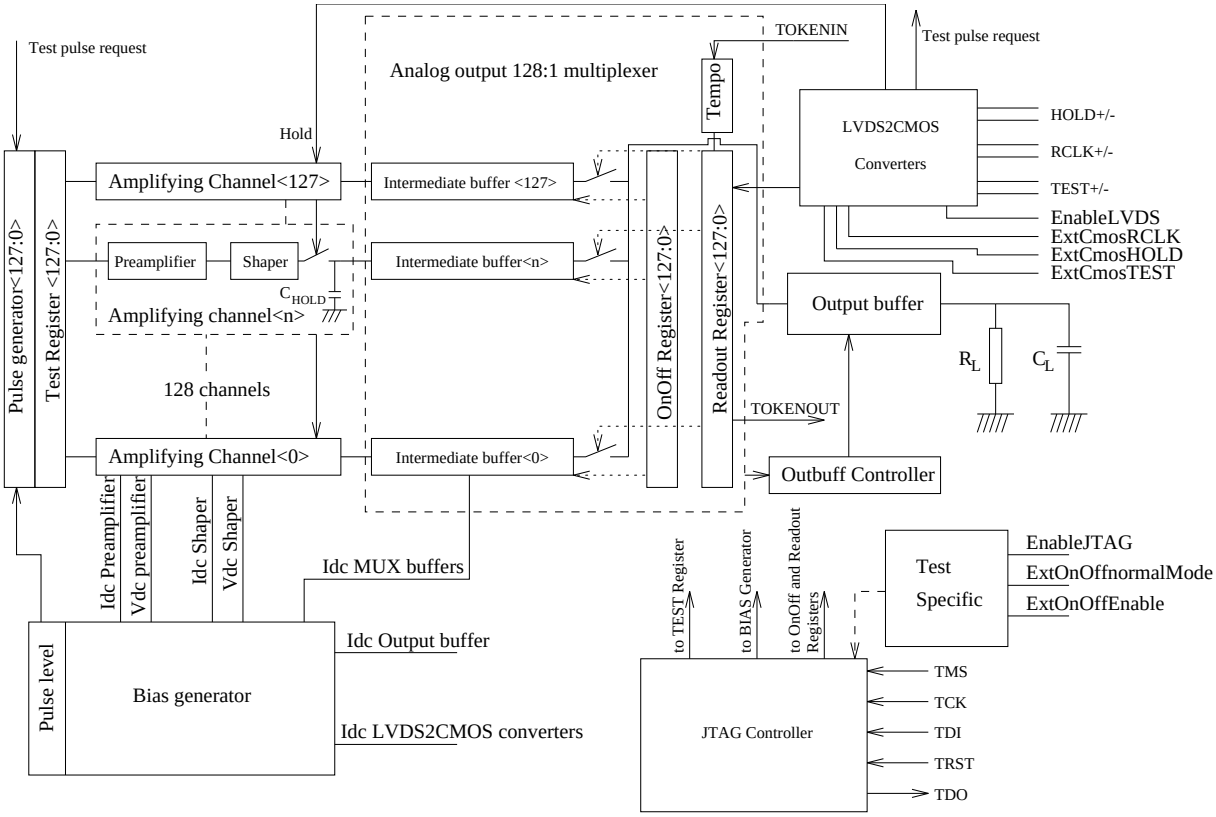

Figure 1 : Block diagram of ALICE128C

2.1 Amplifying channel

The amplifying channel amplifies, shapes and stores as a voltage signal in C_{HOLD} the charge deposited on the corresponding detector strip. The charge preamplifier and the shaper are similar to the ones designed for DELPHI32 [2], but modified to decrease their power consumption. The preamplifier biasing current was reduced to $100\mu A$ in order to limit its power dissipation to $200\mu W$. By the same way, the PMOS input transistor of the high open loop gain folded cascode amplifier used in the shaper was connected between the ground and $V_{SS} = -2V$, and biased with $30\mu A$ in order to limit the global dissipation of the shaper to $90\mu W$. This leads to an acceptable increase of the Equivalent Noise Charge (ENC) at the input where $ENC = 280e^-$ for $10pF$ of detector capacitance and $1.4\mu s$ of shaping time. The gain of the amplifying channel is $48mV/MIP$ and represents the gain of the whole chain since no loss of gain occures through the output multiplexer and the output buffer.

2.2 Analog output multiplexer

The external "TOKENIN" logic signal along with the "RCLK" signal (Read Clock) trigger the serial readout cycle.
The signal stored on C_{HOLD} enters an intermediate buffer aimed to drive the high parasitic capacitance ($\simeq 1pF$) of the output 128:1 multiplexer. Because of the high input signal range ($\pm 13MIPs$) and the high readout rate ($10MHz$), this buffer has to handle a large signal magnitude up to $\pm 1V$, with a good linearity and a settling time less than $30ns$. These specifications along with the high capacitive load require a buffer which dissipates around $7500\mu W$. Obviously, this value is too high to keep all the intermediate buffers on at any time. So, the buffers are switched on only during the readout of their corresponding channel. More accurately, in order to reduce the noise induced by the switching on/off mechanism of the surrounding buffers, the buffers ("n-1" and "n+1") previous and next to the channel being read ("n") are also on while the buffer "n-2"

is switched off and the buffer "n+2" switched on. So, during the readout cycle, only four intermediate buffers are dissipating power. Figure 2 explains the mechanism.

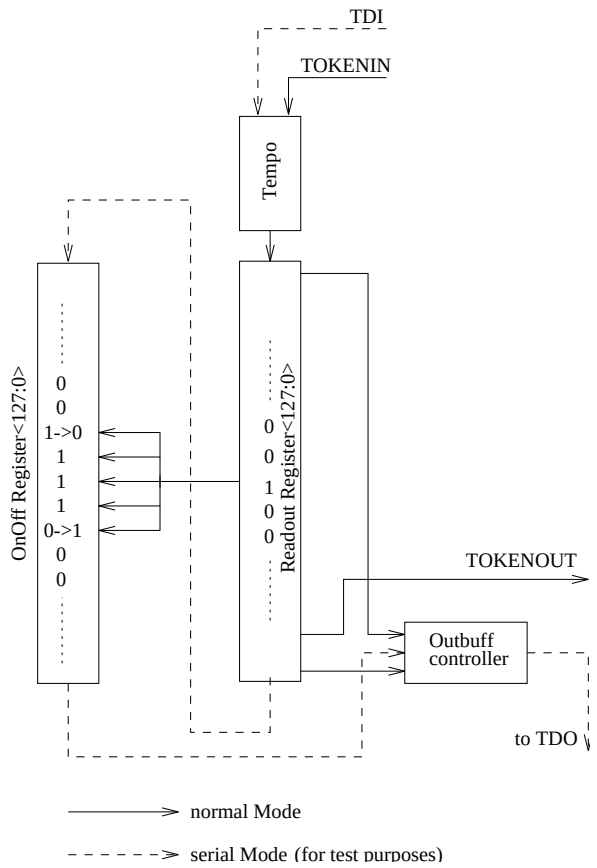

Figure 2 : On/Off switching mechanism

The first memory cell, named "Tempo", delays by one clock pulse the "TOKENIN" signal in order to switch on the first two intermediate buffers before begining the readout. A "TOKENOUT" signal is picked up just before the last channel in order to allow a daisy chaining of several ALICE128C circuits without requiring an extra clock pulse between two consecutive chips. Only an extra clock pulse after the arrival of the "TOKENIN" is required for the first chip of the chain, and an another extra clock pulse is required after reading the last channel of the last chip in order to switch off the last chip's buffers.

2.3 Output buffer

The output buffer is shared by the 128 channels and can drive an external link with a 100Ω characteristic impedance in parallel with a capacitance up to $20pF$. It is a unity gain, single ended buffer designed to provide the analog output signal in $30ns$ to $50ns$ in order to sustain a $10MHz$ readout rate. It can be switched on or off. When on, it dissipates $34mW$. When off, no power is dissipated and the output of the buffer is in a high impedance state. The "Outbuff Controller" (figure 1 or 2) switches on the output buffer during the readout cycle of the chip (i.e. 128 channels). With $R_L = 100\Omega$ and $C_L = 20pF$, the on/off switching settles in less than $50ns$ which allows a daisy chaining of several ALICE128C circuits.

2.4 Bias generator and Test pulse level generator

The bias generator provides five dc currents to bias accurately all the analog modules, and two dc voltages to tune the PMOS feedback resistors of the preamplifier and the shaper. The dc currents come from 8 bit current-scaling DACs. Since the dc voltages bias high impedance MOS gates, they are obtained through similar current DACs which feed a $9.8K\Omega$ polysilicon resistor.
The negative and positive levels of the test pulse are chosen by setting the current delivered by the "test pulse level generator". A linear relation exists between the value of this current and the pulse level in MIPs. This current is also provided by a 8 bit current DAC and allows a pulse level in the range of $\pm 15MIPs$.
The setting of all these DACs is carried out through the "JTAG controller".

2.5 Pulse generator and Test register

The "pulse generator" switches the current provided by the "test pulse level generator" from one branch of a differential stage to the other branch. This switching is performed by changing the external "LVDS TEST" signal. A positive front edge triggers a positive test pulse while a negative front edge triggers a negative test pulse. Using the JTAG controller, one can write in the 128 bit "test register" to select the channels where to inject the test pulse. A logical 1 enables the channel.

2.6 LVDS2CMOS converter

Three logic signals have been implemented with a LVDS (Low Voltage Differential Signal) level [4] to reduce the switching noise induced into the links between the front-ends and the end-caps. These signals are the "Read clock" signal, the "HOLD" signal and the "TEST" signal. The "LVDS2CMOS converters" converts the LVDS level ($\pm 100mV$ around a $1.2V$ dc level) into the internal $\pm 2V$ CMOS level. They have been designed to work at a frequency up to $30MHz$.

2.7 JTAG controller

The JTAG controller allows to select the functional mode of ALICE128C (bias setting, TOKENIN bypass, normal mode,...). It is also used for test purpose (test pulse level setting, selection of channels where to inject the test pulse, functional test,...). It is compatible with the JTAG IEEE1149.1-1990 standard [4] in order to ease the interfacing of ALICE128C.

3 Physical implementation

Figure 3 shows the layout of ALICE128C. The circuit contains around 70000 transistors, is $8640\mu m$ long and $6080\mu m$ wide. Its width matches the width of the silicon strip detectors. The pitch of the pads to connect the detector is $44\mu m$. Two sets of 128 pads, each set dispatched on two columns, have been implemented in order to ease the bonding. On the back side of the circuit, 43 pads are provided. Some of them were especially wanted by designers for test purposes, the others are intented for normal use of the circuit and allow the communication between the front-end electronics and the end-caps.

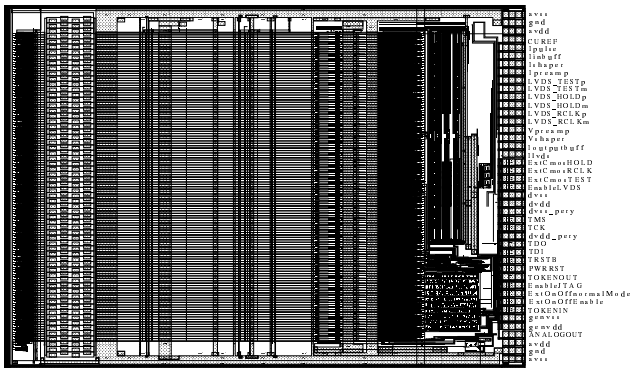

Figure 3 : Physical implementation of ALICE128C

4 Simulation results

4.1 Power budget

Table 2 summarizes the simulated power consumption of every analog module. Implemented in static CMOS logic, the other modules doesn't dissipate a significant power. On the basis of these data, we can perform the circuit power budget for every functional mode.

Analog Module	Power dissipated
Preamplifier	$230\mu W$
Shaper	$98\mu W$
Intermediate buffer on	$7400\mu W$
Intermediate buffer off	$0\mu W$
Output buffer on	$33800\mu W$
Output buffer off	$0\mu W$
LVDS2CMOS	$300\mu W$
Pulse generator (I_{max})	$2048\mu W/channel$

Table 2 : Analog blocks power dissipation

1. **Power dissipated per channel during acquisition** : During acquisition (no readout), the intermediate buffers and the output buffer are switched off and dissipate no power. The sole dissipation takes place into the preamplifier and the shaper. So, the power dissipated per channel is

$$P(\text{no readout}) = 230 + 98 = 328\mu W/channel$$

2. **Power dissipated per channel during the readout** : During the readout, four intermediate buffers and the output buffer are switched on. The power dissipated per channel becomes expressed by

$$\begin{aligned} P(\text{readout}) &= 230 + 98 + \frac{4 \times 7400}{128} + \frac{33800}{128} \\ &= 823\mu W/channel \end{aligned}$$

3. **Mean power dissipation per channel assuming a readout cycle every 1ms** : The ALICE experiment should require a typical readout cycle mean rate of one readout every $1ms$. Assuming such a rate, the ALICE128C circuit dissipates $823\mu W$ during $128 \times 100ns$ every $1ms$ added to $328\mu W$ dissipated constantly. The mean power dissipation for a typical experiment is then calculated as :

$$\begin{aligned} < P > &= \frac{823 \times 100.10^{-9} \times 128}{10^{-3}} + 328 \\ &\simeq 339\mu W/channel \end{aligned}$$

The mean power dissipation was drastically reduced to $340\mu W/channel$ and is below the $1mW/channel$ even during the readout cycle as requested in table 1. Note that we have neglected in our calculations the consumption of the three LVDS2CMOS converters. Taking them into account would increase the power consumption by $3 \times 300/128 = 7\mu W/channel$.

4 Simulation results

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4.2 Gain and linearity

The open loop gain of the intermediate buffers and the output buffer was chosen above $60dB$. As a consequence, the contribution of the analog output 128:1 multiplexer along with the output buffer to the gain and nonlinearity of the whole chain can be neglected. The only source of nonlinearity comes from the preamplifier/shaper set. Figure 4 shows the simulated transfert characteristic for a $1.4\mu s$ shaping time at the output of the shaper, the base line being substracted. A linear regression performed on the full input range gives a gain of $47.9mV/MIP$. The deviation from the fitted linear curve shows that the nonlinearity is below 1% in the range of $\pm 2MIPs$, below 3% in the range of $\pm 8MIPs$, and below 7.5% in the full range.

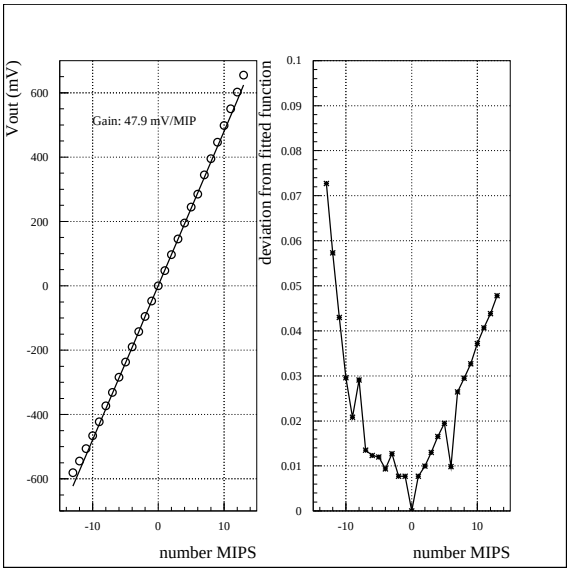

Figure 4 : Transfert characteristic and linearity

4.3 Readout cycle

Figure 5 shows a simulated typical readout cycle. To save computing time, the mixed signal simulation was carried out on a 12 channels chip. Nevertheless, in order to take into account all the parasitics due to layout, the 12 channels chip was obtained by keeping the four first channels, the four last channels and the four channels at the middle of the 128 channels chip, and connecting them vertically through metal lines identical to the ones existing in the 128 channels chip.

Channel "i" was excited by a deposited charge of $g_i \times 10MIPs$ where g_i is a weighting factor. For this post-simulation, $g_1 = 1$, $g_2 = 0.5$, $g_3 = 0$, $g_4 = 0.5$, $g_5 = 0.1$, $g_6 = 0.5$, $g_7 = 1.3$, $g_8 = 1$, $g_9 = 0.1$, $g_{10} = 0.5$, $g_{11} = 0.2$, and $g_{12} = 0$. The output signal is settled in less than $50ns$ for every channel. The settling time is a little bit longer for the first channel since the output buffer has to be switched on. The glitches seen at the begining and the end of the readout cycle are due to the on/off switching of the output buffer.

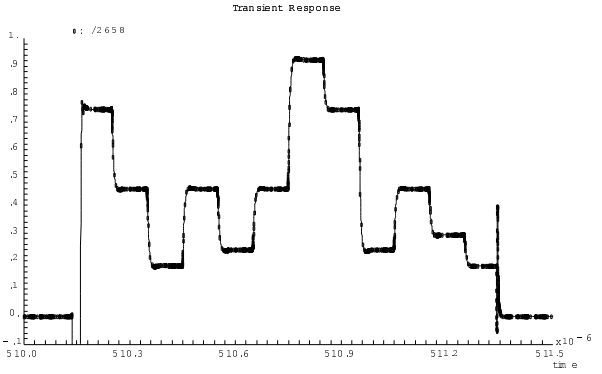

Figure 5 : Typical readout cycle

5 Conclusion

A CMOS mixed-signal integrated circuit aimed to the readout of Silicon Strip Detectors in the ITS of the ALICE experiment has been presented. The discussion was focused on the power consumption issue, the most stringent specification to satisfy. We outlined the new on/off switching mechanism we implemented to reduce drastically the mean power consumption to a value below $340\mu W/channel$. Some relevant simulation results were given and we foresee to test the circuit during october.

References

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4. Draft 1.3 IEEE P1596.3-1995, "Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)", Draft 1.3, November 27, 1995.