SSD documentation

SSD Module

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1 SSD Module design

The SSD consists in a barrel with a radius of 23 cm and is composed of 20 space frame carbon beams each supporting 16 detection modules. Each module (Figure 1, Figure 2) is composed of:

- a double sided silicon strip detector :
  - size : 42 mm * 75 mm,
  - 768 micro-strips per side of detector,
  - a pitch of 95µm,
  - 35mrad stereo angle between P and N strips.
- two hybrid circuits, each composed of:
  - one flexible circuit glued on a carbon fibre stiffener,
  - around 50 SMD components (resistors and capacitors),
  - 6 analogue readout chips : ALICE128C,
  - 1 multi-purpose control chip dedicated to temperature measurements, low and high voltage monitoring: COSTAR.

This leads to 320 detection modules for the whole barrel resulting in 491520 readout channels. Moreover minimising the amount of material and the cooling of the electronics are required. Bonding directly from the detector to the analogue readout chips is not possible due to the pitch mismatch (44µm for the ALICE128C).

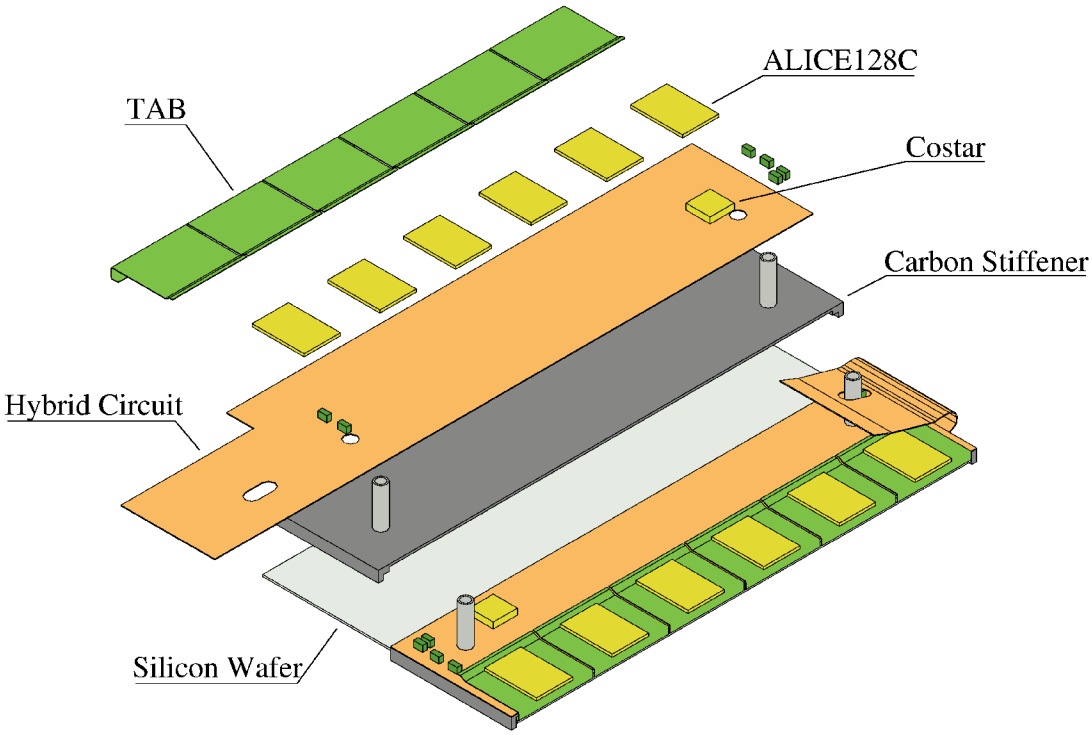

Figure 1 : Exploded view of a SSD module

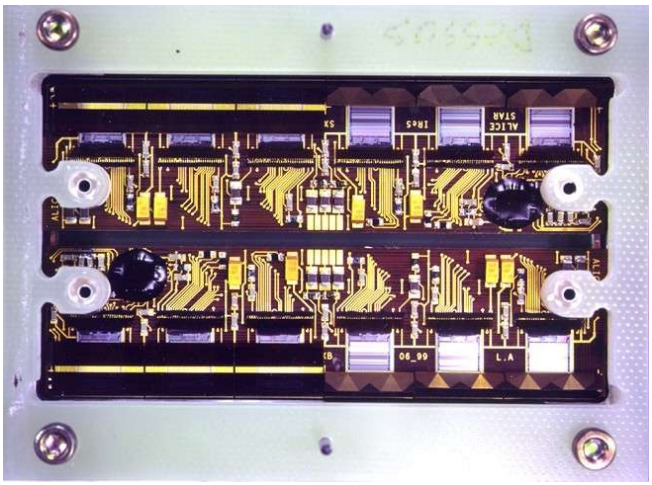

Figure 2 : Top view of a module prototype. The detector faces the backside of the module

2 Double Sided Silicon Strip Detector

The $75 \times 42 \times 0.3$ mm DS SSD includes 768 AC coupled strips on each side with a pitch of 95µm at a stereoscopic angle of 35 mrad. Guard and bias rings are all together ≤ 1 mm wide.
Production specifications have been described in the CCTP document. The main features relate to a unique operating voltage below 55 volts in between depletion voltage and breakdown voltage, a biasing current $i_{bias} \leq 2\mu A$, a guard ring leakage current $i_{guard} \leq 5\mu A$, and a number of dead coupling capacitors on each side below or equal to 10.
More than 440 detectors have been delivered by Eurisys and tested in our laboratory on a probe station in order to select 400 detector working inside the specifications. The test itself is done by mounting the bare detector in an epoxy frame (figure 3) which enables handling, identification, and connection to the test equipment for biasing by means of two bonds on each side. This frame and the related bonds are removed later before the module assembling step. The test measurements are transferred into the production data base.

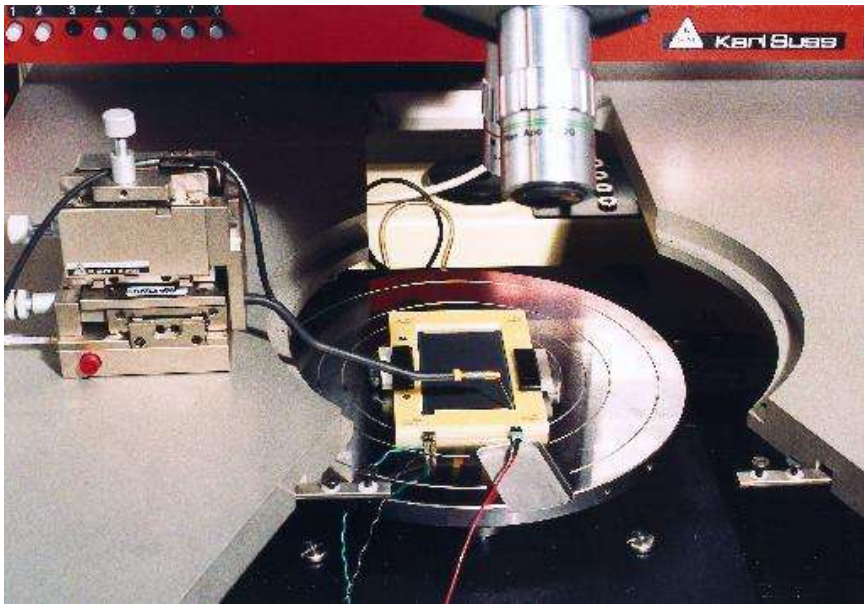

Figure 3 : Measurement of a DS SSD in it's frame.

2.1 Operating voltage and current

The operating voltage V_{op} is derived from the operating range defined between the depletion voltage V_d and the breakdown voltage V_{bd} defined as the biasing voltage corresponding to the maximum allowed current. Deep investigation has been made in order to define those in a reliable way. Depletion voltage V_d can be investigated by measuring, as a function of biasing voltage, the bias current i_{bias}, the bulk capacitance C_{bulk}, the bulk resistivity ρ_{bulk} and the interstrip capacitance $C_{interstrip}$, on the N side. Figure 4 shows $i_{total} = i_{bias} + i_{guard} = f(V)$ in black, $1/C^2_{bulk} = f(V)$ in blue and $\rho_{bulk} = f(V)$ in red.
The $i_{total} = f(V)$ graph shows a weak slope in the plateau area due to the nominal guard ring leakage. The 1/Cinterstrip N = f(V) graph (not represented) shows the same plateau as the $i_{total} = f(V)$ graph.

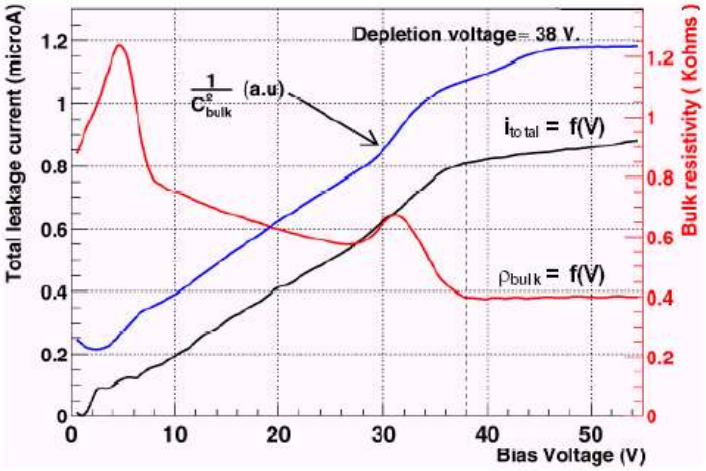

Figure 4 : Operating range of DS SSD STAR171.

The same detector has been assembled in a module and connected to the front-end electronics. Noise measurements of the strips provide also a good information on the depletion. Figure 5 shows the $i_{total} = f(V)$ graph in black squares and the RMS noise graph in red dots. They all show the same plateau for the same voltage range.

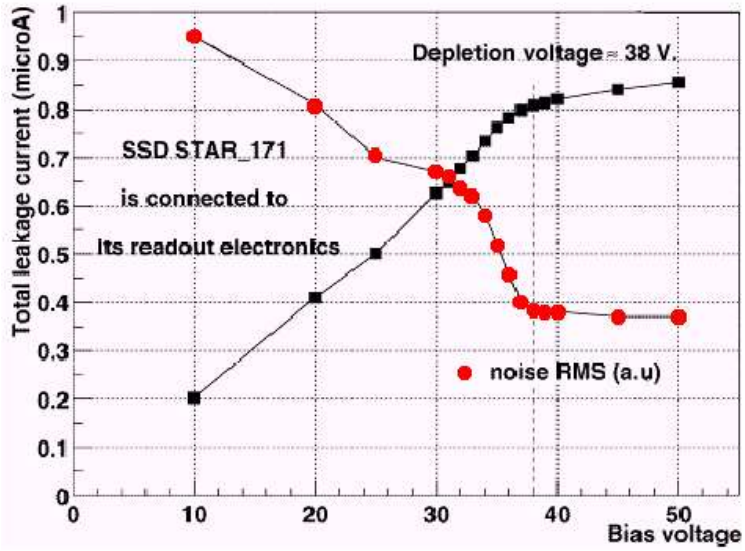

Figure 5 : Total current and noise as a function of voltage.

So, it has been demonstrated that the only $i_{total} = f(V)$ measurement provides consistent and exhaustive information on i_{bias}, i_{guard}, V_d, V_{bd}, and V_{op}.
Figure 6 represents the number of detectors as a function of their possible operating voltage. This plot is made by considering a detector as "1" inside the operating range and as "0" outside this range and adding together these values over the whole set of measured detectors. This graph shows that about 75% of the detectors can theoretically be operated with a unique common biasing voltage of 53 volts. Once the V_{op} has been defined, one can measure the corresponding operating total current i_{tot} whose mean value 1.65 µA appears in Figure 7.

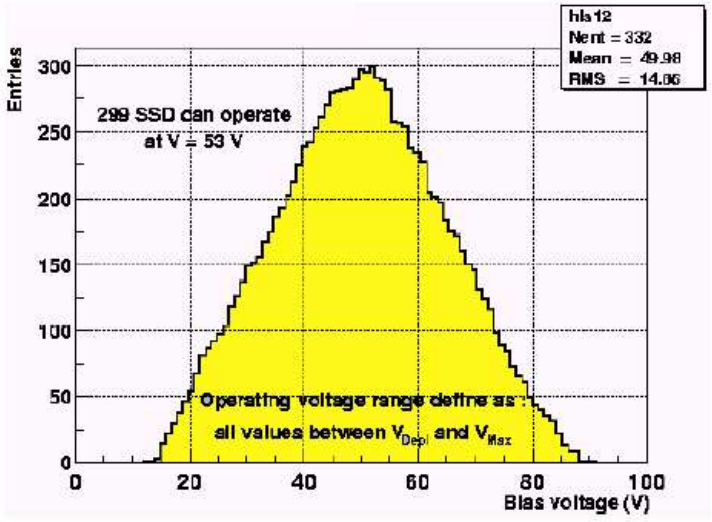

Figure 6 : Sum of the operating ranges of 332 detectors.

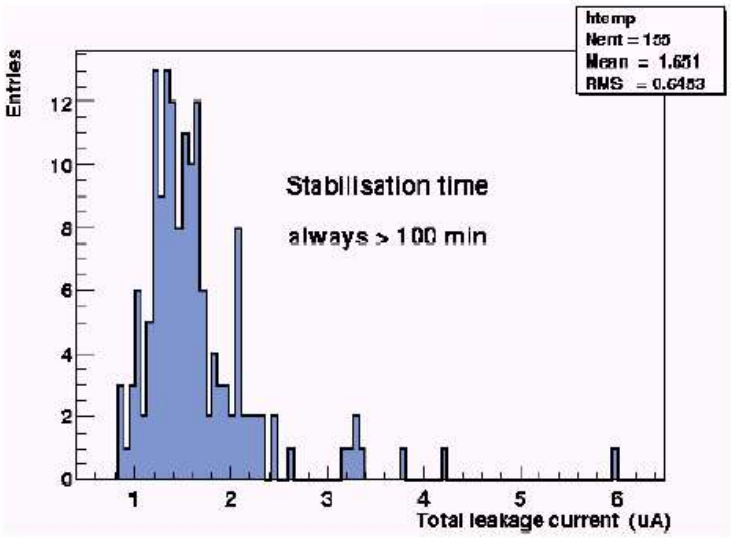

Figure 7: Total current itot: mean = 1.65µA

2.2 Coupling capacitors

The FEE is located on two separate but identical hybrids, one connected to the N side and one to the P side of the detector by means of capacitors integrated on top of each strip for AC coupling. Dielectric characteristics of the insulation, i.e. leakage current and capacitance, are obviously important for detection efficiency and data consistency. Measuring both leakage current and capacitance enables cross checking, the latter also validating the contact quality. During these measurements, a DC voltage of 100 V is applied across the capacitor to check if it stands the operating voltage.
These parameters are measured for each strip by stepping through the contact pads with a test probe. This option avoids all the switching and probe card problems without taking significant more time yet. The corresponding data are registered in the data base. The related distributions are presented on Figure 8 left for the P side and right for the N side. A capacitor is considered as dead if it leaks or if the capacitance is out of range. The mean number of dead capacitors is below 2 units on both sides. 85% of the DSSSDs have at most 4 dead capacitors on both sides i.e. less than about 0.5% of the 768 strips of each detector side.

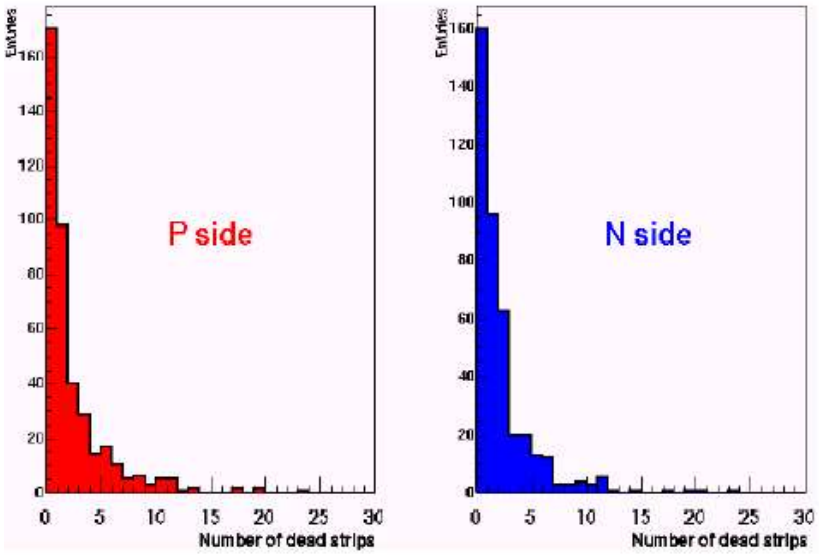

Figure 8 : Dead capacitors on P side (left) and N side (right)

2.3 Detector quality

Compiling the results of these different measurements provides a global information about the quality of the produced detectors as presented on table 1.

Class	Quality	Nb. of SSDs	%
1	Perfect	258	65
2	Good	74	18
3	>10 dead strips/side	20	5
4	High currents	14	3
5	Dead	20	5
6	V_d > 55V	13	3
7	To be tested again	1	/

Table 1: Quality of the 400 measured DS SSD.

2.4 Strip leakage current

For production, we consider that the $i_{total} = i_{bias} + i_{guard} = f(V)$ measurement described in 2.1 and the coupling capacitor measurement described in 2.2 are consistent to characterise a detector. We chose to avoid any disturbance of the main detector by DC test pads. If needed, it is possible to measure the strip leakage current on a test structure located on the same wafer as the real detector. It should be below 5 nA/strip. Furthermore, if the number of leaking strips becomes significant, the problem is detected by the measurement of i_{bias}. So, the strip leakage current is not measured in production, mainly for throughput reasons.

3 TAB technology

In order to meet the requirements listed above, the design of silicon strip layers has to take in account the following constraints:

- flexible connection between Alice128C and detector for cooling and cabling considerations,
- pitch adaptation from 95µm (detector) to 44µm (Alice128C),
- industrial process to achieve a yield of more than 97% of good channels.

This led to the use of TAB tape for the connection of the detector to the ALICE128C. Figure 9 and Figure 10 show the tape developed for this purpose.

The TAB tape has the following characteristics:

- identical for all the position of the readout chip related to the detector,
- a so-called “UIIU” ILB input topology to match the 44µm input pitch of the chip by splitting the tape in two staggered rows having 88µm pitch each,
- Thickness : 17µm Cu, 30µm glue and 70µm Kapton
- Windows are opened in bending area in order to avoid spring effect during the assembly process.

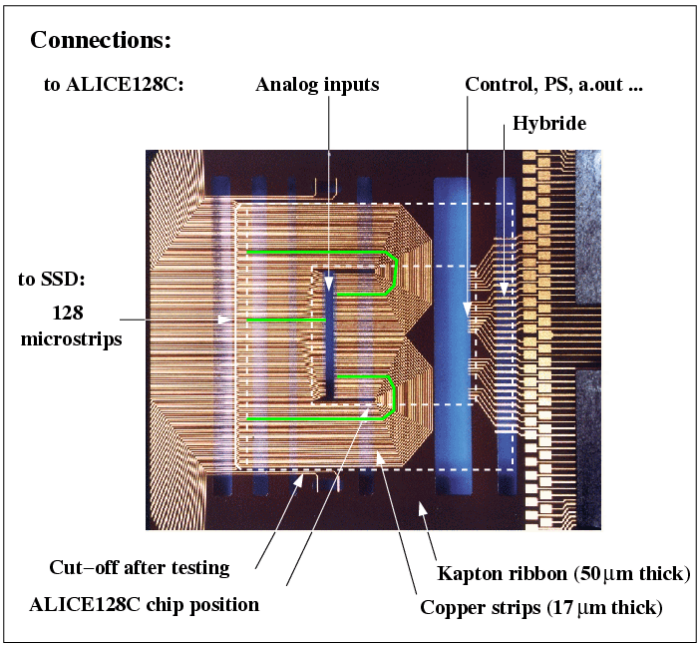

Figure 9 : TAB tape. The outer doted line shows the part really used for the connection, the inner one shows the location of the ALICE128c. The green lines show the geometry of the copper strips.

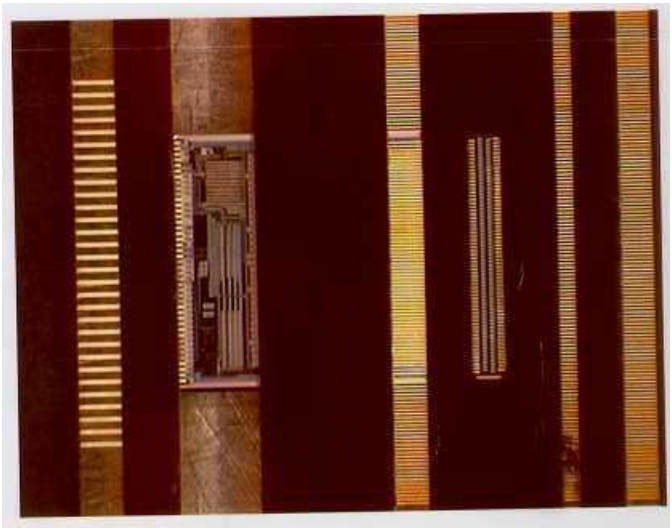

Figure 10 : ILB of the ALICE128C, at the left hand side the pitch is 135mm, at the right hand side the pitch is 88mm in staggered row

Due to the flexibility of use, the tape meets the requirement of 4 different pitches:

- One ILB at 88µm pitch in staggered rows of 44µm at the input of the readout chip (ALICE128c),
- One ILB at 135µm pitch at the output of the readout chip,
- One OLB at 95µm pitch at the detector level,
- One OLB at 300µm (line space 120µm) pitch at the hybrid level.

This tape has been designed by Thales and is produced by the company FCI (formerly named MCTS).

4 ALICE128C Front-End Chip

Each detector module includes two FE hybrids including each 6 FE ALICE128C chips. So producing 400 detector modules for STAR (320 on the experiment + spares) requires 12x400=4800 working chips. 6000 tested chips have been ordered at AMS, the test being a rough test made on the wafer. After cutting, sorting in boxes and TABing of these chips onto microcables, they are measured again in our laboratory before sending for TABing onto the hybrids and detectors.
Testing of these chips has been made easy by integrating inside the chip, from the design level, JTAG operated remote access to all the digital and analog parameters and also to a programmable on-chip pulse generator for each analog channel.

4.1 Manufacturer production and test on wafer

From 6000 tested production chips ordered at AMS, we have 5656 "good" chips, 5355 "bad" inked chips having been rejected by the rough wafer tests.

4.2 The use of microcables

The TABed microcables, providing electrical connection between the DS SSD and the FE chips and between the FE chips and the hybrid, allow for a mechanical freedom in the positioning of the hybrids supporting the FE chips versus the detector. Au layered Cu microcables (17 µm Cu on top of 70 µm Kapton) are used for STAR whereas Al microcables (14 µm Al on top of 12 µm Kapton) will be used for ALICE. Their use eases also the chip test and avoids the use of the probe station.

4.3 Laboratory test of the TABed chips

The accurate testing of these chips is then made at the laboratory after TABing of the chips onto microcables and mounting them in a plastic tests frame for easy handling and testing. So, the chip in its plastic carrier plugs easily into the test socket of the automated chip test equipment. The overall duration of the automated test is below 5 minutes per chip. The test results are recorded into the production database for later use.

The test includes 7 main steps.

- Power the chip and check "+i" and "–i" which should both be negligible.
- Test the digital part of the chip by means of JTAG.
- Bias the chip by sending via JTAG the 7 analog operating parameters.
- Check again "+i" which should stay at about the previous level and "–i" which should increase by 20 mA.
- By means of JTAG, switch one analog channel to transparent mode, pulse it with the on-chip pulse generator and register the sampled analog positive and negative output.
- With "0" input, make acquisition of the 128 channels for pedestal registration.
- With the on-chip pulse generator, pulse sequentially each analog channel with positive and negative pulses with values of +100, +250, -100 and –250 and register the corresponding outputs.

The measurement of 87 TABed production chips provided 83 good chips and 5 bad ones including 1 with overcurrent, 1 with 24/128 dead channels 2 with 2 dead channels and 1 with 1 dead channel. Plots of the other parameters are not represented as they present a very narrow dispersion around the nominal value. The 94% yield after the wafer tests corresponds mainly to cutting, handling and TABing.

5 COSTAR Control chip

The COSTAR control chip has been designed for remote JTAG monitoring and control of various analogue and digital parameters. Basic feature includes on-chip temperature measurement, which is especially important for air-cooling, and on-chip power supply voltage measurement. It includes also detector guard and bias current monitoring. One COSTAR is located on each STAR hybrid.
Testing of the COSTAR bare chip is performed on the probe station by means of a probe card and an automated test equipment. Calibrating of the on-chip temperature sensor is performed during the same process. Results are provided to the production data base. From 351 tested chips, 311 are "good" and 40 "rather bad".

6 Steps of the module production

In this production process, all the components are tested just after production : detector, Alice128c on wafer, COSTAR chip, flexible circuit glued on the carbon stiffener. Most of those tests are performed at IReS/Strasbourg ILB steps: the tape is connected to the ALICE128C (Figure 10, Figure 11, Figure 12) and then inserted into the plastic frame (Figure 13).

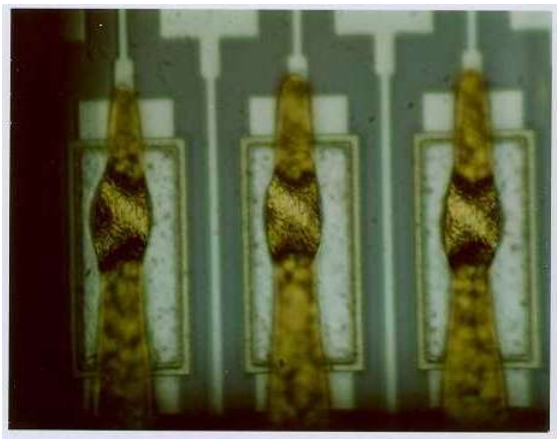

Figure 11 : detailed view of one of the rows at a pitch of 88mm.

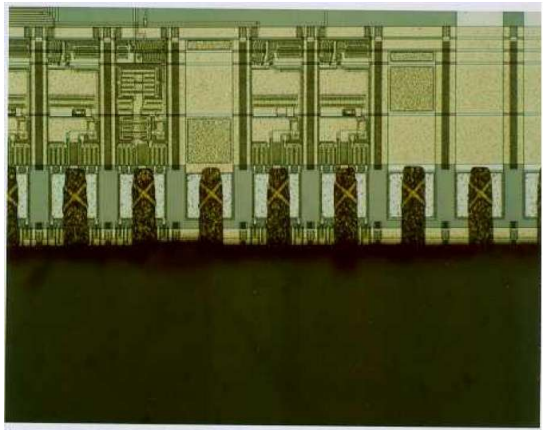

Figure 12 : detailed view of the ILB at 135mm pitch.

Short circuit removal : the short circuit between all the input and output strips is removed. The personalization is made related to the position of the chip. A reference number is written with laser beam for traçability.

Chip test : the chip tabed and mounted in the plastic frame is plugged in a ZIF (zero insertion force) socket. The test performed in this case checks all the connection of the chip, the analogue and digital characteristics of the chip. Then the results of measurements are stored in construction database.

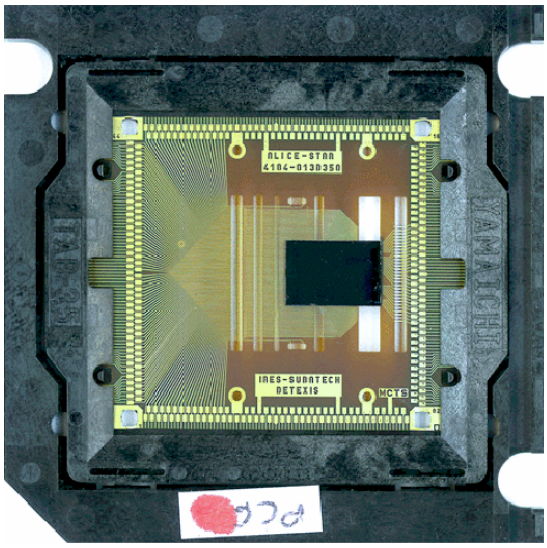

Figure 13 : photograph of an Alice128c (black rectangle) bonded to the TAB tape with the plastic frame. Size of the chip 8640 x 6080 mm

Hybrid mounting : once the flexible circuit is glued on the stiffener, it is checked, then equipped with SMD components and COSTAR. It is tested again.

OLB with the detector : all the inputs of the twelve chips are connected first to the detector.

OLB with the hybrid : two hybrid circuits are precisely positioned relatively to the detector, then the Alice128c are glued and connected to the hybrids (Figure 14).

Folding : the two fully hybrid circuits are folded on the top of the detector (figure 11).

Finally the detection module is fully tested. A method allowing the analysis of defects has been developed to diagnose what kind of fault occurs when a channel does not work and if it is due to the assembly process or not. This analysis is based on signal and noise measurements. The signal can be either a real signal coming from the detector (stimulation obtained with a β-source) or a pulse injected via the internal generator integrated in the ALICE128C. The noise is mainly due to the detector and the readout electronics. Moreover the contribution from the last one is sensitive to the capacitance connected at the input of the preamplifier.

Six different cases of defect can be diagnosed this way:

Case 1: noisy channel, probably due to the detector itself,

Case 2: non-connected strip, two possibilities: first a bad connection with the TAB bonding, second an interruption of the aluminium strip on the detector,

Case 3: preamplifier destroyed due to electrostatic discharge (ESD), being not protected against ESD, in order to lower the noise,

Case 4: dead channel, a defect in the chip itself,

Case 5: dead chip or not readable, due to bad connections during the OLB with the hybrid or a defect on the hybrid itself,

Case 6: pinholes in the detector coupling capacitor, a defect occurring in the detector production.

Except for the case 5, all the other defects are tolerable when not exceeding a percentage of 3%. Even if the first four prototypes showed defects of case 5, the beginning of the production gave detection module within the specifications.

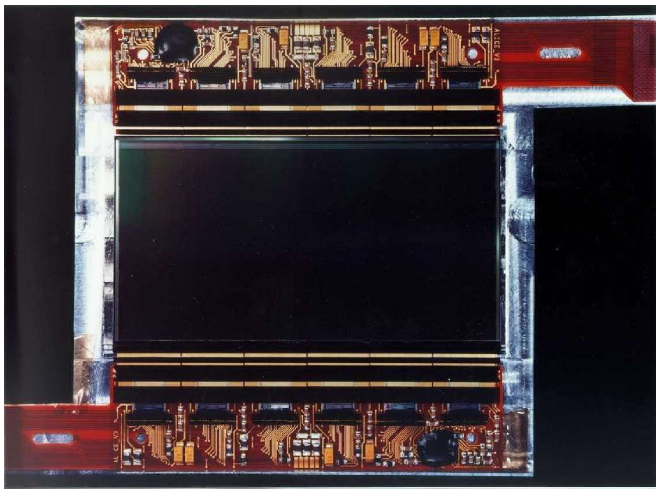

Figure 14 : detection module before folding. The detector is in the middle and the hybrids equipped with all the electronics are on both sides

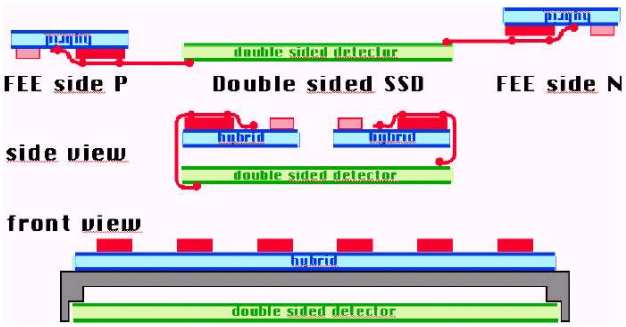

Figure 15 : schematic view of the operation consisting in folding the two hybrids over the detector.

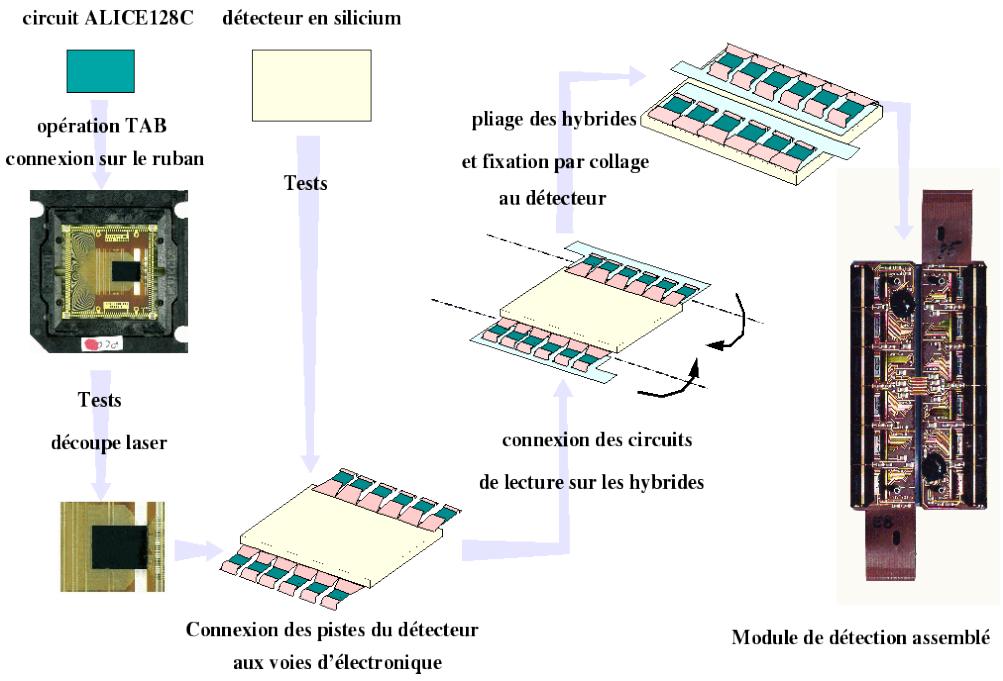

Figure 16: Summary of the module assembly

7 Test results

The last step consist of the verification if the detection module is suitable for tracking particles. The best way is to test the module with a beam of particles. This kind of test has been done several times at CERN. The dedicated setup is showed in figure 17.
One of the most important specifications is the signal to noise ratio, which has a direct consequence on the resolution of the particle hit localisation. Figure 18 shows the distribution of the signal to noise ratio on both sides of the detector. The results (S/N =28 for N side and 40 for P) side meets the requirement of STAR tracking.

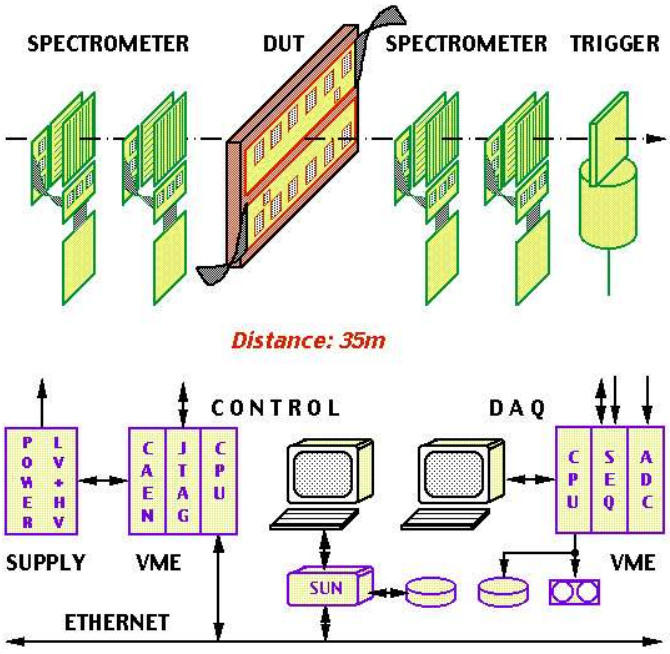

Figure 17: schematic view of a beam test setup.

Another aspect of the detection module specification is the ability to match one signal from one side to the other. Figure 19 shows the performance of the charge matching, This result meets the requirement too.

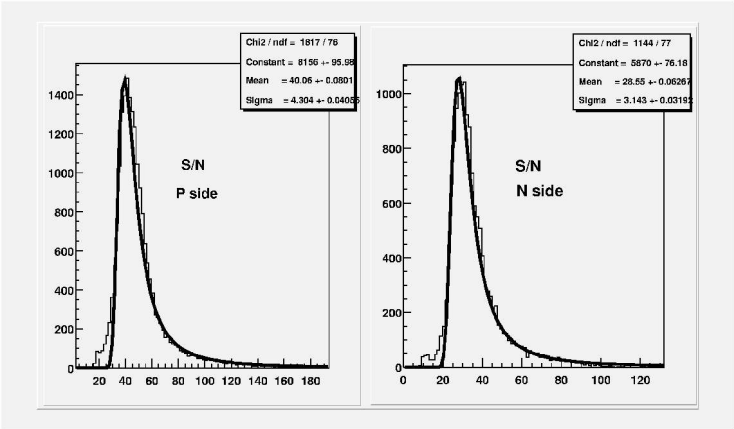

Figure 18: signal to noise ratio of detection module on both sides.

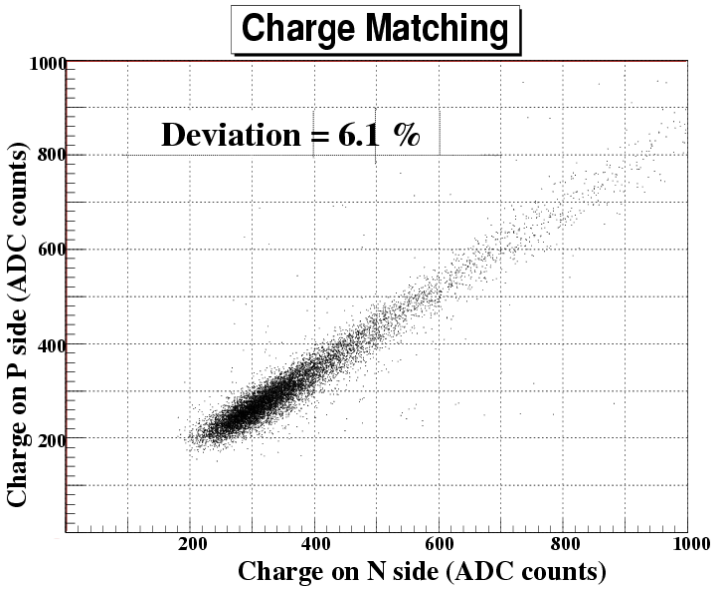

Figure 19: charge matching between side P and side N

8 Detailed material budget

The SSD module can be split in the following components using the specified material :

Wafer				Silicon

Hybrid	Printed circuit	Flexible circuit		Kapton/Copper
		A128C chip	chip	Silicon
			A128C glue	Silver silled epoxy paste H20E
		Costar chip	chip	Silicon
			Chip coat	Namics G8345 (epoxy based)
			wire bonding	Aluminum
		Passive components	SMD components	
			Glue	Silver silled epoxy paste H20E
	Stiffener	Stiffener		Carbon fiber/Epoxy
		Pins		Aluminum
		Glue		Epoxy Araldite 2014
	Glue (flex on stiffener)			Epoxy Araldite 2014
TAB	TAB			Kapton/Copper
	Chip coat			Namics G8345 (epoxy based)
Glue (wafer on hybrid)				Silicon RTV 162

Table 2 : material budget of the detection module