SSD documentation

Readout chain

Version Number : 3

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1 Description of the SSD readout chain

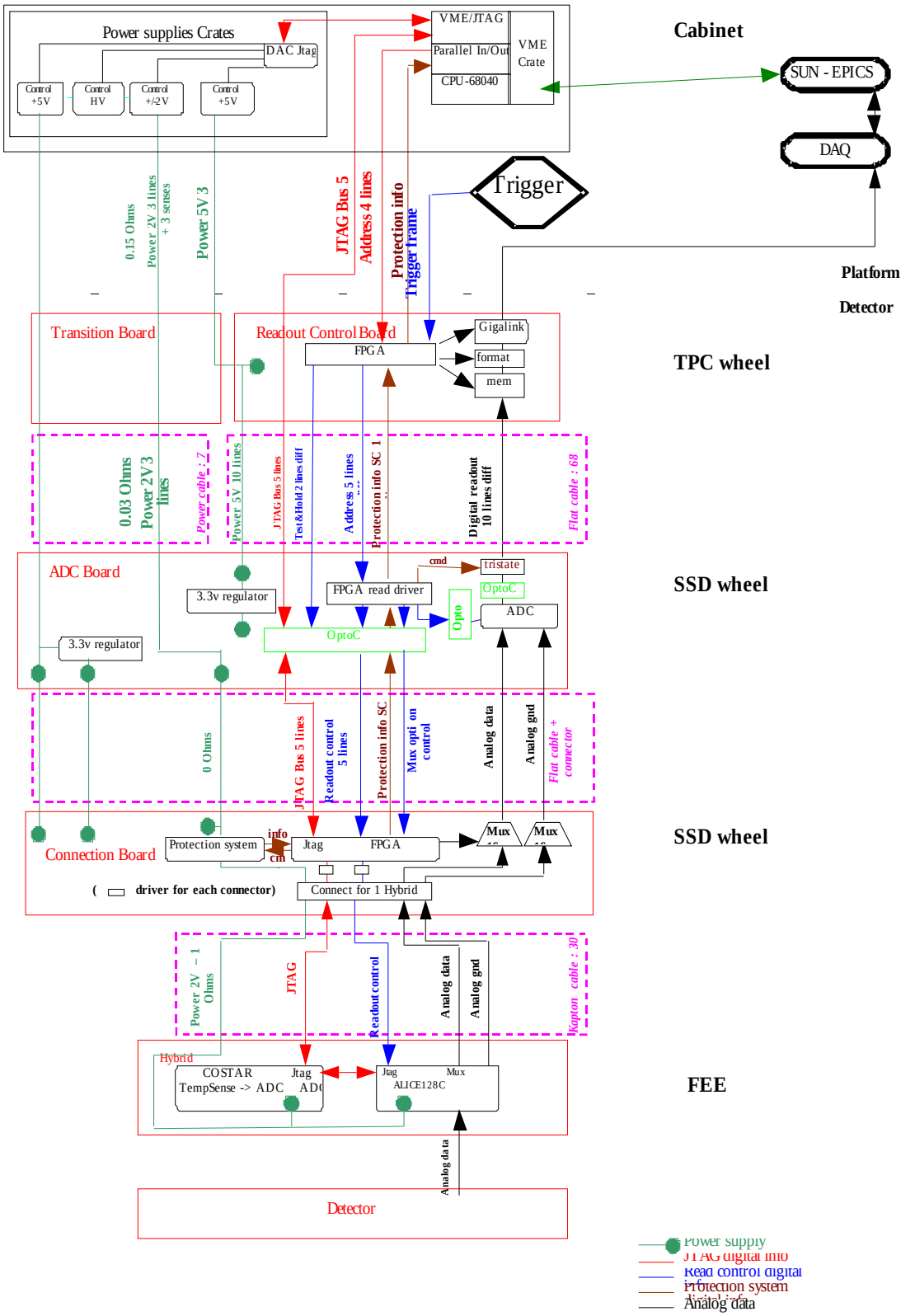

Figure 1 : schematic overview of the SSD electrical system

Figure 1 shows the global electrical system of the SSD from the FEE to the DAQ, the slow control and the power supply.

The readout chain is composed by the following components :

- 1 hybrid circuit where sit 6 front end chips (ALICE128C) and 1 control chip (COSTAR), this component is part of the detection module.
- 1 connection and control board (C2D2) which is basically the interface between 16 hybrids and 1 ADC board. This board is able to detect a latch-up on one of the hybrid circuit, to switch off the power supply of this hybrid and to bypass all the signals without any modification in the readout sequence.
- 1 ADC board which convert the analogue signal coming from one detection module.
- 1 readout board which is a kind of “hub” in the readout chain and the slow control system of the SSD. It is the interface between the barrel and the “outside world” (slow control, trigger and DAQ).

Electrically the SSD is divided in four subsystems (one P-side and one N-side on each clamshell), which correspond in terms of data to four half of ten ladders (). The first division by 2 is due to the mechanical structure (two clamshells) and the second division by 2 is due to the bias voltage of the double sided silicon strip detector (around 40V). It involves the FEE to work at a floating ground equal to this bias voltage.

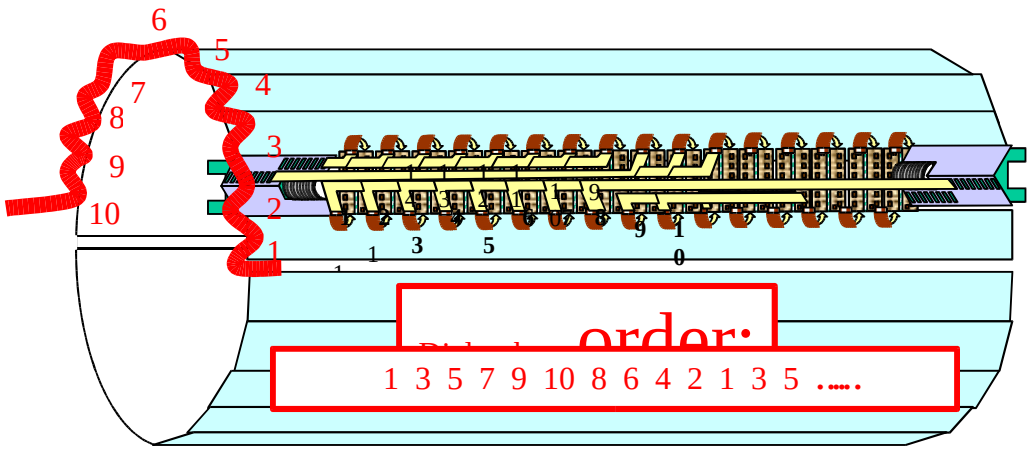

Figure 2 : division of the SSD barrel in four subsystems. Daisy-chain of the ladders.

To reduce the number of cables and readout boards, the 10 ADC boards of one half clamshell are daisy-chained, each of them having a specific address. Each ADC board will be requested by the readout board to send a data in the specific order mentioned on figure 2. To achieve this readout scheme, the speeds of the buses have been chosen consequently (figure 3).

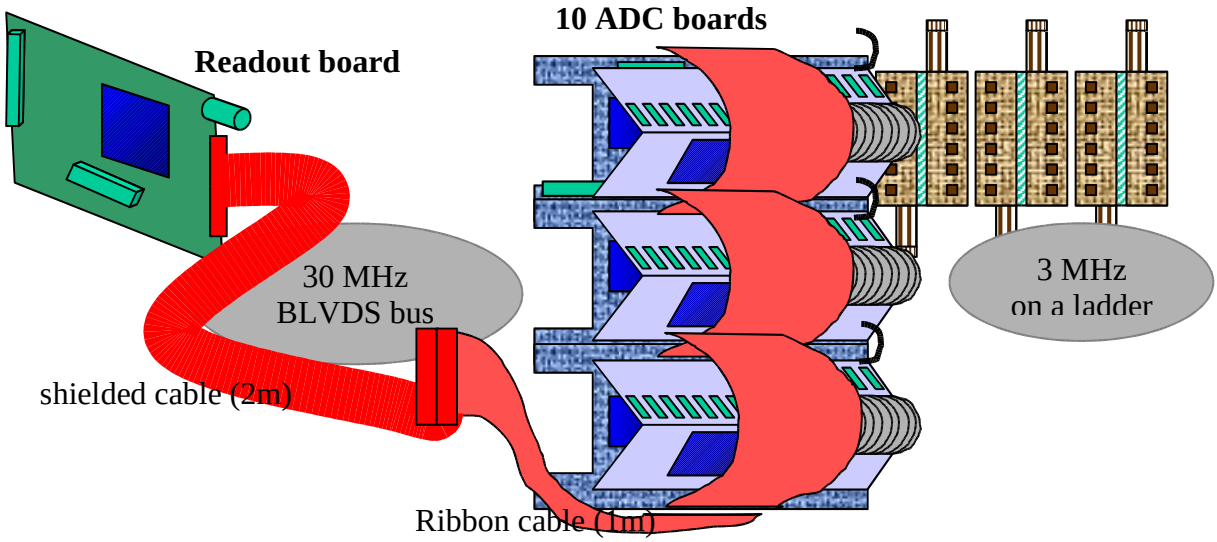

Figure 3 : speeds of the SSD buses

The total number of printed circuit boards is:

- 4 readout and control boards, each one addressing 10 ladder P or N sides
- 40 ADC boards, one at the end of each ladder, 10 of them are multiplexed together.
- 40 C2D2 boards multiplexing and controlling 16 hybrids (each one corresponding to a set of P or N sides of the detection modules).

2 ADC board

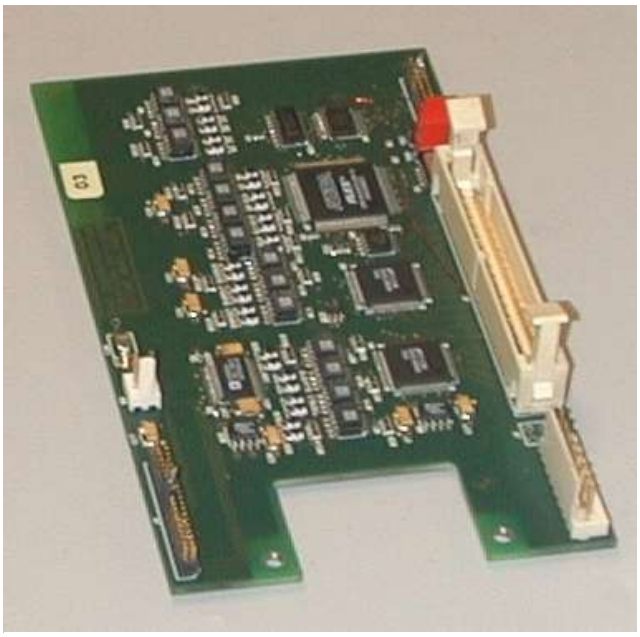

Figure 4 : photo of one ADC board

The ADC board has been designed in order to sit at the bottom end of the ladder (figure 2 and figure 4). The features of this device are the following (figure 5):

- Decoding the commands coming from the Readout board and sending them to the C2D2 board,
- Generating the +3V voltage for the C2D2 board,
- Translating the signals from the ground reference to a floating ground which can be the low voltage side (around 0 V) or the high voltage side (around 40V) of the detector.
- Converting the analogue signals coming from the detection modules passing through the C2D2 board.
- Measuring its own temperature.

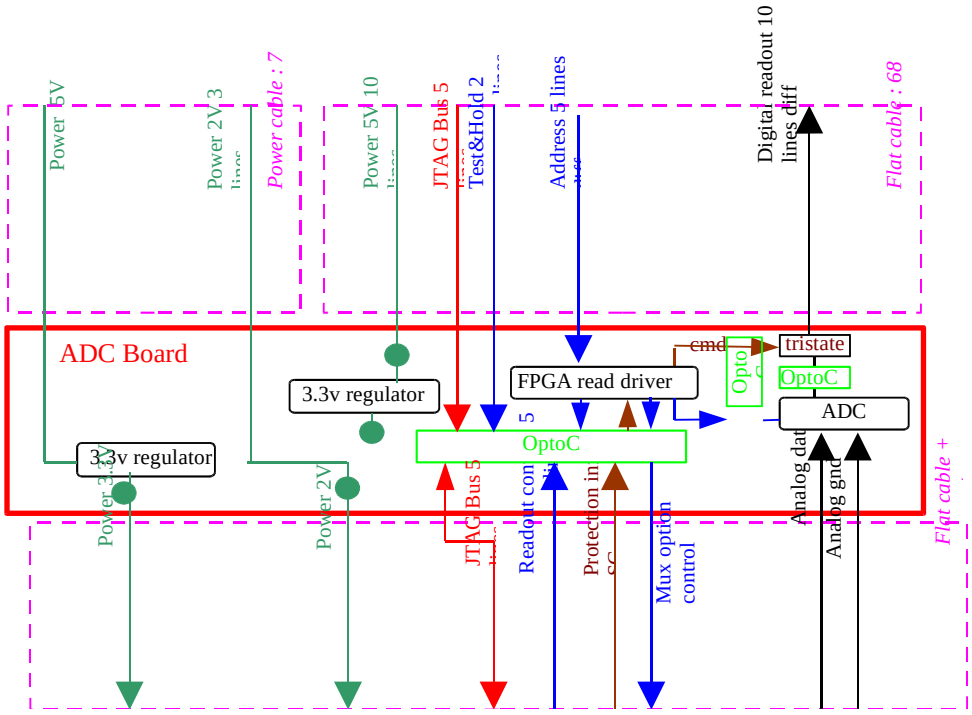

Figure 5 : Schematic view of the ADC board

3 Connection board

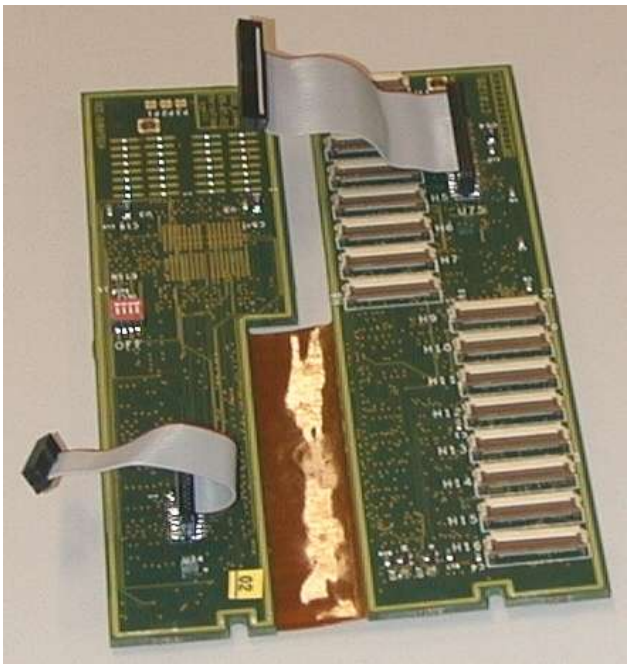

Figure 6 : photo of a C2D2 board

The C2D2 has been designed to sit on the top end of the ladder. This is why the board is composed of two printed circuit boards linked by a flexible circuit (figure 2 and Figure 6). The features of the boards are the following (figure 7):

- Latch-up detection : when a latch-up occurs in one hybrid, the power supply of the hybrid is switched off, and all the control signal are bypassed in order to avoid any disturbance during the readout.
- Remote power supply control and monitoring of each hybrid.
- Multiplexing the analogue signals coming from the 16 hybrids and sending them to the ADC board.
- Transmission of the commands coming form the ADC board to the hybrids of the detection modules.
- Temperature measurement readable by the JTAG chain.
- Generation of reference voltages to replace the Costar pedestal compensation in case of troubles.

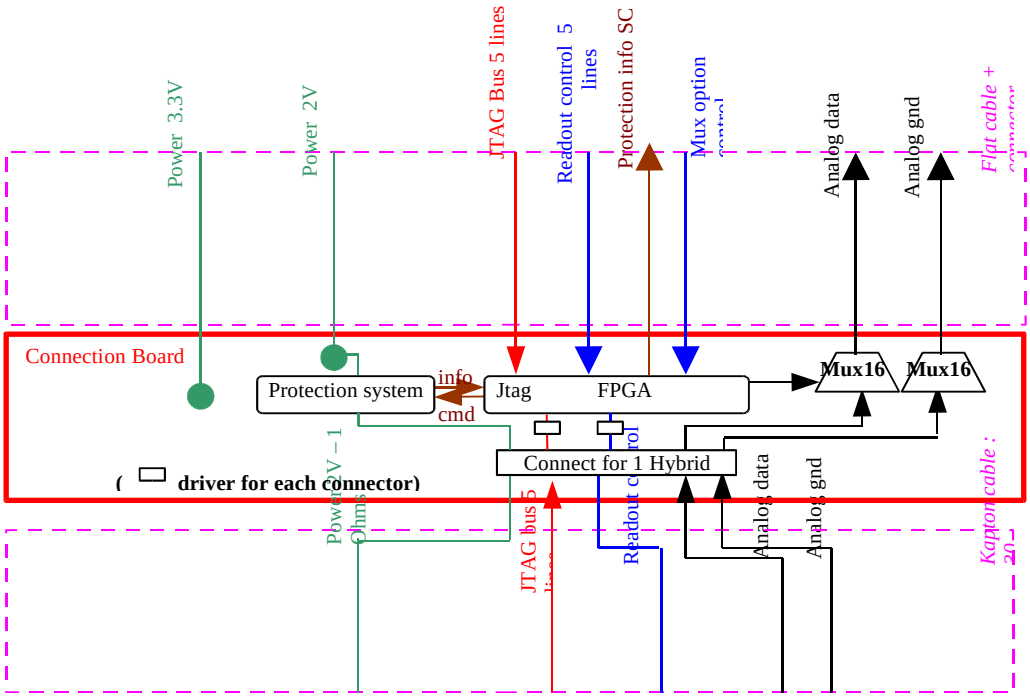

Figure 7 : schematic view of the C2D2 board

4 Readout control board

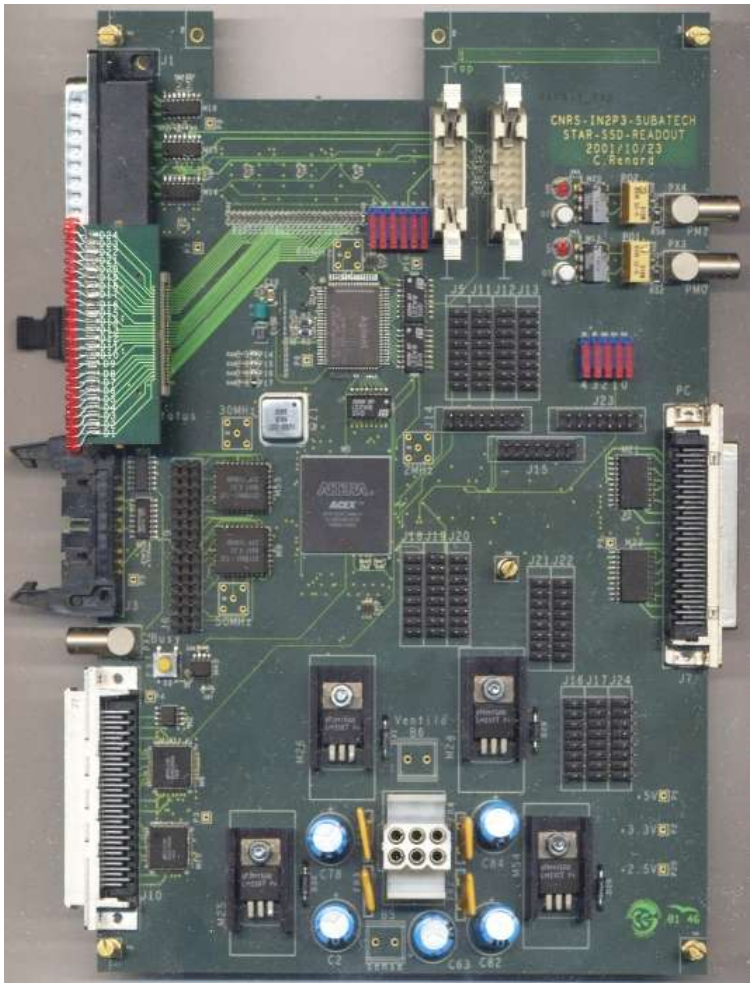

Figure 8 : Photo of the readout board

The main part of the readout board (Figure 8 and Figure 9) is in a programmable device (Altera acex 1K100 FPGA). This FPGA decodes the commands issued by the Trigger, plays the readout sequence of the front-end electronics, formats the data before sending them to the DAQ and interfaces the slow-control and the SSD test-bench.

The signals coming from the trigger are the trigger word (four bits) and the RHIC_strobe (10MHz). They are in differential PECL and are converted to TTL on board. The RHIC_strobe is phase filtered by a "roboclock" circuit. This circuit also delivers a 50MHz clock (trg_50_clk), phase locked to the RHIC_strobe. These two clocks are used to read and decode the trigger commands. Two handshake signals are sent back to the trigger (not used for the moment).

The onboard 60MHz-quartz oscillator (tx_clk) is phase filtered by a "roboclock" circuit. This circuit also delivers a 30MHz clock (fe_clk), phase locked to tx_clk. Fe_clk is used to sequence the readout of the front-end data (10 bit words). These data are in BLVDS and are

converted to TTL onboard. Tx_clk is used to send to the DAQ the header and the formatted data (20 bit words). A Giga-link circuit serialises these 20bit-60MHz-words that are, then, converted to light signals and sent to the DAQ inside an optical fibre.
The readout board receives a 7 Volts – 6 Amperes power supply. It creates 3.3 Volts and 2.5 Volts onboard, each of them protected by a 2.5 Amperes polyfuse. Onboard 5 Volts is protected by a 4 Amperes polyfuse. The board provides the ADC board chain with a 5 Volts power supply, protected by a 2.5 Amperes polyfuse.

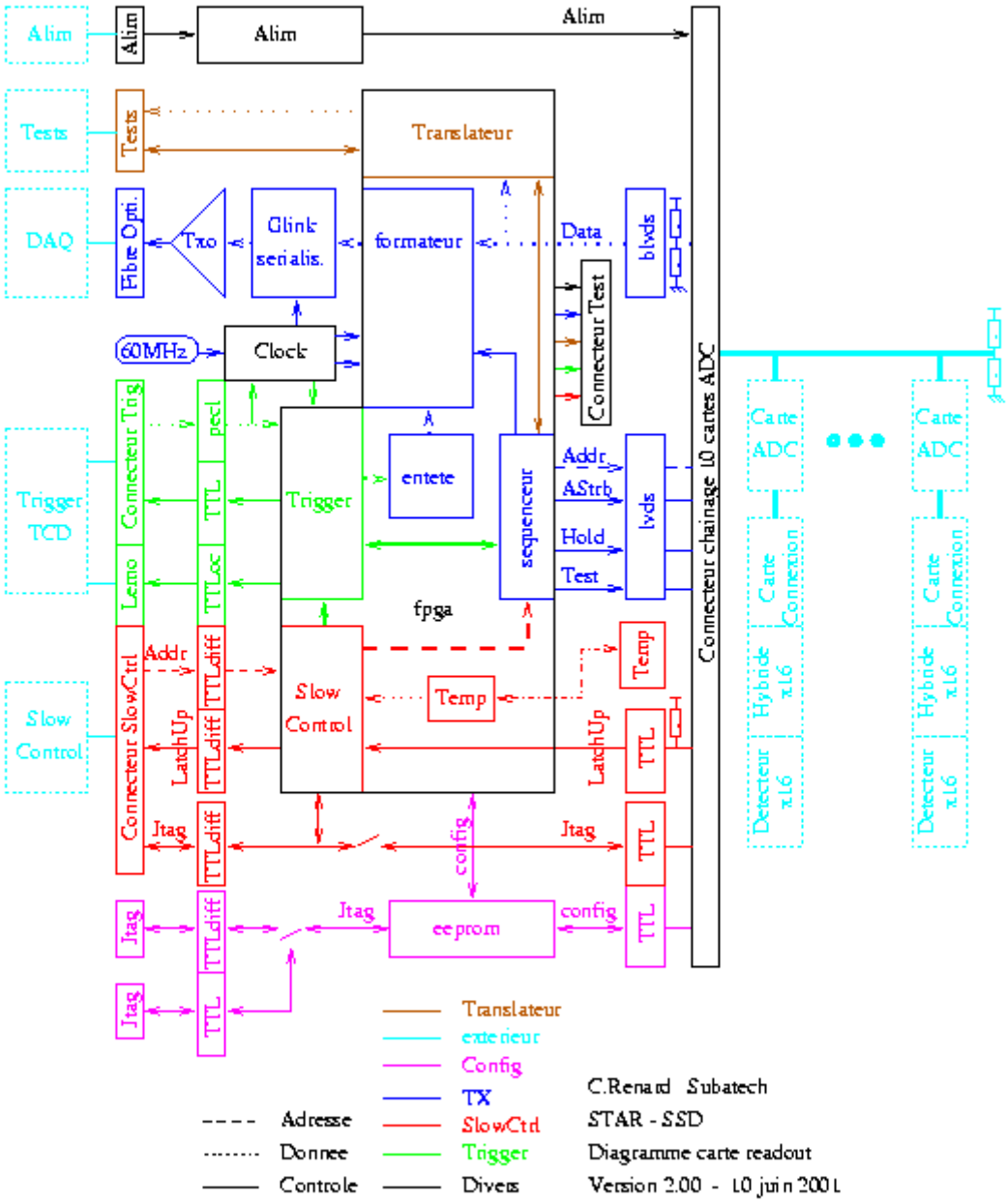

Figure 9 : schematic view of the readout board

To get room for the SSD Readout boards, the cooling pipes have been removed from the top of three SVT Readout boxes at each end of the TPC wheel. There will be two Readout boards at each end of the TPC wheel. The Readout boards will be located between the SVT Readout boxes and the Air-Manifold (Figure 10). Some room must be left at the back for the SVT optical fibre. The top of the SVT Readout boxes cannot be used as radiator because it is not cooled and might then be warm. It will be electrically isolated from SVT box. A prototype of the SSD readout box has been designed (Figure 11).

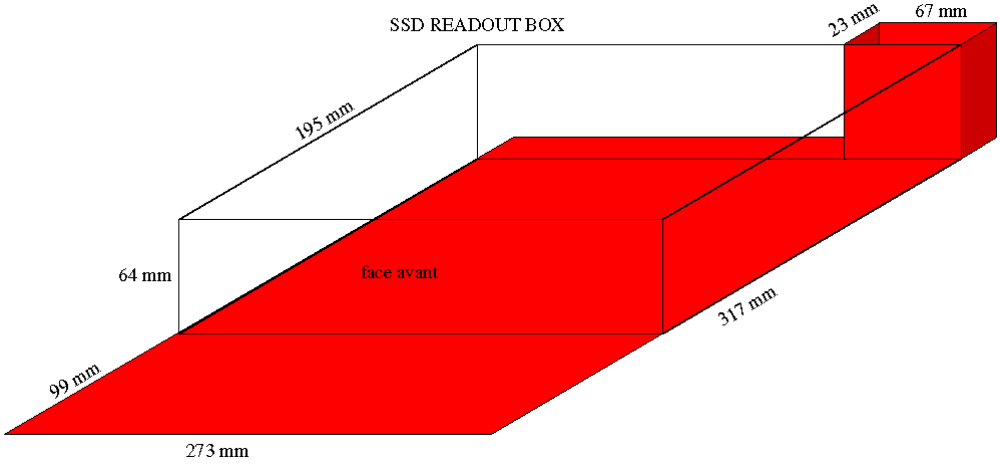

Figure 10 : Available space on the SVT readout box for the SSD readout board

Figure 11 : Prototype of the SSD readout Box

5 Readout time calculation

	clock60	*clock50*	*clock30*	*clock100*	*other*	*individual*	*cumulated*	
ns	*16.667*	*20.000*	*33.333*	*100.000*	*1.000*	*ns*	*ns*	
cmd input				1		100.0	100.0	
cmd decode		1				20.0	120.0	
clock shift					16.67	16.7	136.7	
hold wait	3		45			1550.0	1686.7	
event_start	9					150.0	1836.7	
Header	64					1066.7	2903.3	
data_start	9					150.0	3053.3	
TPC wait					100000	100000.0	103053.3	
Token in			2			66.7	103120.0	no abort
ADC pipeline			30			1000.0	104120.0	no abort
Rdo pipeline			10			333.3	104453.3	no abort
Min data	15360					256000.0	360453.3	no abort
data	230400					3840000.0	4200453.3	
asic fill to 64x256	36864					614400.0	4814853.3	to be verified
asic fill to 64x512	147456					2457600.0	7272453.3	to be verified
event_end	9					150.0	7272603.3	
Total						**7272603.3**		