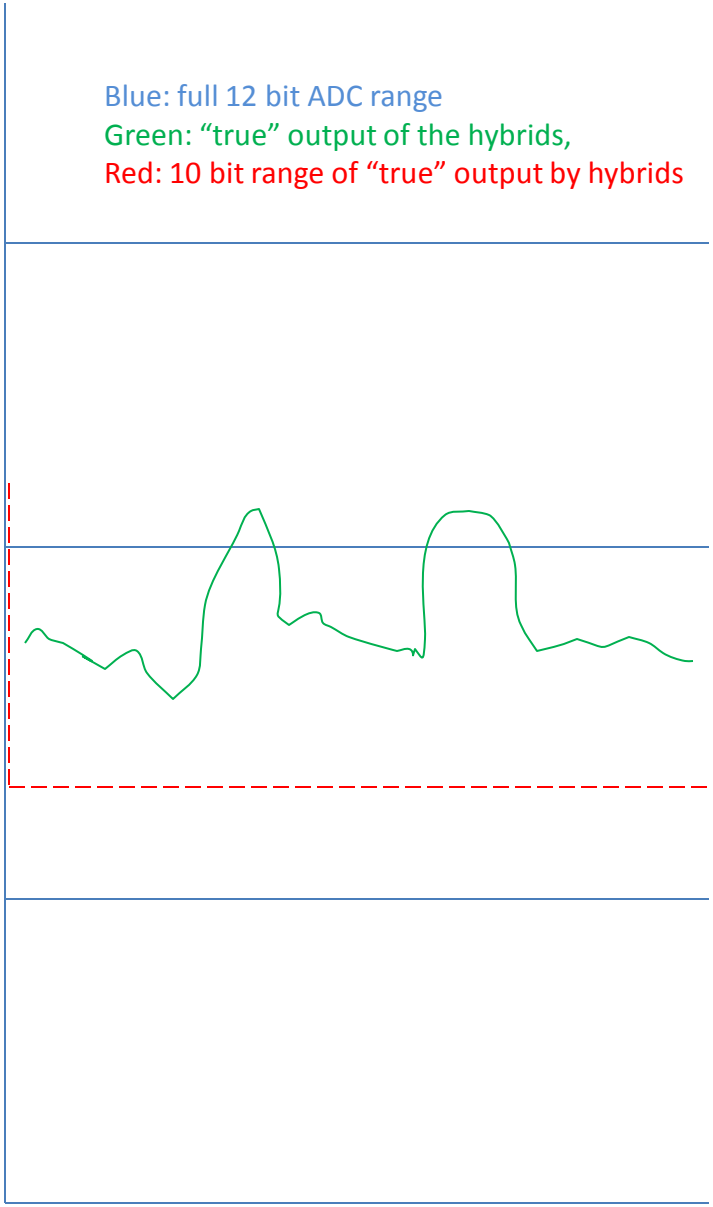
SSD pedestal subtraction

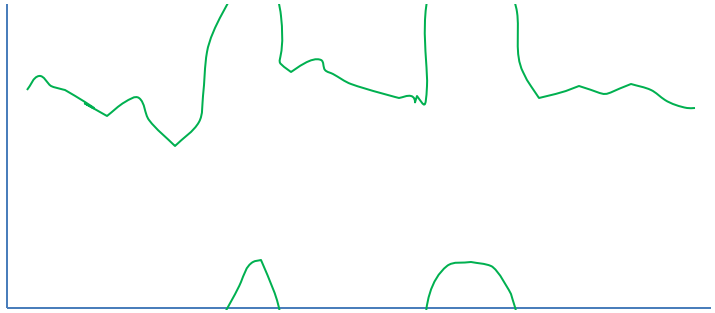
- The SSD data are collected with a 12 bit ADC
- Only 10 bits are sent to DAQ, the top two bits are dropped before sending the data
- This leads to an ambiguity regarding the absolute magnitude of the received ADC data. This is important because the hybrid signals are level shifted by an unknown amount before entering the ADC. But the good news is that the DC shift is the same for all hybrids and all ladders.
- The hybrids are only capable of producing signals in the range 0-1023 … so if we knew the level shift then 10 bits would be enough.
- Due to the fact that we drop the top two bits on the 12 bit ADC, then any amount of level shift will cause some of the signals to go “off the top” of the scale and reappear as (apparently) low level signals. Signals can also go “through the bottom” and reappear as (apparently) high level signals at the top of the scale.
- The wrap around problem, which is caused by the level shift (or offset), must be resolved before calculating the pedestals.
- Solution: take a pedestal run. Shift the data to midscale while simultaneously fixing the wrap around effects, calculate the pedestals, and finally shift the pedestals to a baseline value of 100 for P signals, and a baseline value of 900 for N signals.

What is going on inside the electronics

Blue: full 12 bit ADC range
Green: “true” output of the hybrids,
Red: 10 bit range of “true” output by hybrids



What we actually see
(note that signals can also wrap around off the bottom of the plot and reappear at the top)



Pedestal Subtraction for the SSD

- The signal is mixed with noise when it is observed
  - (S+N) = observed signal
- Pedestal subtraction removes the (average) noise
  - $[\ (S+N) - \text{Pedestal}\ ]_{\text{mod}1024}$
- All additions and subtractions are **modified** modulo arithmetic (example, below)
  - if ([(S+N) – Pedestal] >= 1024) S = [(S+N) – Pedestal] – 1024
  - if ([(S+N) – Pedestal] < 1024) S = [(S+N) – Pedestal]
  - if ([(S+N) – Pedestal] < 0) S = [(S+N) – Pedestal] + 1024
- Calculate the Pedestal
  - Collect a sample of data with random triggers
  - Discard bad ladders, Discard bad wafers, Discard bad hybrids, Discard bad strips
  - WA = average noise on one wafer = < N > Sum(all good strips on one wafer) / Number(good strips on wafer)
  - Pedestal = $< [\ N - WA + 512\ ]_{\text{mod}1024} >$ - 412 for P side data (shift baseline to 100)
  - Pedestal = $< [\ N - WA + 512\ ]_{\text{mod}1024} >$ + 388 for N side data (shift baseline to 900)
- Calculate the Signal … Signal = $\{\ [\ (S+N) - (WA-100)\ ]_{\text{mod}1024} - \text{Pedestal}\ \}_{\text{mod}1024}$

  Signal = $\{\ [\ (S+N) - (WA-900)\ ]_{\text{mod}1024} - \text{Pedestal}\ \}_{\text{mod}1024}$

Notes

- Note modified modulo arithmetic: true modulo(1024) arithmetic does not work when subtracting numbers so the arithmetic must be done with the sequence of if statements, shown on the previous page.
- Note that the pedestal data wrap can also around … especially on the low side. Wrap around effects are not limited to the physics signals.
- Luis has empirically determined that a value of 212 counts can be used instead of Wafer Average shown on the previous page. The goal is to put the pedestal data near 512 before doing the pedestal average. This is sufficient to solve the "wrap around" problem due to the missing top 2 bits from the SSD ADC data. Then continue the algorithm as shown on the previous page. In other words:
- Pedestal = $< [N + 300]_{mod1024} >$ – 412 for P side data (shift baseline to 100)
- Pedestal = $< [N + 300]_{mod1024} >$ + 388 for N side data (shift baseline to 900)
- Signal = $\{ [(S+N) - 112]_{mod1024} - \text{Pedestal} \}_{mod1024}$ for P side data
- Signal = $\{ [(S+N) + 688]_{mod1024} - \text{Pedestal} \}_{mod1024}$ for N side data