D-RORC registers at BARi:

Reg. index	Byte offset	Short name	Description	Access mode	
0	0x00	RCSR	D-RORC control and status	R/W	**R O R C**
1	0x04	RERR	D-RORC error register	R	
2	0x08	RFID	D-RORC firmware ID	R	
3	0x0C	RHID	D-RORC hardware ID	R/W	
4	0x10	CSR	Channel control and status	R/W	**D D L C H A N N E L**
5	0x14	ERR	Channel error register	R	
6	0x18	DCR	Channel DDL command register	W	
7	0x1C	DSR	Channel DDL status register	R	
8	0x20	PGP1R	Channel Pattern Generator Parameter 1	W	
9	0x24	PGP2R	Channel Pattern Generator Parameter 2	W	
10	0x28	PGP3R	Channel Pattern Generator Parameter 3	W	
11	0x2C	PGP4R	Channel Pattern Generator Parameter 4	W	
12	0x30	PGSR	Channel Pattern Generator Status	R	
13	0x34	RRBAR	Channel Receive Report Base Address	W	
14	0x38	RAFLR	Channel Receive Address FIFO Low	W	
15	0x3C	RAFHR	Channel Receive Address FIFO High	W	
16	0x40	TRBAR	Channel Transmit Report Base Address	W	
17	0x44	TAFLR	Channel Transmit Address FIFO Low	W	
18	0x48	TAFHR	Channel Transmit Address FIFO High	W	
19	0x4C	Reserved			
20	0x50	RDR1R	Channel Receive Data Rate 1	R	
21	0x54	RDR2R	Channel Receive Data Rate 2	R	
22	0x58	RDR3R	Channel Receive Data Rate 3	R	
23	0x5C	RDR4R	Channel Receive Data Rate 4	R	
24	0x60	TDR1R	Channel Transmit Data Rate 1	R	
25	0x64	TDR2R	Channel Transmit Data Rate 2	R	
26	0x68	TDR3R	Channel Transmit Data Rate 3	R	
27	0x6C	TDR4R	Channel Transmit Data Rate 4	R	
28	0x70	Reserved			
29	0x74	Reserved			
30	0x78	Reserved			
31	0x7C	Reserved			
32	0x80	JCSR	JTAG control/status	R/W	**J T A G**
33	0x84	JERR	JTAG error register	R	
34	0x88	JCR	JTAG command register	W	
35	0x8C	JSR	JTAG status register	R	
36	0x90	JTA	JTAG Transmit Address	W	
37	0x94	JBL	JTAG Block Length	W	
38	0x98	JRA	JTAG Receive Address	W	

D-RORC control/status register bits:

Bit	Command register content	Status register content
0	D-RORC reset	Read as 0
1	Channel 0 reset (excluding the DIU)	Read as 0
2	Channel 1 reset (excluding the DIU)	Read as 0
3	Clear D-RORC error register	Read as 0
30..4	Reserved	Reserved
31	Reserved	Error register is NOT empty

Channel control/status register bits (offset 0x10):

Bit	Command register content	Status register content
0	DIU reset	Read as 0
1	Clear data FIFO	Read as 0
2	Clear Receiver Address FIFO	Read as 0
3	Clear Transmitter Address FIFO	Read as 0
4	Clear D-RORC error register	Read as 0
5	Clear data rate counters	Read as 0
6	Reserved	Reserved
7	Reserved	Reserved
8	Data download (RDMA) enable/disable	Data download is active
9	Data receiver (WDMA) enable/disable	Data receiver is active
10	Pattern generator enable	Pattern generator is active
11	Pattern generator disable	Read as 0
12	Loop-back enable/disable	Loop-back is set
13	Reserved	Link down
14	Reserved	Link full
15	Reserved	DTCC register is NOT empty
16	Reserved	DDL command register is NOT empty
17	Reserved	Receive report base address is NOT set
18	Reserved	Receive address FIFO is empty
19	Reserved	Receive address FIFO is full
20	Reserved	Transmit report base address is NOT set
21	Reserved	Transmit address FIFO is empty
22	Reserved	Transmit address FIFO is full
23	Reserved	Receiver status FIFO is NOT empty
24	Reserved	Receiver data FIFO is almost full
25	Reserved	Receiver data FIFO is NOT empty
26	Reserved	Transmit data FIFO is NOT empty
27	Reserved	Transmit data FIFO is almost full
28	Reserved	Transmit is waiting for the DTCC
29	Reserved	Reserved
30	Reserved	Reserved
31	Reserved	Error register is NOT empty

JTAG control/status register bits (offset 0x80):

Bit	Command register content	Status register content
0	JTAG reset	Read as 0
1	Clear JTAG error register	Read as 0
2	JTAG download enable	JTAG download is active
3	JTAG download disable	Read as 0
30..4	Reserved	Reserved
31	Reserved	Error register is NOT empty

Pattern generator parameters (offset 0x20, 0x24, 0x28, 0x2C):

Pattern Generator Parameter 1			
31	**30** ... **4**	**3** ... **0**	
Rand.	Block length	Pattern code[1]	

Pattern Generator Parameter 2	
31	**0**
Initial data word/Random seed	

Pattern Generator Parameter 3	
31	**0**
Initial event number	

Pattern Generator Parameter 3		
31	**30** ...	**0**
Inf.	Cycle number	

Note:

1. Valid pattern codes:
   - 0 – constant zero
   - 1 – constant ones
   - 2 – alternating
   - 3 – flying zero
   - 4 – flying one
   - 5 – incrementing
   - 6 – decrementing