The STAR Trigger

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Abstract

We describe the trigger system that we designed and implemented for the STAR detector at RHIC. This is a 10 MHz pipelined system based on fast detector output that controls the event selection for the much slower tracking detectors. Results from the first run are presented and new detectors for the 2001 run are discussed.

1 Introduction

The STAR Trigger is designed to facilitate the search for new states of matter such as the quark-gluon plasma and the quest to understand the interior of hadrons. It is a pipelined system in which digitized signals from the fast trigger detectors are examined at the RHIC crossing rate [1] ($\sim$10 MHz). This information is used to determine whether to begin the amplification-digitization-acquisition (ADA) cycle for slower, more finely grained detectors. The slow detectors [2] provide the momentum

[1] Typically 9.37 MHz during the 130 GeV per nucleon pair $AuAu$ running in Summer 2000.

[2] Fast detectors are fully pipelined. Slow detectors are not and include the central Time Projection Chamber (TPC), Silicon Vertex Tracker (SVT), Forward TPC (FTPC), Shower Max Detector (SMD), Photon Multiplicity Dectector (PMD), Time-of-Flight-patch (TOFp), and Ring Imaging Cherenkov (RICH).

and particle identification on which our physics conclusions are based, but they can only operate at rates of $\sim$100 Hz. Interaction rates approach the RHIC crossing rates for the highest luminosity beams, so the fast detectors must provide means to reduce the rate by almost 5 orders of magnitude. Interactions are selected based on the distributions of particles and energy obtained from the fast trigger detectors. Interactions that pass selection criteria in four successive trigger levels are sent to storage at a rate of $\sim$5 Hz ($\sim$50 MB/s). The final trigger decision is made in Level 3 based on tracking in the slow detectors and is discussed elsewhere in this volume. The first three levels, 0, 1, and 2, are based on fast information, as discussed here.

Data flow through the trigger (TRG) is shown in Figure 1. The trigger detectors in our first run consisted of a Central Trigger Barrel (CTB), and two Zero Degree calorimeters (ZDC East and ZDC West). The 240 slats of the CTB measure charged particle multiplicity in the pseudo-rapidity range $-1 < \eta < 1$ and 2π in azimuth angle ϕ while the ZDCs measure neutron multiplicity in a small solid angle near zero degrees. The anode wires at the two ends of the cylindrical TPC act as MultiWire proportional Counters (MWC) for fast signal analysis. Individual slats or subsectors can be viewed as pixels in $\eta - \phi$ space for analysis. Each of the trigger detector systems has multiple channels as shown in Tables 1-3. We have recently added a portion of the Barrel Electromagnetic Calorimeter (BEMC) which provides energy localization of $\delta\eta \sim 0.05$ and $\delta\phi \sim 0.05$ (high towers) and patches of $\delta\eta \sim 0.2$ and $\delta\phi \sim 0.2$ (tower sums) to the STAR trigger, suitable to selection of electrons and photons. The algorithms of Level 0 (see below) generate $\delta\eta \sim 0.8$ and $\delta\phi \sim 1.0$ patches suitable for jet selection. Each detector channel is digitized for every RHIC crossing and fed into a Data Storage and Manipulation (DSM) board where it is analyzed and combined with the other signals in a multi-layer pipeline that forms a fast decision tree.

Output from the DSM tree is fed to the Trigger Control Unit (TCU) where it is combined with detector status bits to act as an 18 bit address to a lookup table (LUT) which holds the trigger word that goes with each bit combination. The trigger word then acts as an address into the Action Word LUT which holds the information on which detectors are to be involved and what action is to be taken for this trigger. This DSM-based decision tree constitutes Level 0 of the trigger and is constrained to issue a decision within 1.5μs from the time of the interaction. When an interaction is selected at Level 0, each STAR detector designated to participate in this type of event is notified using a 4-bit Trigger Command and told to identify this event with a 12-bit token[1].

While the amplification/digitization cycle is proceeding in the slow detectors, the fast detector information is gathered by VME processors and examined in a coarse pixel array (CPA) at Level 1. The cells of Level 1 have $\delta\eta \sim 0.5$ and $\delta\phi \sim \pi/2$, suitable to respond to gross spatial symmetries in particle distributions typical of beam-gas background, which could lead to Level 1 aborts. Interactions not aborted by Level 1 continue their data acquisition cycle while the raw trigger dataset is collected in the memory of one of several CPUs that constitue the Level 2 farm. This raw data set forms a fine pixel array whose pixels are of suitable size for jet isolation or for refinement of particle topologies useful in selecting specific interaction mechanisms. Both the coarse and fine pixel arrays are expected to be subjected to shape analysis in event selection. When an interaction is accepted at Level 2, the trigger system notifies the central Data Acquisition (DAQ) system and relinquishes control of the proto-event to DAQ.

Data flow through the trigger pipeline is controlled via a 12-bit token, which is issued for each interaction that is accepted at Level 0. This token guarantees that the resources are available in the trigger system to complete a Level 2 decision to abort or to hand off the event to DAQ within 5ms of the occurance of the interaction. All of the raw trigger detector data and the results from Level 1 and Level 2 analyses are packaged and sent to DAQ with the token. The token stays with the event and is used as an identifier within DAQ to organize collection of all the fragments from each STAR detector. Once DAQ either accepts and stores the event or aborts it, the token is returned to the trigger and recycled.

This paper describes the requirements that led to the STAR Trigger design, the detectors involved at the fast trigger levels, and the electronics and connection to the run control system. We show results obtained during the 2000 and 2001 running periods during which we took many types of physics and calibration triggers. We conclude with a discussion and summary of the trigger performance.

2 Requirements

The requirements that drove the design of the STAR trigger are summarized below.

- Select central collisions in AA and pA interactions based on charged particle multiplicity in the TPC acceptance. These involve the largest number of nucleons and are expected to maximize collective effects.
- Select ultra-peripheral collisions. These represent specific elementary processes which may be enhanced in AA collisions.
- Select jet events. Jets reveal internal structure.
- Select events based on bunch polarization. Polarization porvides a sensitive probe of spin structure.
- Select Cosmic Ray events. Useful for system debugging and calibration.
- Adapt to new physics. To explore new territory and select specific rare interactions.
- Operate for pp, pA, and AA interactions. The STAR research program investigates such interactions for spin and QGP (Quark Gluon Plasma) studies.
- Issue triggers when requested by different STAR detectors. Necessary for calibration of individual detectors.

- Accomodate new detectors. To support STAR's vigorous upgrade program.
- Reject background. Expect beam-gas rate of $\sim$100 Hz at maximum luminosity.
- Minimize trigger related deadtime. Maximize beam use.
- Open TPC amplifier grid in $< 1.5\mu$s. Lose 2% of the data per μs delay.

These requirements led to the development of the fast detectors and pipelined electronics system described below.

3 Trigger Detectors

There are four primary trigger detectors for STAR: CTB, ZDC, MWC, and BEMC (described elsewhere in this volume). We expect to add a Beam-Beam Counter (BBC) in the near future to cover the high η region necessary for normalizing event rates in the pp program. We also expect to add a Forward Pi0 Detector (FPD) to measure polarization, and an Endcap Electromagnetic Calorimeter (EEMC) to complement the BEMC.

3.1 The Central Trigger Barrel (CTB)

The CTB consists of 240 scintillator slats arranged in 4 cylindrical bands each covering 1/2 unit of pseudo rapidity. The CTB slats cover the outer shell of the 4m diameter TPC as shown in Figure 2. Details of the CTB are shown in Table 1. Each slat consists of a radiator, light guide, and mesh dynode photomultiplier tube (PMT - Hamamatsu R5946). The slats are housed in aluminum trays to ease handling and mounting on STAR, with two slats end-to-end in each tray. The PMTs are attached to the radiators using ultraviolet-transmitting acrylic plastic light guides. The scintillator is wrapped in DuPont Tyvek B1060 and the light guide in black construction paper. The narrow edges of the light guide are painted black to reduce the flash from particles close to the PMT and to remove reflections in the slat. Each PMT is powered by a channel of LeCroy 1440 high voltage and has an independent light-emitting diode (LED) attached to the far end of the slat for calibration purposes. Each PMT sends a single anode signal through 100 feet of RG58 cable to a CTB Digitizer Board (CDB).

The slats were tested with partially collimated cosmic rays uniformly distributed over the slat. The width of the ADC response to cosmic rays is 25%, in reasonable agreement with simulation. The largest single contribution to this measured width is the calculated 16% variation in scintillator response. The wrapping scheme achieves a signal uniformity over the slat with an RMS of 6% as determined by testing with a source.

Each CDB has 16 input channels, as shown in detail in Table 4. The input signals go to a gated integrator and 8-bit ADC (2.4 pC per count sensitivity) and to a discriminator. The discriminator sets an output, called the timing bit, whenever it detects a signal greater than its threshold whose leading edge lies within a narrow time window. The integrator gate signal and the discriminator time-over-threshold pulse are available on an external connector for testing and for use by other detectors. [3] Each CDB channel sends 8 bits of information, normally the 8-bit ADC value, to a DSM board input channel. The timing bit can be routed to become the least significant bit of the 8-bit output, a feature that facilitates a fast count of the number of slats hit in any interaction. Timing in the CDB is controlled by the RHIC Clock, a trigger-wide distributed clock. The integrator gate, discriminator threshold, timing bit window width and offset, and LED are all controlled via VME settable registers.

3.2 Zero Degree Calorimeter (ZDC)

Each of the RHIC experiments constructed a pair of Zero Degree Calorimeter detectors to provide the accelerator operators a common tool for monitoring interactions at each region. These are placed at nearly identical positions along the beamlines on either side of the intersection regions. Each ZDC [4] consists of three modules. Each module consists of a series of tungsten plates alternating with layers of wavelength shifting fibers that route cherenkov light to a PMT (see Table 2). The ZDCs are used for beam monitoring, triggering, and locating interaction vertices.

The ZDCs operate as fast detectors for the STAR trigger. The anode signal from each PMT is routed to a linear fan-in module, with one output routed to a CDB channel; a second output routed through a 14 dB attenuator and into another CDB channel; and a third output routed to second linear fan-in channel, where it is added to the signals from the other two PMTs in its ZDC. One copy of this sum is sent to a CDB channel and another copy is attenuated by 14dB and sent to another CDB channel. The hadronic minimum bias trigger requires a coincidence between the two STAR ZDCs of summed signals greater than $\sim 40\%$ of a single neutron signal.

An output from the linear fanout for the first PMT in each ZDC is sent to a NIM discriminator whose output is used to start a constant current source. The current source is stopped by a signal from the RHIC clock each crossing. The current is directed to a channel of the CDB where its value is digitized to provide a measure of the time at which the PMT was hit. Comparison of the times from ZDCE and ZDCW gives a measure of the interaction location. Many of our triggers cut on the location of the interaction vertex being within $\sim$25 cm of the center of the TPC.

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[3] Both the RICH and the TOFp use the CDB discriminator outputs to form an independent multiplicity sum.

[4] NUCL-EX:0008005[2]

3.3 Multi-Wire Counter (MWC)

The MWC is not a separate detector, but simply uses the TPC anode wires as a fast detector. Details of the MWC are shown in Table 3. The primary function of the TPC anode wires is to provide (avalanche) gas gain for the clouds of electrons that drift through the gas volume and are admitted through the gating grid. The images of these avalanches form the pad signals used for tracking in the TPC. Ionization from charged particle tracks that pass directly through the anode wire region also avalanches onto the wires. These signals can be used to measure the multiplicity of such tracks, which is useful for Level 0 trigger formation. The electronics used to process these "prompt" signals must 1) provide a low AC impedance for the wires to prevent the wires from "bouncing" and injecting signals into all the pads under them; 2) produce a logic level signal for each minimum ionizing track with good efficiency (threshold $<$0.5 MIP); and 3) perform numerical calculations to derive multiplicities within the Level 0 trigger logic timing constraints (1.5μs).

The STAR MWC Front-End Electronics (FEE) uses a variant of the Star Shaper Amplifier (SAS) with resistive feedback to provide an always-alive preamplifier (not gated) ([3]). The electrons in this region take more than 100 ns to drift onto the wire for amplification, leading to signal shapes longer than a single RHIC crossing. Thus, interactions in one crossing may overlap into successive crossings. The electronic shaping time was matched to this drift time to maximize efficiency. The shaper outputs are fed directly to fast comparators whose logic-level outputs are sent to a sector control board via twisted pair flat cables. Here Field Programmable Gate Arrays (FPGAs) are programmed to latch the bits (one bit per wire), count the number of wires hit, and format the data for transmission to off-chamber receiver modules via gigalink optical fibers. The Receivers combine FEE card multiplicities into subsector multiplicities, 80 wires per subsector, and pass the data to the Level 0 DSM tree. All these functions are performed in synchrony with the RHIC clock.

4 Electronics Design and Implementation

4.1 Trigger Level 0

Approximately 350 bytes of data from the CTB, ZDC, and MWC come into the Level 0 system every bunch crossing (i.e., every 107 ns), and another 450 bytes are expected from the BEMC when it becomes operational in 2002. Additional data coming into Level 0 includes the LIVE/BUSY status bits from the other detectors, any requests for calibration triggers, and information from RHIC (including number and fill status of each bunch). In Level 0, the raw data from each detector are analyzed to determine whether a requested type of interaction occurred in this crossing. Level 0 issues a trigger within 1.5μs of the occurrence of the interaction if it detects a requested signal and the detectors are LIVE. If it does not detect an interesting signal, it can issue calibration triggers for any LIVE detectors requesting them, or it can simply wait for the next crossing.

The description of an interaction often requires the detected particle multiplicity and the distribution of these particles in η, ϕ space. This description involves summing the number of hits on the CTB slats and the number of hit MWC wires. The digitization and summing process takes longer than the 107 ns between bunch crossings. To minimize deadtime in the trigger we designed a pipelined synchronous system based on custom VME modules.

There are four types of custom boards in this system, as well as the CDB and MWC receiver boards discussed above. These are the Data Storage and Manipulation (DSM), the Trigger Control Unit (TCU), the Trigger Clock Distribution (TCD), and the RHIC Clock and Control (RCC) boards. All of these are 9U VME boards that are controlled by the RHIC clock, whose period is the time between bunch crossings.

Level 0 analysis uses a tree of DSM boards. Each board receives new data every RHIC clock tick, performs a simple calculation (eg., a part of the sum), and passes the result to the next DSM board in the tree in time for the next RHIC clock tick. The tree narrows to one DSM board, which passes the final results to the TCU.

The TCU board looks at the results for each bunch crossing and issues trigger commands to the rest of STAR. The trigger commands and token are transmitted to another VME crate, which houses the TCD boards, one for each detector system (TPC, SVT, etc. ...). The TCD boards are the interface between the trigger and the detectors. The RCC board receives the RHIC clock from RHIC and distributes it, with the correct (register set) phase, to all the DSMs and the TCU. When no RHIC clock is available, a local oscillator takes over to act as the trigger heartbeat.

There are four layers of DSM boards in the Level 0 system, as shown in Figure 3. Details of the DSMs are shown in Table 5. Every board receives a RHIC clock from the RCC and 128 input data bits from other sources, in eight 16-bit channels. The data bits can come from another DSM, a CDB, or a receiver board. The data is latched onto the DSM board on the rising edge of every RHIC clock tick, where it is used to address eight 16-bit look-up tables. These tables enable the user to get quick results from a calculation on each set of 16 bits (for example, subtracting a constant pedestal from each ADC value and normalizing the gain).

The output data from the eight look-up tables is saved in a circular buffer large enough to contain complete data sets for 64k crossings. Simultaneously the data is input to an FPGA, which takes $\sim$half a RHIC clock tick to analyze its input data (eg., summing the hits). On the rising edge of the next RHIC clock tick, as the next set of data is latched into the DSM board, the FPGA result is latched off the DSM board and driven to another DSM board or to the TCU. Once a trigger is issued, the data must be gathered from the DSM boards that contributed to that trigger decision. That data has been stored in the circular input buffer pipeline, and the memory location specified by the token for this event is read out using a VME64 transaction many crossings later.

The final DSM board passes its data to the TCU. There is only one TCU in the STAR trigger system, and it is the only part of the system that can issue a trigger. This board is in a VME crate with the DSM boards in Layers 1-3 of the DSM tree. The TCU receives the RHIC clock from the RCC as input, and it also receives 12 output bits from the last DSM board and six live/busy status bits from six possible slow detector systems (systems that require longer than one RHIC clock tick to digitize their data). The data is latched onto the TCU board on the rising edge of every RHIC clock tick.

The 18 bit TCU input is used as an address for the 16 bit Trigger Word look-up table, whose output is used to classify the type of each interaction. Details of the TCU are shown in Table 6. A set of many different combinations of input bits can all point to the same trigger type or trigger word. For example, all combinations of input bits that indicate that the TPC is LIVE and that a high multiplicity event occurred could be given the trigger type of 1, independent of what the other bits are.

The 16 bit Trigger Word is used as an address to access the pre-scale system and the Action Word look-up table. The pre-scale system allows the TCU to select only a pre-determined fraction of each trigger type. The Action Word look-up table is loaded with a list of which detectors should be triggered for this Trigger Word (e.g., just the TPC, or the TPC and SVT, etc. ...) and what action those detectors should take (e.g., normal digitization and readout, calibration procedure, etc. ...). Just as each detector produces a single LIVE bit, each detector responds to a single ACTION bit. When a trigger is issued, one of the tokens is attached to that event. The token stays with that event as it moves through the trigger system, and is not returned to the TCU for reuse until the event is completely processed (aborted or stored) by DAQ.

If the event is selected, then a trigger is issued. The Action Word, Trigger Word, token, and a copy of the RHIC strobe are passed to the TCD crate for distribution to the detector subsystems. The data is also stored in three output FIFOs on the TCU with the input from the last DSM board and the LIVE bits. The FIFOs are read by the Level 1 Control CPU (L1CTL), which starts the next stage of trigger processing to run in parallel with the digitization cycle of the slow detectors.

If there is no new trigger to issue on the current crossing, then the TCU can issue Abort or Accept commands concerning events that were triggered earlier and are currently being digitized and stored by various slow detectors. These commands are produced by Levels 1 and 2 and are sent to the TCU where they are loaded into the Response FIFO for distribution to the TCDs.

Each TCD board consists of a standard mother board and a mezzanine card that is customized for the individual detectors. There is at least one TCD board for each detector subsystem. Every TCD board takes the trigger information from the TCU as input. The RHIC strobe that is part of the trigger information latches the 96 bits from the TCU onto the TCD boards. Each board decodes the Action Word at every crossing, and when a TCD board sees its detector ACTION bit set, the customized mezzanine card takes the appropriate action for that detector subsystem to handle that trigger command.

A second input to each TCD board comes from a front-panel connector into which a BUSY signal from DAQ can be plugged. This signal is ORed together with an internal hardware BUSY signal that is generated by the TCD board itself to cover the digitization time of that detector's front-end electronics. The combined BUSYturns off the LIVE signal that is passed from the TCD to the TCU through the VME crate to crate connection.

4.2 Trigger Levels 1 and 2

Once a trigger is issued, there is a period of several milliseconds during which the selected detectors are busy digitizing their data. This period allows time for more detailed analyses of the trigger data to determine whether the event meets more finely grained criteria. If it does not, then the digitization process is aborted, freeing the detectors for a new trigger. The analysis is split into two pieces that roughly match the digitization phase and the data transmission phase of the TPC: Level 1 with a time budget of $\sim 100\mu$s and Level 2 with a budget of $\sim$5 ms. Level 1 works on a subset of the trigger data that is stored in the input buffers of the DSM boards in the TCU crate, the coarse pixel array in η,ϕ space.

The Level 1 system also contains a control section, responsible for the overall flow control of events that pass through the trigger system. If an event is not aborted by the Level 1 analysis, it is passed to Level 2. Level 2 uses the full trigger data set, including the raw data that forms the fine pixel array. Again, the event can be accepted or aborted. If the event is accepted, both the detector subsystems and DAQ are notified. Levels 1 and 2 are implemented in several Motorola 2306 VME CPUs. The CPUs are linked together by an SCI ring and are connected to DAQ by a SCRAMNET link.

5 Run Control

The trigger is operated through the STAR Run Control (RC) system. The run control system for the trigger consists of three layers: a graphical user interface (RC Client), a message handler, and a set of trigger server tasks. The RC Client provides an interface for the user, gathers configuration parameters, and generates configuration files. Its components include a message browser, an interface to view the run log browser, an interface to add free-form comments to the run log, an interface for viewing and modifying run parameters, and an interface for controlling runs.

The Handler is the interface to the trigger subsystem. It distributes run control commands and parameter files generated by the RC client to each of the trigger processors and writes the run parameters to the online databases.

The trigger server tasks run on MVME 2306 processors and communicate with the handler via ethernet. Each server task receives commands from the handler, processes them, and then returns a state and status to the handler. In the event of an error, the task returns a string that contains the reason for the failure. The configuration of the trigger follows a multi-tiered scheme. Tier 1, a static binary file internal to the trigger system, contains the low-level programming of the trigger hardware, the DSM and TCU boards, and the FPGAs on those boards. Tier 3, a binary file generated by RC Client, contains a list of parameters and values that define the trigger, including the name of the Tier 1 file. The Tier 3 file is the entire configuration information structure that is passed to the trigger by run control. Tier 2 is a documentation file that contains a description of the information provided in Tier 1 and the meanings of the Tier 3 parameters. A complete description of the trigger conditions for any data set can be constructed from the Tier 2 documentation and the Tier 3 parameter files stored in the run database.

6 Performance

During the 2000 and 2001 running periods, STAR has used a number of different triggers, as shown in Table 7. The simplest trigger used the RHIC clock and triggered whenever the detector was alive. Our "Hadronic Min Bias" trigger required a coincidence between the two ZDC detectors, ZDCE•ZDCW. ZDCE and ZDCW refer to the analog sum of the three PMT signals from the East and West detectors and indicate that these signals exceeded some threshold, typically $\sim 40\%$ of the single neutron peak. The "Central" collision trigger took two forms: one required signals in both ZDCs and in the CTB to exceed some thresholds, while the other relied on the CTB alone being above a very high threshold. This was to account for the fact that the ZDC signal was small for the very highest multiplicity collisions, and we wanted to make sure that we sampled the full multiplicity range presented.

In addition, we used special triggers to collect pedestal values, create laser tracks in the TPC, and test all of the electronics for the TPC, FTPC, TRG, RICH, pTOF, FPD, BEMC, and SVT.

The central (CENT) and hadronic min bias (HMB) triggers were based on neutrons detected in the ZDCs and on charged particles detected in the CTB. The correlation between these signals is shown in Figure 4 for data that passed all of the trigger and analysis cuts that required tracking to point to a good central vertex for the interaction. In terms of impact parameter, the figure shows that there is a region of strong forward neutron production during which there are few charged tracks produced in the CTB (region I, characterized by $\sum CTB \leq 1500$), followed by an anti-correlation in ZDC vs.CTB signals (region II $1500 \leq \sum CTB \leq\sim 20000$), and ending in a region (III $\sum CTB \geq\sim 20000$) of high charged particle multiplicity with low neutron signal. These are interpreted as large impact parameters in region I and very small impact parameters (central collisions) in region III.

Extrapolating minimum ionizing tracks from the TPC onto CTB slats indicated that a typical minimum ionizing particle (mip) in the center of a slat gave a signal of 5 counts. In 2000 we used a simple ADC sum to indicate multiplicity, while in 2001 we used a combination of ADC sum and MIP sum in which the ADC values were converted to MIP counts. A histogram of the CTB multiplicity for tracked events triggered by the CTB above a low threshold gives the CTB Multiplicity distribution. For the CENT trigger the cut for threshold 2 was at 2000 and for threshold 3 was at 6000 MIPs.

The ultra peripheral collision (UPC) program has so far required the greatest flexibility in our trigger, although we expect the spin program to hold that distinction soon. The UPC trigger divides the CTB into 16 sections, four in ϕ by four in η, just like the coarse pixel array. It then makes use of the DSM look-up-tables (LUT) to map 8 bit ADC values into mip counts, taking out the lowest order bit which is packed as the timing bit by the CDB. It then asks for back-to-back pairs of hits looking at the geometry of the CTB and selects collisions in which there are 2 or 4 tracks which have characteristic back-to-back geometry, eliminating high multiplicities and highly asymetric events. The UPC trigger also vetoes events having hits on the top ($-\pi/4 < \phi < \pi/4$) or bottom ($3\pi/4 < \phi < 5\pi/4$) of the TPC , since these are dominated by cosmic rays. When these conditions are met the UPC bit is set and sent to the TCU. Using this trigger, the UPC group has found a large enhancement in reconstructable resonances compared to a similar number of events taken with just a low multiplicity trigger.

7 Conclusions

The STAR trigger used signals from the CTB and ZDCs during the 2000 and 2001 AuAu runs at $\sqrt{S_{NN}} = 130$ GeV/nucleon and $\sqrt{S_{NN}} = 200$ GeV/nucleon respectively to study minimum bias, peripheral and central collisions, and to provide calibration and test triggers for the TPC, FTPC, TRG, RICH, pTOF, FPD, BEMC, and SVT detectors. We expect to augment our trigger detector set with the MWC, a Beam-Beam array, and more of the BEMC detector in the coming run to extend our coverage in eta and to explore the capabilities made available by the new detectors.

References

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Table 1
Central Trigger Barrel (**CTB)**

Parameter	**Description**
Purpose	Measure charged particle multiplicity in $-1 < \eta < 1$.
Coverage by single slat	π/30 in ϕ; 0.5 in η
Average occupancy	10/slat for central AuAu interactions
Multiplicity (M) measurement accuracy	$<$3% at M$>$1000 ; single hits at low M
Channels (slats)	240
Radiator	BC408 : 1 cm $\times$ 21 cm $\times$ 112.5 or 130 cm[5]
Light detectors	Hamamatsu R5946 PMTs

Table 2
Zero-degree Calorimeter (**ZDC)**

Parameter	**Description**
Purpose	Verify centrality in AuAu collisions, provide hadronic minimum bias signal, and provide interaction signal for RHIC operation.
Average occupancy	$\sim$25 neutrons for central AuAu collision
Channels (modules)	6
ADC (PMT amplitude)	8 bits, 2.4 pC per count
Radiator	PMMA fibers with W plates
Light Detector	Hamamatsu 2490-05 PMT

Table 3
Multi Wire Counter (**MWC)**

Parameter	**Description**
Purpose	Measure charged particle multiplicity in $-2 < \eta < 1$ and $-1 < \eta < -2$.
Cell coverage	Variable in η and ϕ
Average occupancy	0.1 - 0.2 per cell in central AuAu
Multiplicity (M) measurement accuracy	$<$3% at M$>$1000 ; single hits at low M
Channels	96 from 24 sectors each having 4 subsectors of 80 wires. The 7200 wires are fed in groups of 20 to front end boards, summed to 5 bits each and then sent to receiver boards where they are grouped by subsector forming 96 sums sent to Level 0

Table 4
CTB Digitizer Board (**CDB)**

Parameter	**Description**
Purpose	Digitize signals at 10 MHz rate and provide logic level when signal exceeds threshold within time window.
Input	-2.0V $<$ signal $<$ 0.0V
Channels	16
Integrator	20 ns to 80 ns window
Range	8 bits, 2.4 pC least count
Discriminator	15 mv minimum threshold, time-over-threshold output
Timing bit	set when discriminator output within time window
Time window	10 ns to 60 ns

Table 5
Data Storage and Manipulation Boards (**DSM)**

Parameter	**DSM**
Input bits	128
Output bits	32
Gain correction and pedestal sub LUT	8 - 16 bits wide
Cyclic buffers for storing input data	8 - 16 bits wide $\times$ 64k deep
Level 0 Algorithms	1 FPGA
Output FIFO (tree alignment)	2k $\times$ 32 bits

Table 6
Trigger Control Unit (**TCU)**

Parameter	**TCU**
Input bits from DSM trees	12
LIVE bits (from TCDs)	6 [6]
Input counter	2 - 256k $\times$ 32 bits
Trigger word LUT	256k $\times$ 18 bits
Trigger word counter	2 - 65k $\times$ 32 bits
Prescale table/counters	2 - 65k $\times$ 32 bits
Token FIFO	4k $\times$ 12 bits
Response FIFO (to TCD)	4k $\times$ 28 bits
Accepted trigger information FIFO	4k $\times$ 60 bits

Table 7
Triggers 2001

Hadronic Min Bias	[ZDCE ≥ 5 + ZDCW ≥ 5] + CTB ≥ 75
High Mult	CTB ≥ 33000
UPC	Topology bit
Hadronic Central	[ZDCE ≥ 5 + ZDCW ≥ 5] + [Vertex cut] + CTB ≥ 2000 mips
High Mult	CTB ≥ 6000 mips

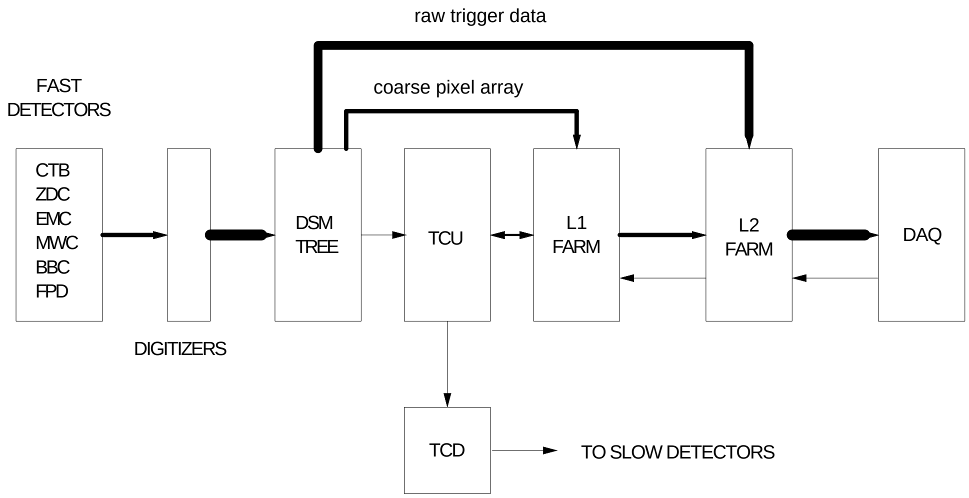

Fig. 1. Data flow through the trigger. See text for definition of acronyms.

Central Trigger Barrel

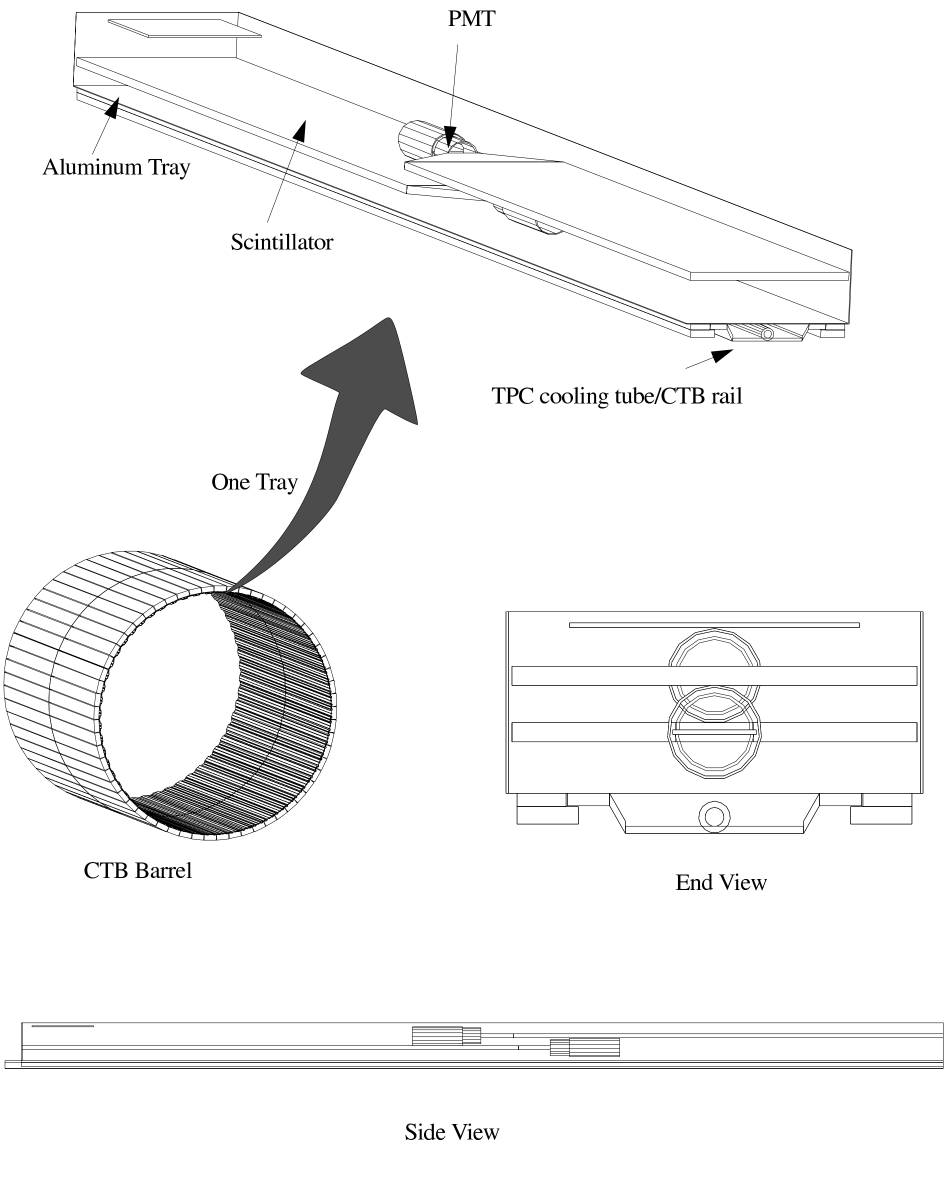

Fig. 2. CTB cylinder and detail of tray and slat.

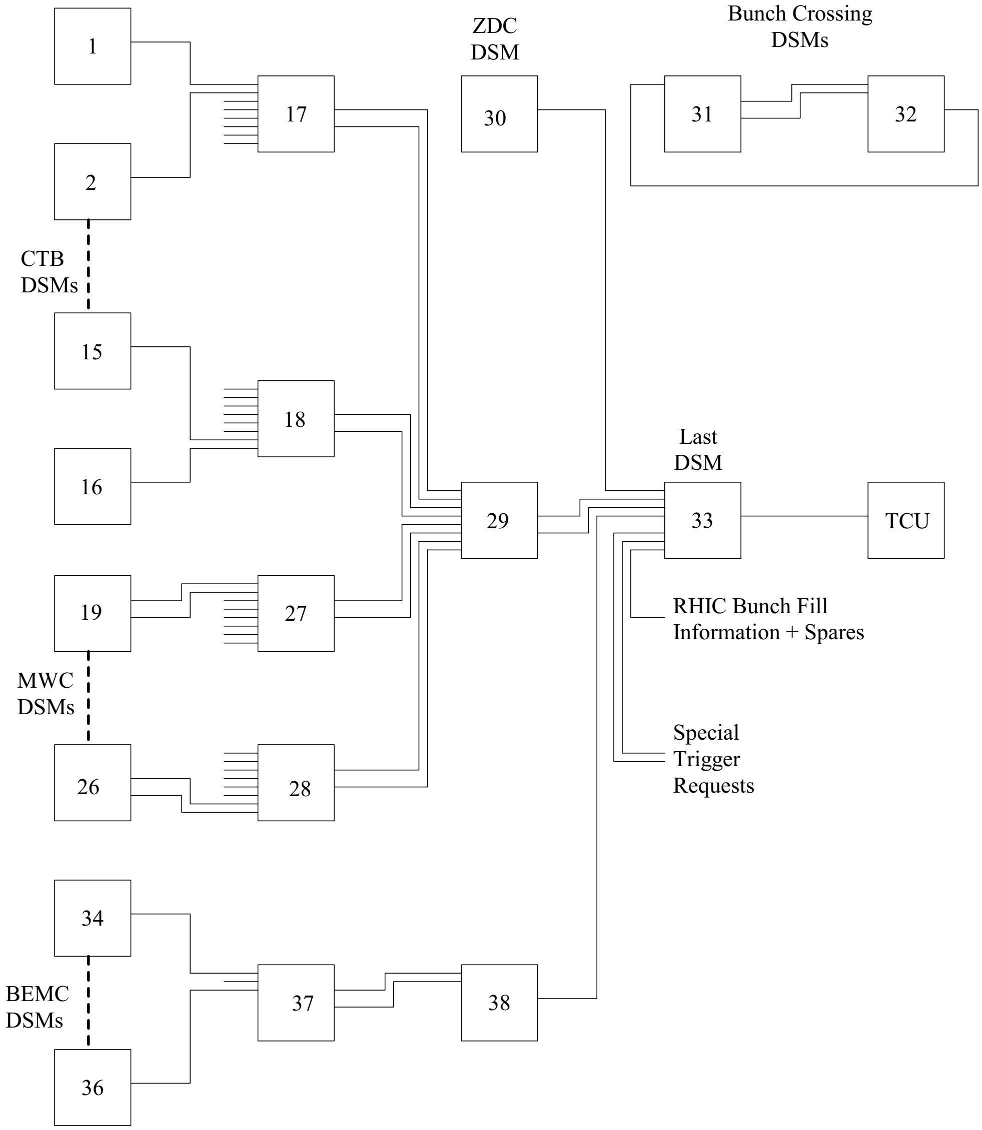

Fig. 3. DSM tree as set up in 2001.

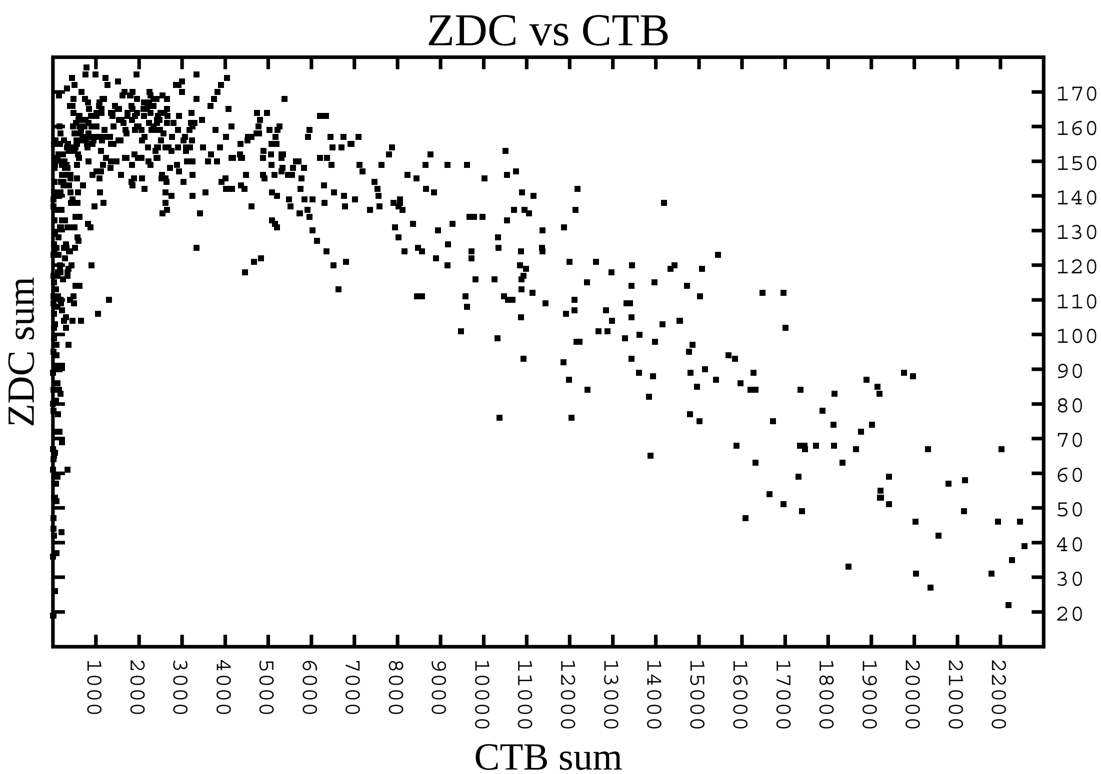

Fig. 4. ZDC-CTB correlation showing 3 regions.