last update 031210

Startup:
000. Some software checks;
- 1.definition of all DSM registers in list and for GUI
- 2.verify GUI info going to correct register for critical ones
  - (BBC small ADC threshold (bb001 – BB004)
  - threshold for BBCE,W in BB101
  - threshold for ZDCE,W in ZD101
  - BBC delta T min and max in VT201
  - ZDC delta T min and max in VT201
- 3.DSM tree logic
- 4. CDB files , BDB files
- 5. V124 setup (from Angelika D)

00. DAQ checks
- 1. run trigger detectors with DAQ and check output files
- 2. run each detector with DAQ and trigger and check output files

0. Some signals to check:
- 0. check timing of TRGPD cables into DAQ room
- 1. GLINK connections to and from daq room and platform
- 2. alignment of blue and yellow fill signals – use blue PET to align
- 3. yellow, blue, and rev-tick on platform
  - see page XX in Logbook YY
- 4. check alignment of all CDB gates for CTB, BBC, ZDC
- 5. check each bit coming into TCU from last DSM
- 6. check that ZDCW1 signal and gate and ZDCE1 signal and gate
  - are being shipped to daq room from driver board
- 7. check gate widths and vary using CDB config files
- 8. measure TAC sensitivity

1. PMT HV
- start with “best guess” demand file for CTB, BBC, ZDC
- HV files: /export/home/users/sysuser/epics/R3.12.2-LBL/TRGhvApp/src

2. ADC gate timing – use Yellow timing as driver
- check ZDC E and W coincidence
- vary yellow bit timing (fine delay on PET page)
  - check gate and signal relative timing on oscilloscope
  - get edges of ADC range response – select PET settings
  - establish ZDCE.W coincidence using fiber signals
    - see page XX in Log YY
- use ZDC coincidence to trigger scope and look at:
  - BBCE gate with BBCE1 signal
  - determine time from leading edge to signal

use BBC TCD phase delay to change, not PET
set TCD delay to get signal at front of gate
measure earliest start and latest stop for BBCE1 TAC
wrt BBC1 ADC gate
earliest start should come ~12ns following
leading edge of BBCE1 signal
OK to let gate trailing edge act as stop

3. DSM alignment
   check that ZDC, BBC and CTB all fall in same
   crossing in data stream
   (want cookbook for this procedure)
4. Blue/Yellow bits
   time these into the trigger
   start with all buckets “on” in PET page
   need PET manual for operation
   then remove to reveal “real” fill pattern
5. TAC range
   check range of TAC – should be <250 channels max
   if gate stop is too late, need to set delay on TAC stop
   to reduce range (needs access)
6. Check calibration of ZDC and BBC
   check single neutron peak in ZDCs, mip peaks in BBC
   allign all TAC edges so TAC minimum works for vertex
   correlate BBC vertex with L3 vertex
   correlate ZDC vertex with L3 vertex
7. Find “earliest hit” for each TAC channel
   histogram TAC values , decide on “early” edge
   set LUT so this earliest hit maps to same max value
   for each channel
8. Diamond definition
   check diamond shape using TAC
9. Min bias definition
   check consistency of all layers of DSM input
   check consistency of TCU input bits with DSM tree layers
   investigate vertex definition using ZDC and BBC
   decide which detector works best for each centrality
10. Scalers
    check definition of each scaler channel
    check readout and file integrity
11. CTB setup
    check noise in pedestals
    check timing bit setup