STAR Trigger TAC Board – Current Status

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## History

The original design for the STAR Trigger system included two detectors that just needed to produce simple energy deposition information (Central Trigger Barrel and Zero Degree Calorimeters) and one that needed high precision energy and timing information (Vertex Position Detector). As a result of funding issues the development of the VPD and its associated electronics was cancelled. However, the CTB and ZDC were built, and a digitizer board (CDB) was developed to digitize their signals and produce the necessary ADC values. The discriminator outputs from each channel were driven off the board to be used for monitoring and other purposes.

Several years later the Beam-Beam Counters were added to the experiment. These detectors needed time information as well as energy. However, the funding to develop a high-precision ADC/TDC module was still not available. The compromise solution was the Time-to-Analog board (TAC). This board would accept the discriminator outputs from the CDB and use the leading edge of each signal to start a current source. All the current sources would be stopped at the same time. The duration of the current for each channel would therefore be equal to the time between the leading edge of the discriminator signal and the common stop. The currents could then be fed back into unused channels of the CDB, integrated and digitized, effectively producing TDC values.

The TAC boards were developed and have been used in STAR for many years now. Please see Figures 1, 2 and 3 at the end of this document for a block diagram, a description of the timing circuit and a timing diagram for the flow of data through the TAC. Over the same time period the original CDB boards were all retired and replaced with a new digitizer board; the QT board. The discriminator outputs from the QT boards use a different voltage standard (PECL) than the original CDB boards (ECL), but the TAC boards still use the original standard. So an interface board is currently used to convert the QT discriminator outputs back to the original ECL standard.

A new ADC/TDC module is now being developed by Blue Sky as part of an SBIR project. It may be implemented as a new daughter card for the QT boards, in which case it could fit easily into the existing STAR system. However, both the form factor and the schedule for completion are currently uncertain. Various upgrade detectors are due to be installed in STAR in the next few years. Some of them require that the resolution on the vertex position measured by the Level 0 trigger be good enough to select events within 5 cm of the center of STAR. Achieving this resolution should be possible with the new electronics from Blue Sky, however if those modules are not ready in time it may be necessary to make do with the existing TAC boards for an intermediate period of time.

Our experience with the TAC boards over the years has brought to light some problems with the mechanical and electrical design. In addition, the boards are aging, part failures are becoming more common and acquiring replacement parts is becoming more difficult. This document summarizes the current status of the known mechanical and electrical problems with the TAC boards. The final section describes three possible upgrade scenarios for improvements to these TAC boards.

## Mechanical Issues

1) The board is physically the wrong shape. It needs to fit into the rear card cage of a STAR Trigger standard VME crate, which has a P3 backplane with long pins. The board needs a cut-out to

enable it to connect to P2 without interfering with P3. That cut-out was not implemented for the TAC PC board, so currently the shape has to be cut out by hand after manufacture.

2) In order to make the boards work a LARGE number of patches are necessary: parts need to be added by hand in difficult locations. For example, some additional resistors need to be loaded on top of existing parts. This makes the boards much harder to load, debug and maintain.
3) The two potentiometers cannot be reached when the board is installed, so adjustment has to involve unplugging the board. Space on the front panel is taken up by the RHIC clock connector and the local delay jumpers, which typically do not need to be accessed more than once during setup. It would be more convenient if those connectors were moved off the front panel, further into the board, and the two potentiometers were located so they were front-panel accessible.
4) The RHIC clock connector is currently a 20-pin connector, of the type used when receiving signals from a Trigger Clock Distribution board (TCD). During 2011 the TCD modules for fast trigger detectors, and their TAC boards, will be removed. The TAC boards will then receive their clock signals from the new RCC modules, which drive 10-pin cables, not 20-pin.

Electronic Issues

1) The board is somewhat unstable, leading to the situation where the behavior of one circuit is time and location dependent. The circuit in question is the summing circuit, and the instability can be seen in the potentiometer setting. In the original design there was no potentiometer in this circuit, just appropriate resistors. It was not possible to get the circuit to behave properly with resistors, so the adjustable potentiometer was introduced. When first installed the potentiometers work properly. However, as they age they become overly sensitive to small changes in their setting, or the temperature, and their behavior drifts. It is not possible to adjust the potentiometer settings once the boards are installed at STAR. So, setting them correctly involves a cumbersome procedure for adjusting the setting outside of STAR, installing and checking the boards at STAR and then iterating until the boards behave correctly. The lifetime of the potentiometers appear to be only a few years, so they all have to be checked and re-set every year and typically one or two have to be replaced. The problem could be due to a number of different problems:
    a. Part selection, layout or grounding plane issues.
    b. Issues of dealing with both ECL and PECL (and their different voltages) on the board.
    c. An un-detected fundamental problem with the circuit design
    d. All of the above.
    e. Others…

    Ideally it would be best to find and fix the source of the instability so the potentiometer could be removed from the summing circuit and replaced with fixed resistors.
2) The TAC board was originally designed to work with the ECL discriminator outputs produced by CDBS. It had to receive those ECL signals, and a PECL clock, and then produce (in parallel to the current outputs) PECL outputs. Since the two standards use different voltages (+5V vs -5V) there is a significant amount of complexity in the circuit design for dealing with generating and distributing these different voltages, and translating signals between the two standards. This could be the source of some of the instability referred to above. The CDBS have now been replaced by QT boards, which produce PECL discriminator outputs, not ECL. A separate card is used to translate the PECL QT outputs to ECL so they can feed the TAC boards, which ultimately translate them back to PECL. This has resulted in significant un-necessary complexity and extra noise in the system.

3) The circuit that produces stretched outputs is not protected against out-of-time hits, i.e. hits that come while the current source circuit is being reset. This means some stretched outputs have no corresponding current output. Also the length of the stretched output signals is not guaranteed to be at least 50ns (this guarantee was one of the original requirements). The summing circuit, which sums the stretched outputs, is therefore also not protected from late hits and can give an erroneously high sum. Over the years various users have adapted to use this feature. At a minimum the situation should be reviewed to see what the current generation of users needs.
4) The discriminators on the CDB and QT boards are not high precision devices so consequently they add to jitter on the time measurement. In addition the long path that the discriminator signals take through the FPGA on the QT daughter cards, through the mother board, an interface card and various driver chips also adds to the jitter. A scheme in which the detector signals are split upstream of the QT boards and one branch goes directly to TAC boards that include high precision discriminators could significantly reduce the jitter and improve the timing resolution of the board. This scheme could also reduce the latency through the TAC system, so the current outputs would get back to the QT boards for digitization earlier. This would effectively increase the range of the timing measurement.

Upgrade Scenarios

1) Minimal Effort
   The TAC circuits would be kept essentially the same. All of the known patches would be integrated into the design, and the layout of the board would be re-done. The new layout would include the cut-out to avoid the P3 connector. The existing 20-pin clock connector would be replaced with a 10-pin connector. Only two of the pins are actually used, so this change has no effect on the rest of the board. Also, the new clock connector, the local delay jumpers and the potentiometers would be relocated so the potentiometers could be adjusted from the front panel.

2) Moderate Effect
   All of the changes described in the Minimal Effort section would be implemented. The TAC input circuits would be re-designed to receive and process PECL inputs instead of ECL. The requirements for the stretching circuit would be reviewed to see if the existing feature (see Electronics Issue #3) should be kept, modified or eliminated. Any necessary changes to how the stretched outputs are set and reset would then be implemented. Once this was done, the summing circuit would also be checked to see if it could be stabilized enough to remove the need for the potentiometer.

3) Maximum Effort
   All of the changes described in the Minimal Effort section would be implemented. In addition, the input stage would be fundamentally changed. The circuit would be re-designed to receive PMT signals as input instead of discriminator outputs. A high precision discriminator would then be implemented for each channel, and its output would then drive the existing current output, stretched output and sum output circuits. The current output would still be fed into the QT boards for digitization. This new design would entail splitting the PMT signals upstream of the QT boards, with one branch still going to the QT boards and the other branch going to the TAC

boards. As part of this larger re-design, the form factor for this board would also be re-considered to see if there is a better way for it to fit into the STAR trigger system, e.g. convert it to a front-of-crate card instead of a back-of-crate card.

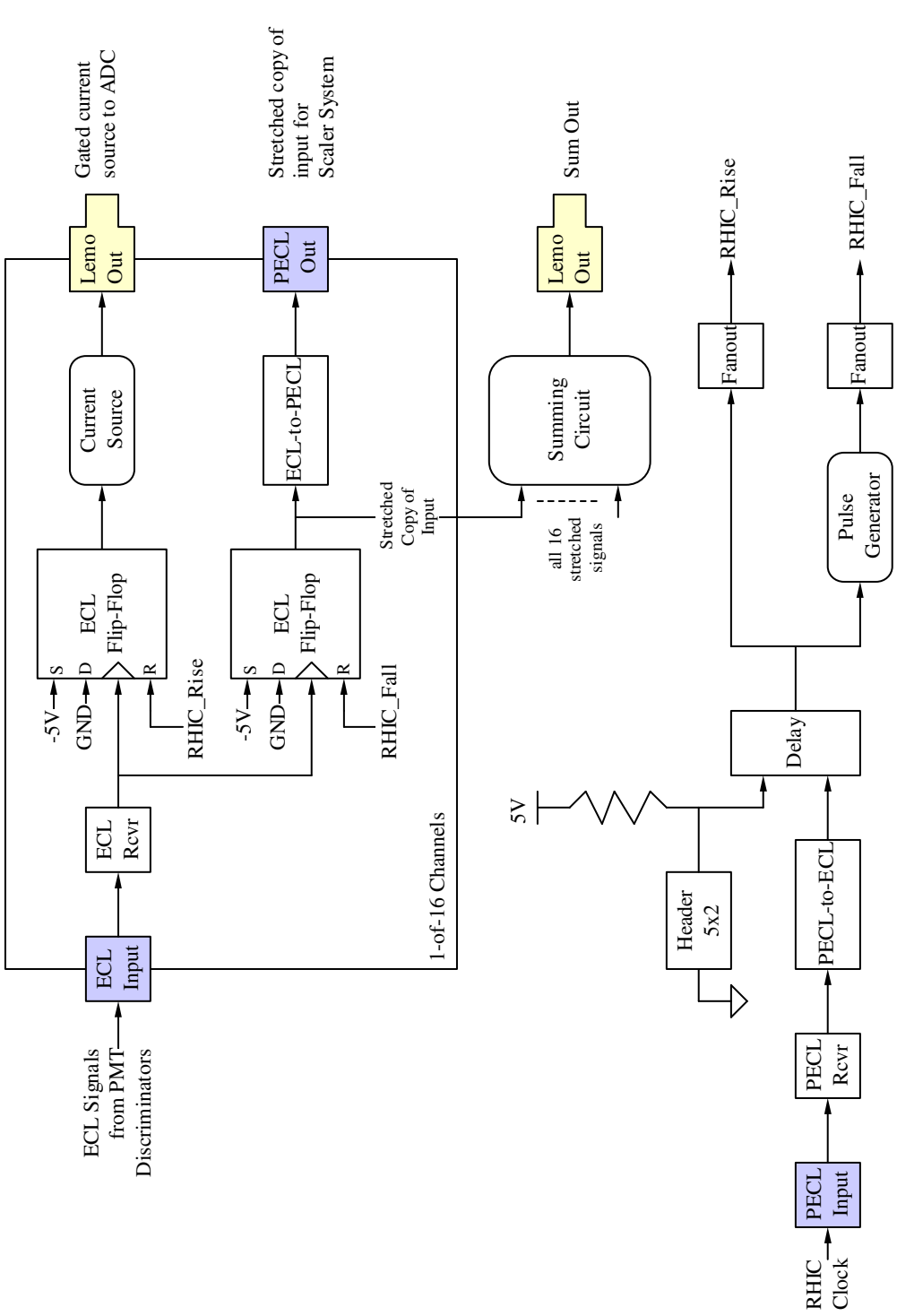


Figure 1: Block Diagram of the STAR Trigger TAC Board

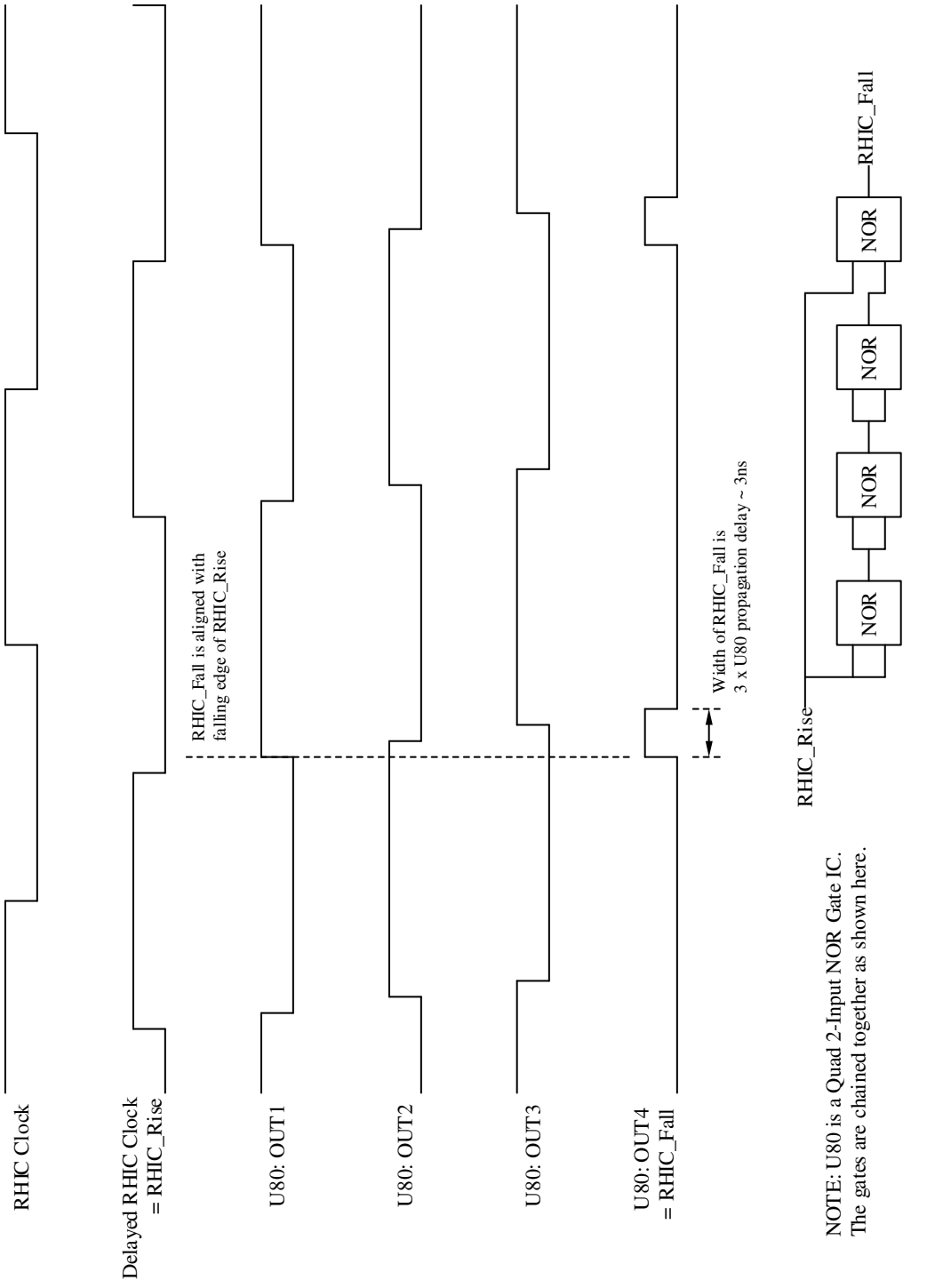


Figure 2: Timing Circuit of the STAR Trigger TAC Board

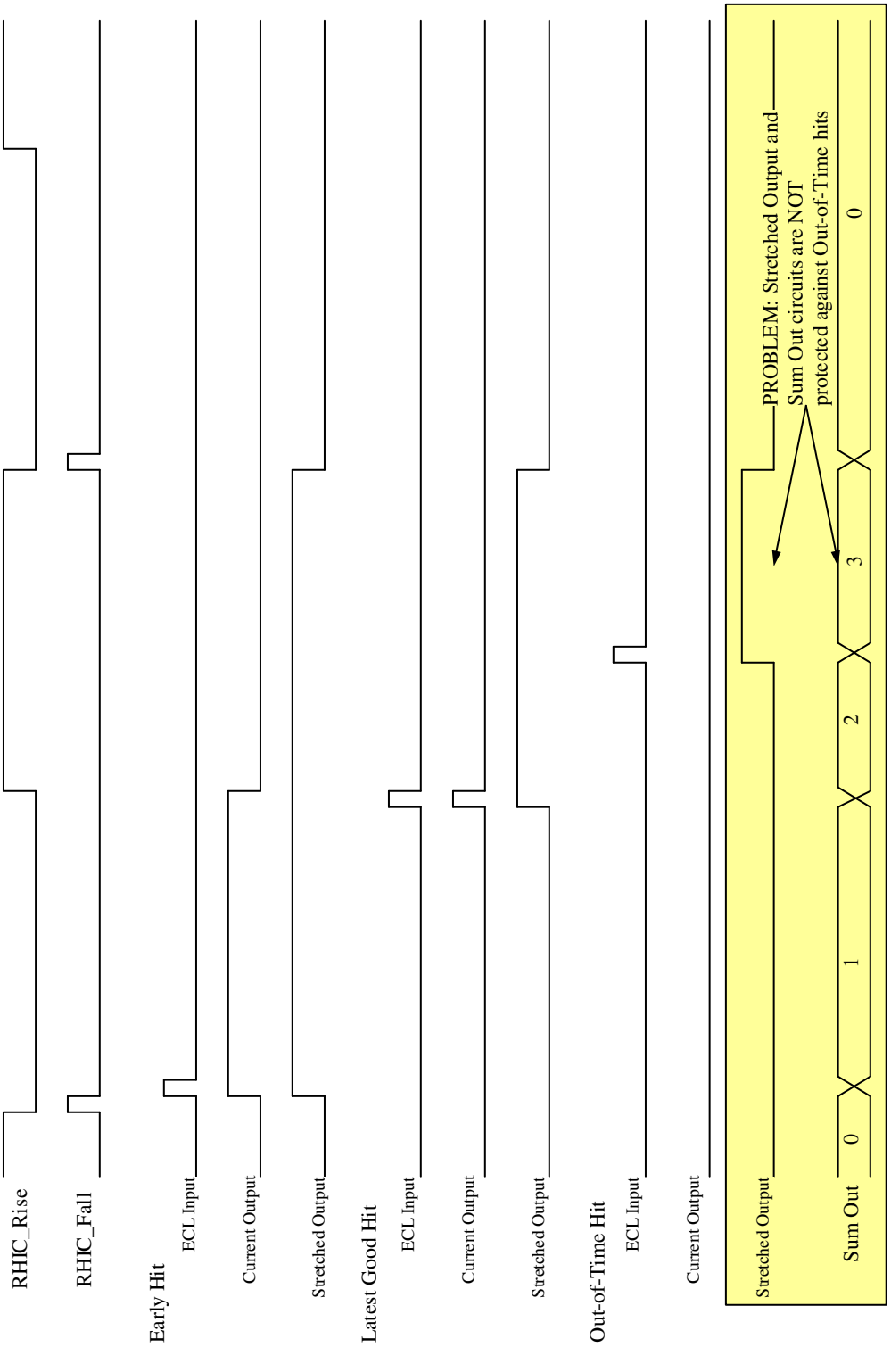


Figure 3: Timing Diagram for Data Flow in the STAR Trigger TAC Board