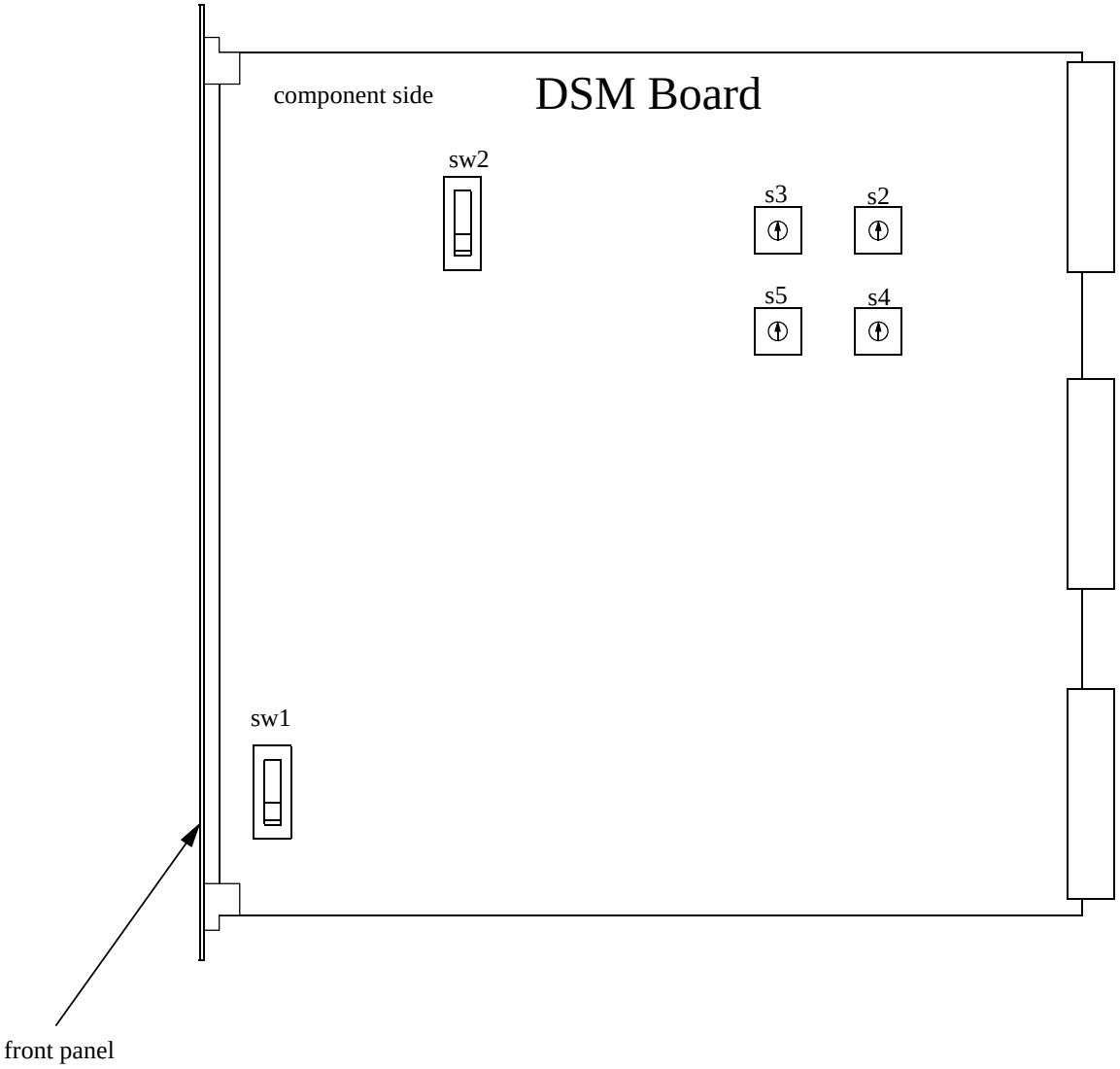

SW1 - selects how the board configures the FPGA engine algorithm, from a prom or over the VME backplane. SW1 up selects from a prom. SW1 down selects from VME.

SW2 - selects the board clock. This switch should always be in the down position.

s4, s2 - select the VME base address of the board. s2 is the LSB, s4 is the MSB. For example, if you wanted the board base address to be 0x1f000000, s4 should be set to 1 and s2 should be set to f. *

s3, s5 - select the base address of the chain block transfer. s3 is the LSM. s5 is the MSB. For example, if you wanted a CBLT address of 0x20000000, s5 should be set to 2 and s3 should be set to 0.

* please see the STAR Trigger VME Base Address document for setting addresses of DSM and other VME boards.

SIZE	REV	DRAWING #
A		

DWN BY: Leo Greiner	DATE: 9/29/99	SCALE	UC Berkeley - Space Sciences Laboratory Crawford Group
COG. ENG.: Leo Greiner	DATE	DO NOT SCALE DRAWING	TITLE: DSM Hardware switch settings
ALL SCREW THREADS PER ANSI 14.6 BREAK EDGES 0.020 MAX ON MACHINE WORK. REMOVE BURRS, LOOSE SCALE AND WELD SPLATTER REFERENCE - ANSI 14.5 & B46.1		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE INCHES DECIMAL TOLERANCES .X = ±0.06 .XX = ±0.02 .XXX = ±0.004 ANGULAR TOLERANCE ± 1 DEG.	