RCC2 VME Memory Map
January 8, 2016

ID: Name	Address	Functionality	Access
0: Firmware revision	0x YY00 0000	0xabcdmmnn - Major and Minor revision	R
1: Firmware date	0x YY00 0004	0xdayymmdd – Date of this revision	R
2: Mode selection	0x YY00 0008	0 = Slave mode 1 = Master mode (power-on default)	R/W
3: Input Selection	0x YY00 000c	0 = Local oscillator (power-on default) 1 = TTL Clock 2 = RHIC clock from V124 3 = 10-pin PECL connector clock 4 = Fiber connector clock	R/W
4: Clock error behavior	0x YY00 0010	0 = Auto-switch on error to local oscillator clock (power-on default) 1 = No automatic switching	R/W
5: Clock error period	0x YY00 0014	D(0:15): Clock period that produced an error	R
6: Clock error status	0x YY00 0018	D0 = Clock period above high threshold D1 = Clock period below low threshold NOTE: Valid for selected clock only	R
7: Reset clock error status	0x YY00 001c	D0: Reset	W
8: Run/Stop	0x YY00 0020	0 = Stop (power-on default) 1 = Run	R/W
9: Address Latch	0x YY00 0024	D0: Generate address latch pulse	W
10: Spare 1	0x YY00 0028	Spare control level	R/W
11: Test Pulse Trigger	0x YY00 002c	D0: Generate test pulse	W
12: Global delay	0x YY00 0030	D(0:7): Global delay in ½ ns steps	R/W
13: Clock delay	0x YY00 0034	D(0:7): Clock delay in ½ ns steps	R/W
14: Test Pulse Delay	0x YY00 0038	D(0:7): Test pulse delay in ½ ns steps	R/W
15: Group 1 Delay	0x YY00 003c	D(0:7): Group 1 delay in ½ ns steps	R/W
16: Group 2 Delay	0x YY00 0040	D(0:7): Group 2 delay in ½ ns steps	R/W
17: Group 3 Delay	0x YY00 0044	D(0:7): Group 3 delay in ½ ns steps	R/W
18: Group 4 Delay	0x YY00 0048	D(0:7): Group 4 delay in ½ ns steps	R/W
19: Group 5 Delay	0x YY00 004c	D(0:7): Group 5 delay in ½ ns steps	R/W
20: Group 6 Delay	0x YY00 0050	D(0:7): Group 6 delay in ½ ns steps	R/W
21: Group 7 Delay	0x YY00 0054	D(0:7): Group 7 delay in ½ ns steps	R/W
22: Group 8 Delay	0x YY00 0058	D(0:7): Group 8 delay in ½ ns steps	R/W
23: Group 9 Delay	0x YY00 005c	D(0:7): Group 9 delay in ½ ns steps	R/W
24: Group 10 Delay	0x YY00 0060	D(0:7): Group 10 delay in ½ ns steps	R/W
25: Test Pulse Voltage	0x YY00 0064	D(0:11): DAC value	R/W
26: Test Pulse Rate	0x YY00 0068	D(0:15): Free-running test pulse rate	R/W
27: Test Pulse mode	0x YY00 006c	0 = Off 1 = Free-running 2 = Single shot	R/W

28: RESET	0x YY00 0070	D0: Reset all settings to power-on default	W
29: Local Address Control	0x YY00 0074	D0: Reset to zero D1: Copy current value to CSR30 D2: Increment by one.	R/W
30: Read Local Address	0x YY00 0078	D(0:15): Address counter value, 16 LSB	R
31: Read Local Address	0x YY00 007c	D(0:15): Address counter value, 16 MSB	R
32: Clock period low threshold	0x YY00 0080	D(0:15): Minimum prescaled clock period in units of 66 MHz clock ticks	R/W
33: Clock period high threshold	0x YY00 0084	D(0:15): Maximum prescaled clock period in units of 66 MHz clock ticks	R/W
34: Clock period	0x YY00 0088	D(0:15): Clock period in units of 66 MHz clock ticks	R
35-39: Reserved for future use	0x YY00 008c: 0x YY00 009c	TBD	R/W
40: Fiber Rx Refclk Select	0x YY00 00a0	0 = 20 MHz oscillator (power-on default) 1 = 18.766 MHz oscillator	R/W
41: Fiber Rx Control	0x YY00 00a4	D0 = BISTEN: Built-In Self Test Enable D1 = RF (Reframe Enable)	R/W
42: Fiber Rx Status	0x YY00 00a8	D0 = Fiber Rx SD (Signal Detect) D1 = RVS (Received Violation Symbol) D2 = SC/D* (Special Char/not Data)	R
43: Reserved	0x YY00 00ac	TBD	R/W
44-47: Reserved for Fiber Tx Control/Status	0x YY00 00b0: 0x YY00 00bc	TBD	R/W
48: Flash Memory Data Input FIFO	0x YY00 00c0	D(0:7): Data to be written to the flash memory	W
49: Flash Memory Data Output FIFO	0x YY00 00c4	D(0:7): Data read from the flash memory	R
50: Flash Memory Bytes	0x YY00 00c8	D(0:15): Number of bytes to be read from or written to the flash memory	R/W
51: Flash Memory Start Address – 16 LSB	0x YY00 00cc	D(0:15): 16 LSB of address to start reading/writing	R/W
52: Flash Memory Start Address – 8 MSB	0x YY00 00d0	D(0:7): 8 MSB of address to start reading/writing	R/W
53: Flash Memory I/O Control	0x YY00 00d4	D0: Reset Input FIFO D1: Reset Output FIFO D2: Enable write access D3: Disable write access D4: Read Identification D5: Read Status Register D6: Write block protection bits D7: Start a write access D8: Start a read access D9: Erase one sector D10: Erase whole flash memory	W
54: Flash Memory Status	0x YY00 00d8	D0: Write-in-progress bit (WIP)	R

		D1: Write Enable Latch bit (WEL) D(2:4): BP0-BP2, the block protect bits D(5:6): Unused, always zero D7: Not implemented D8: Data Input FIFO empty D9: Data Input FIFO full D10: Data Output FIFO empty D11: Data Output FIFO full	
55: Flash Memory Block Protection	0x YY00 00dc	D(0:2): BP0-BP2 Define which sets of sectors are write-protected	R/W
56: Flash Memory Sector	0x YY00 00e0	D(0:3): Sector to be erased	R/W