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Requirements for QT32D digitizer mother boards

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The QT boards, measuring charge and arrival time for fast analog signals entering four 8 channel daughter cards (DC), were originally designed for use with the Forward Meson Spectrometer, an electromagnetic calorimeter, which set many of its requirements. It was adapted for vertex position measurements using an external back-of-crate board (TAC) that yielded a <50ps TDC capability in its QT32B mother board (MB) incarnation, using QT8B daughter cards. This high precision TDC was internalized in the QT8C daughter cards which used the QT32C version of the mother board for the Event Plane Detector (EPD), providing a higher precision ~25 ps TDC. The QT32Cs are now used for the Beam-Beam Counter (BBC), Vertex Position Detector (VPD), Zero Degree Calorimeter (ZDC), and Muon Telescope Detector (MTD). All of these are designed to be Fast detectors used in establishing triggers for STAR.

This document describes the requirements for a new mother board (QT32D) to be compatible with both QT8B and QT8C daughter cards to provide point-to-point readout capability to provide event readout at >20kHz rates by eliminating the VME CPU and backplane in the readout process. Note that many of these requirements match the details of the existing QT Memory Map.

Requirement 1. Clock : The MB must accept a STAR standard clock or an internal oscillator, register selectable.

Justification: The board needs to operate with a STAR standard clock for synchronization with all other trigger electronics. We use the RCC2 to synchronize local memories on each board using the RCC2 run/stop line. These signals are distributed on P3 from the RCC2. The board must incorporate a local oscillator for testing.

Requirement 2: Signal capture: Up to 80 ns active gate for signal capture time.

Justification: Signal development in the various detectors and variation in vertex location within the interaction diamond lead to signal arrival times at the input to the QT8 daughter cards spread over up to 50 ns. The signal width adds to this to allow capture of the full charge in the pulse.

Status: The MB controls the gates for each of its 4 DCs based on the arrival time of its clock. It uses 2 registers to set gate width: a register that sets the delay with respect to the leading edge of its clock signal for the START and another register for the STOP. These delay lines have 1ns granularity and 255 ns full range.

Requirement 3: LED indicator: A Front panel LED will indicate which clock is active.

Justification: useful in testing and checking operations.

Status: - we agree that an LED indicating the board is in RUN mode would be useful, but there may not be front panel space. We will look into a multi-color single LED to convey more information.

Requirement 4: Discriminator thresholds: A single threshold will be used for all input channels on a board. The range will be from 10mv to 100 mv.

Justification: Signal amplitudes are expected to be roughly gain-matched prior to entry to the QT DCs. The discriminator signals from each channel are used to start the local 5ns TDCs and to provide scaler monitoring of hits in each channel. Since neither of these functions requires finer than 5ns time stability of the discriminator output a single threshold for each board is sufficient. The 5ns TDC is useful for background rejection.

Requirement 5: Output to scalers : The MB must drive the scaler bits used by both flavors of DC to VME P2.

Justification: This is how bits are sent to the scaler system. The QT8B board sends a discriminator signal for each channel. The QT8C board sends a discriminator signal for the first four channels (the input signals), a logical OR of the discriminator signals, and a spare output. The MB should be able to handle each of these DCs and send the appropriate scaler signals.

Status : The first six bits from each DC can be sent out on P2 in the same way that was done on QT32B and QT32C. On QT32C, the highest two bits in the MB-DC connectors were converted to provide an additional voltage rail to the DC so a scheme must be developed to choose between sending the scaler bits from QT8B or providing 1.2V to QT8C. In addition, on QT32C, the highest bit on P2 was converted to a TAC Stop Input signal. A similar scheme must be developed to choose between sending this scaler bit from QT8B or receiving a TAC Stop on QT8C. It may be difficult to include jumpers for each B <-> C change, so will see if these can be accomplished using configurable register settings.

Requirement 6: DC Flavor indicator: Will need a register to check which flavor of DC this MB is set up to use.

Justification: We need to be able to tell remotely whether a board is configured correctly for the daughter cards it is using.

Requirement 7: Rate capability: operate at 10 MHz.

Justification The STAR trigger is based on a fully pipelined dead-time-less operation allowing maximum use of the luminosity and keeping a local record of each crossing's input and FPGA calculation result. The local memory increments at the RHIC Strobe (RS) speed of ~10 MHz.

Requirement 8: Interface to STAR Trigger Level0 (L0) : Provide at least 32 bits of output from the QT32D FPGA driven on the outer rows of the P3 backplane

Justification: This is how bits are sent to the trigger decision tree

Status: We may want another output from this board using an SFP+ fiber but there may not be room on the front panel for a port. It may also be possible to multiplex multiple sets of 32 bits out if necessary, but this is not a requirement.

Requirement 9: Output latch delay: a register will be provided to specify delay of output from QT board to P3. Sensitivity of 5ns is sufficient.

Justification: This allows alignment with other detector information going to L0.

Requirement 10: Maximum output delay from interaction: The board must present its values to L0 within 400 ns (4RS) of the interaction.

Justification: The QT board requires a minimum of 2 RS to complete its digitization cycle. The additional 2 RS allow for routing timing.

Requirement 11: VME Reset: The board can be reset via standard VME sysreset command or via ConnectCore command.

Justification: In this way we can reset a crate without power cycling. Using sysreset allows us to reset a full crate with a single command. This will cause the FPGA to be reloaded from its prom.

Requirement 12: Local memory: Require at least 8 MB of circular memory per QT board.

Justification: The easiest local storage is to use circular memory leading to a requirement of 32 chn x 4 B/chn/xing x 64k xing (7 ms worth) => 8 MB of local storage. Each channel would store its ADC and TDC value for each crossing.

Status: We also want to store locally the result of any FPGA calculations for each crossing and have an option for reading this information out as well. The board will have ~500 MB of local memory. We will continue discussion of how much circular memory to use. Note that the bunch ID used to address the circular memory is already produced as 32 bits in the TCU although currently we use only 16 bits.

Requirement 13: Readout Command : Each QT32D board should receive the trigger system Build_Event command directly from L0 via the STP2 network over a front panel fiber port.

Justification : By receiving the Build_Event command directly on the QT board, each board can begin readout as quickly as possible and in parallel with other QT boards. The

QT boards record at least 7ms worth of data in a circular buffer before that data is overwritten so readout should be done as quickly as possible after a trigger is issued to avoid stale memory readout. Receiving the readout command directly is also faster than the scheme used on previous versions of the MB, which allows for higher maximum trigger rates.

Requirement 14: Input Memory Readout : Each QT32D board should send triggered data directly to L2 via the STP2 network over a front panel fiber port.

Justification : Memory readout for a given token is initiated upon receiving a Build_Event command from L0 as described in a previous requirement. The QT32D board should send data directly to the L2 CPU via the STP2 network over a fiber port located on the front panel of the board. This is in contrast to previous versions of the board in which data was readout by a VxWorks CPU over the VME bus and then sent to L2 via STP over the PCI bus. The fiber port to STP2 should be the same port as used for receiving the Build_Event command in requirement 13. Sending data directly to L2 from each board allows for faster readout, as well as simultaneous parallel readout of multiple boards, which allows for higher maximum trigger rates.

Requirement 15: Memory synchronization: Use an OR of (RUN/STOP signal from RCC2) with (contents of a register) to set the board into run mode.

Justification: This will allow all QT board memories to be synchronized so that the "correct" crossing information can be selected for a given trigger. Allowing a register to put the board in run mode makes debugging much easier. Because we want the register to be able to force two states: RUN and STOPPED (over-riding the RCC2 signal) two bits are required: one to say "obey RCC2 or local" and one to say RUN or STOP when in local mode.

Requirement 16: Readout time monitoring : A timestamp of when readout occurs should be sent along with the data.

Justification : The QT boards have at least 7 ms worth of circular buffer space available before data is overwritten by the next crossing. A timestamp of when the readout of a trigger occurs can be compared to the time that the trigger happened, as provided by the TCU, to determine if the QT data was readout in time. This timestamp will be a counter that is reset at the start of a run and that increments with each RHIC clock tick so that it stays in sync with the rest of the trigger system. In previous versions of the board, there wasn't sufficient FPGA capabilities to do this onboard the QT so a worst-case readout time was provided by reading out the timestamp from the RCC2 board after the readout of all QTs in a crate was done. A more powerful FPGA on the QT32D should provide the capability to do this directly onboard and thus provide a more accurate readout timestamp which will allow for higher maximum trigger rates while still guaranteeing that the data was readout before being overwritten.

Status: The QT32D uses an Artix7 FPGA which is much more powerful than the Spartan 3 FPGA of the original QT boards. The newer FPGA can easily provide this monitoring capability.

Requirement 17: Readout rate: The QT32D must be capable of readout rates in excess of 20 kHz.

Justification: The goal for the STAR upgrade is to allow readout rates in excess of 20 kHz. We do not want the readout of trigger information to significantly affect that rate.

Requirement 18: Zero-suppression: Register selectable option.

Justification: Most events have only a few hits, so data sparsification is reasonable. Each channel uses 4B per event (12 bit ADC, 5 bit TDC, 5 bit channel address, 10 spare bits). With zero-suppression, we decrease the payload from as much as 128B to as little as 4B of input information readout for each event. We need to require full readout for pedestal calculations.

Requirement 19: Monitoring: Front panel Test points for gate and clock.

Justification: It is useful to be able to see the relation of the clock and gate as they appear at the input to the digitizer.

Requirement 20: Test input: Inject a fixed charge into each front end for testing.

Justification: This will simplify board testing.

Status: The amplitude and rate of input pulse are register settable for each MB.

Requirement 21: Form factor: The board will be a 32 channel extended 9U VME board.

Justification: This sets the number of crates required for the full complement. “Extended” means that the board should measure 400mm from the front panel to the backplane, which is longer than the standard VME size-D length of 340 mm.

Requirement 22: Configuration and Board Monitoring : The board should be configurable over a standard Ethernet port located on the front panel.

Justification : An Ethernet interface with each board allows for configuration and monitoring (ie reading and writing registers) using standard off-the-shelf ethernet equipment. Previous versions of the board used a VME interface for configuration and monitoring which required the procurement and maintenance of outdated and slow MVME processors. This requirement, along with the direct receipt of the Build_Event command and direct readout to L2 allows for these processors to be eventually removed from the trigger system.

Requirement 23: Crate mix compatibility: The QT32D must be able to operate in a VME crate with older QT32B and QT32C boards.

Justification: We do not intend to replace all existing boards.

Brief description:

Analog signals enter daughter cards where they are split, with one path going to an integrator and the other path going to an edge-sensitive discriminator. Their charge is integrated for the duration of the specified gate and this charge integral is digitized using a 70 MHz 12 bit ADC that operates at 60 MHz.

Output from the discriminator is used as input to a 5ns sensitivity time-to-digital-converter (TDC). The TDC is based on a counter operating at 21x RHIC clock speed (~200 MHz) and counts the interval between the discriminator signal and the next leading edge of the clock. This leads to a 5 bit TDC value which is stored and reset at the leading edge of each RHIC clock signal.

ADC and TDC values for each channel are stored in a STAR-standard circular memory. The memories arealigned to 0 when the boards are put into run mode. They are addressed by the bunch crossing number of the triggered event modulo the total circular buffer size.

The FPGA will route each channel's digital signals to local memory for storage until receipt of a trigger. The FPGA will then read the crossing-specified memory locations for each board and ship the data via STP2 fiber optic cable to a PCIe receiver card in a linux CPU.