Requirements for RCC Upgrade
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This document describes the requirements that need to be met by the new RHIC Clock and Control (RCC) unit for STAR. This replacement module is motivated by the need for a more robust clock distribution, as the number of STAR detectors has grown and their electronics is no longer confined to the platform, and by the need to maintain multiple boards, which is now impossible for the current 15 year old design. Each module will be able to act as master or slave in distributing the 3 necessary lines: experiment CLOCK, RUN, and LATCH.

We are currently thinking of this module as consisting of 2 boards, one for the front-of-crate (FOC), and one for the back-of-crate (BOC). All of the active components will be on the RCC-FOC Board, including individual channel delays. The distribution channels will be on the RCC-BOC board. Communication between the FOC and BOC will be through the 64 usrdef lines of a standard VME P2 backplane. The RCC-FOC board will accept RUN, and LATCH signals through the front panel, or (for the master) via VME, or Ethernet. The RCC-FOC board will accept CLOCK signals through the front panel or from an onboard oscillator. The front panel will include a copper connector of the same form factor as used in distribution, to allow a MASTER to control many SLAVES or CUSTOMERS, as well as a standard fiber-optic connector with a brain for SERDES operations.

1. Requirement: Master/Slave: The board must be able to operate either as the master source of clock and control signals, or as a slave for distributing these signals.
Justification: We want to have a single board design to minimize board proliferation and provide spares.

2. Requirement: Form factor: The RCC-FOC must be a 6U VME module, preferably using only the +5V line for power. The RCC-BOC must be 6U and 27.4 cm long and notched to clear P3/J3 connector.
Justification: All of STAR's trigger electronics is housed in VME crates. The only unpopulated slots in many of the crates which will be required to house a RCC module are 6u. RCC-BOC must be of the same length as current BOC cards (e.g. DSMI, QT-BOC) to fit existing card cage.

3. Requirement: VME standards: The board must respect all VME backplane communication standards including 64Bit transfer operations and SYSRESET.
Justification: We need to operate in a standard VME environment with other VME modules including DSMs. We want to be able put the modules into their initialized state without using the power cycle.

4. Requirement: Configuration: The board must be configurable over Ethernet or over VME. The ROC-FOC front panel should allow access to a JTAG connection to allow the initial downloading of code into the FPGA, and a serial connection to configure the Ethernet interface.
Justification: We want to use these boards in VME crates and in stand-alone applications.

5. Requirement: Copper I/O standard: Signals distributed over copper will be PECL.
Justification: To be compatible with existing input requirements on client boards.

6. Requirement: Optical I/O: The RCC-FOC board must also accept fiber inputs and the RCC-BOC board must be capable of driving fiber outputs.
Justification: For some of the distant detectors (e.g. FMS, FPD-east, etc) it is much more robust to use fiber-optic links.

7. Requirement: CONTROL inputs: The board must be able to accept RUN and LATCH signals as input from Ethernet or VME, or from the front panel through connectors that have the same form factor as is used to distribute the RUN, and LATCH to other systems.
Justification: the RUN and LATCH signals are generated on the MASTER board on command from the Run Control via Ethernet or VME. Requiring that the board can also accept these signals through the front panel in the same format that is used for distribution will allow us to chain multiple boards together.

8. Requirement: CLOCK input: The board must accept an input clock of ~10 MHz in 4 different form factors:
   a) Differential input via BNC twin-ax connector
      Justification: The RCC Master must receive the input RHIC clock signal from V124 module via the SMR and SMTX fiber MAU units.

   b) PECL via 10pin IDC connector
      Justification: We need to have an input path for the RHIC clock for slave RCC modules that is compatible with the output from the RCC-BOC card. Existing RCC-BOC clients (e.g. DSMI, QT-BOC, etc.) require 10pin IDC.

   c) TTL via lemo connector
      Justification: We want to use this in tests where a clock is provided by a signal generator.

   d) SERDES via multimode fiber
      Justification: need the ability to supply RHIC clock and RC control signals to remote locations (see requirement 12).

9. Requirement: Internal CLOCK generation: The board must be able to generate a local clock of frequency ~10 MHz (>9.4MHz). A local clock of 66 MHz for running the FPGA and other board control is also required.

Justification: We want to use this in various test setups, and the board needs to run in standalone mode for setup and testing.

10. Requirement: clock selection: the input clock must be selectable
Justification: With five possible clock sources, we must be able to remotely control and monitor which clock is selected at any given time.

11. Requirement: clock integrity: The board must check the selected input clock integrity and have the ability to issue a STOP command when the clock misses more than a register-settable number of pulses, or fall over to the local clock and issue a warning. Both STOP and warning commands must conform to STAR standard ethlib protocols.
Justification: We need to keep the experiment clock reliable to keep our synchronous system operating correctly and be notified if a failure has occurred.

12. Requirement: Global Clock delay: An FPGA controlled digital delay line must be between the CLOCK-SELECT point and the CLOCK-FANOUT point to allow gross phase changes with a sensitivity of at least 10 ns over a range at least as long as the RHIC clock period.
Justification: This will allow us to align the clocks on slave RCC boards that receive their clock signals from the master over cables of significantly different lengths.

13. Requirement: Individual Clock Delays: The RCC-FOC must produce at least 9 copies of the selected clock, each of which can be individually phase-adjusted using an FPGA-controlled digital delay line. The delay lines must have a granularity of no more than 1ns over a range that is at least as long as the RHIC clock period.
Justification: To allow phase alignment for each client module (e.g. DSM, TAC). The granularity and range are set by the needs of the TAC boards. The minimum number of different phases is set by the BBQ crate, which needs 9 different clock phases: one for the QT boards and one for each of the eight TAC board.

14. Requirement: Cycle-to-cycle Jitter: The typical cycle-to-cycle jitter introduced in each copy of the selected clock by the RCC-FOC must be no more than 100ps.
Justification: This is set by the needs of the TAC boards. Once the current set of STAR upgrade detectors are installed, STAR would like to trigger on primary collision vertices within 5cm of the center of STAR. The vertex position is determined from the difference between two TAC measurements. The resolution of the TAC difference measurement is limited by the jitter between the clocks driving the TAC boards. If the RCC-FOC introduces no more than 100ps of jitter into each output clock, than the maximum jitter between TAC clocks is ~140ps which corresponds to a 4.2cm jitter on the vertex position measurement.

15. Requirement: output distribution: The RCC-BOC board must make up to 20 copies of the CLOCK, RUN, and LATCH signals available for local distribution.
Justification: A STAR crate has between 4 and 17 modules that need synchronous clocks including QT, DSM, and TAC boards.

16. Requirement: Clock-Control Relative Timing: In both Master and Slave modes, the RCC FOC-BOC combination must maintain the same relative timing between the output clock and the control signals that is produced by the existing RCC/RCF boards.
Justification: The firmware in the existing DSM and TCU modules expects that relationship between the incoming clock and control signals, and that firmware cannot be altered at this point.

17. Requirement: Test pulse: The RCC FOC must produce a PMT-like pulse with fixed amplitude of no more than -2V and a fixed width no less than 10ns. The pulse should be generated once per tick of the test-pulse-clock. That clock would be another phase-adjusted copy of the selected clock, prescaled to a frequency in the range 100 kHz to 1 Hz. The test pulse should be driven off the board on a lemo connector.
Justification: This pulse can then be used to provide a test input pulse for QT boards and their associated TAC boards.

18. Requirement: Local status and monitoring: The RCC-FOC front panel should incorporate the following signals to allow easy visual inspection of the current state.
- FPGA Configured (or not) LED
- Run/Stop Status LED
- Clock Error LED
- Clock Source Identification (1->5)
- Control Source Identification (1->3)
- Clock Out (TTL 50ohm lemo)
- Run/Stop Out (TTL 50ohm lemo)
- Test pulse Out (50ohm lemo)