Implementation of STAR CTB, VPD and MTD Triggers 2008

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CTB 2008: Only 4 of the original 16 layer 0 DSM boards are present. The analog signals are being summed in groups of 4 in η so the ϕ resolution stays the same. The layer 0 and layer 1 algorithms are unchanged, however the layer 2 algorithm will be simplified; there will only be 4 input topology bits instead of 16 and only one valid combination of those bits.

Layer 0 DSM CTB_CB001-004

NOTES:

Timing: This Module uses one RHIC clock override cycle, input $\Rightarrow$ n+2 output

Input: CB001 – South quadrant
CB002 – Bottom quadrant
CB003 – North quadrant
CB004 – Top quadrant

In each DSM:
15x 8 bit ADC values (corresponds to 60 slats)
Least significant bit is treated as the timing bit (bit 0/8)
Channel 16-bit8 = LED bit

Registers:

R0: (4bits) CTB dead time in RHIC counts
R1/R2 (12 bits) Min/Max of ADC sum for topology bits
R3/R4 (4bits) Min/Max for Slat sum for topology bits
R5-R12 dummies for halt counter
R13-R15 hidden halt counter registers

Tasks:

Gate ADC channels with dead time
Dead time: ADC=0 for R0*RHIC crossings after an ADC value was above zero
Sum gated ADC's
Count # of hit slats (gated ADC>0)
Check out-of-time signal for hit slats
Place thresholds on ADC sum and Slat Sum
Build topology information
Contains halt counter mechanics

Action:

1st Latch in ADC values
NOTE: All 8 bits are latched. It is assumed that if the CDBS are configured to send the timing bit, rather than the LSB of the ADC value, the effect in the MIP sum will be negligible.
Latch in LED bit
Latch timing bits (least significant bits of inputs)
Latch and invert board mode for halt counter

2nd Gate input channels with the dead time bit, determined from previous crossings
Delay timing bits to sync with gated ADC's
Delay Led Bit until clock 7

3rd Intermediate ADC sums
Intermediate sum of hit slats (ADC>0 after dead time gate)
Build out-of-time bit ('1' if in any channel ADC>0 and bit 0=0)

4th Total ADC sum
Total Sum of Slats
Delay timing bit until clock7.
Component 'engine dead' determined dead time status of each channel for next crossing

5th Delay ADC sum until clock 7
Place thresholds on ADC sum and Slat sum

6th Combine threshold bits to topology bit + overflow
Topology = ADC sum in window (R1/R2) and Slat sum in window (R3/R4)
Overflow = ADC sum > max (R2) or Slat sum > max (R4)

7th Map output

8th Latch output

Output (16 bits)

(0-11) Sum ADC (15*8 bits)
(12) Out-of-Time // (1: o-o-t-hit occurred, 0 event ok)
(13) Topology
(14) Topology Overflow
(15) Gain monitoring LED fired. (see below)

Layer 1 DSM L1_CB101

NOTE: In 2008 only 4 of the original 16 layer 0 DSM boards are present. Those boards send their data to channels 0:3 of CB101. Channels 4:7 will be zeroed out in the LUTS so their data will not contribute to the results of the algorithm. CB102 will be completely unused so its data will be zeroed out at the input to CB201, the layer 2 DSM.

Tasks:

Sum ADC's
Or and propagate led bit, out of time bit, topology overflow
Propagate topology bits

Input: Channel 0 (CB001) - South
Channel 1 (CB002) - Bottom
Channel 2 (CB003) - North
Channel 3 (CB004) - Top

From each of CB001, 2, 3 and 4
(0-11) ADC sum,
(12) out-of-time,
(13) Topology
(14) Topology Overflow
(15) LED bit

Registers:

None

Action:

1st
Latch ADC sums (0-11)
Latch out-of-time bit (12)
Latch topology bits
Latch topology overflow (14)
Latch led bit (15)

2nd
Intermediate ADC sum
Or LED bits
Or out-of-time bit
Delay topology bits for 2 cycles
Or topology overflow bits

3rd
Final ADC sum
Delay LED bit
Delay out-of-time bit
Delay topology-overflow

4th Map output

Output: (32 bits):

(0-14) ADC sum // 8*12 bits = 15 bits
(15) LED bit
(16) out-of-time bit
(17-22)Unused
(23-30)Topology bits
(31) Topology Overflow

Layer 0 DSM MIX_VP001-004

The VPD is currently using the BBC Layer 0 DSM algorithms. Please see the Vertex Tree documentation on the web at http://www.star.bnl.gov/public/trg/TSL/Software/BBC.pdf for a description of these algorithms

Layer 1 DSM L1_VP101

The VPD is currently using the BBC Layer 1 DSM algorithms. However there is a small change to take into account a cabling difference between the two systems, which results in a separate RBT file for the VPD. In the VPD system the input cable map is:

Channels 0/1: VP001, East-South
Channels 2/3: VP002, East-North
Channels 4/5: VP003, West-South
Channels 6/7: VP004, West North

The actual logic is the same as for the BB101 algorithm documented on the web at http://www.star.bnl.gov/public/trg/TSL/Software/BBC.pdf .

Layer 0 DSM MIX_MT001-2

Inputs: 16 8-bit TAC values

Registers:

R0: TAC window low threshold (8)
R1: TAC window high threshold (8)

LUT: Pedestal subtraction

Action:

1st Latch inputs

2nd Compare TAC values to thresholds

3rd For each channel, “valid TAC” = “low threshold < TAC < high threshold”
Build MTD bit from “valid TAC” bits
(ch0 and ch1) or (ch6 and ch9) or (ch5 and ch8) or (ch4 and ch7) or
(ch2 and ch3) or (ch10 and ch15) or (ch11 and ch14) or (ch12 and ch13)

4th Latch output

Output (0) MTD bit
(31-1) Unused

Layer 0 DSM MIX_PP001

RBT File: mix_pp001_2008_a.rbt
The same algorithm is used for PP001 (“Vertical” DSM) and PP002 (“Horizontal” DSM).

Inputs: 8 8-bit ADC values on channels 0-7.

Registers:
R0: ADC low threshold (8 bits)

LUT: Pedestal subtraction

Action:

1st Latch inputs

2nd Compare ADC values to threshold (R0) to make PMT bits
PMT(0) = 1 if ADC(0) > R0
PMT(1) = 1 if ADC(1) > R0
Etc….

3rd Build RP bits from PMT bits:
RP(0) = PMT(0) or PMT(1)
RP(1) = PMT(2) or PMT(3)
Etc….
Build elastic and inelastic bits from RP bits
Elastic(0) = RP(1) and RP(2)
Elastic(1) = RP(0) and RP(3)
Inelastic(0) = RP(0) xor RP(1)
Inelastic(1) = RP(2) xor RP(3)
Delay PMT bits

4th Latch output

Output (32 bits)

To layer1 DSM:

(0-1)	Elastic bits
(2-3)	Inelastic bits
(4-7)	Roman pot bits
(8-15)	Unused

To scaler system:

(16-23)	PMT bits
(24-25)	Elastic bits
(26-27)	Inelastic bits
(28-31)	Roman put bits

Layer 1 DSM L1_MD101

RBT File: l1_md101_2008_a.rbt

Inputs: From MT001 (channel 0) and MT002 (channel 2)

(0) MTD bit

NOTE: MT001 will not be used n the 2008 run so its input to MT101 will be zeroed out in the LUT.

From PP001 – pp2pp Vertical DSM (channel 4)

(0-7) EA (bit 0), EB, IEV, IWV, EVU, EVD, WVU, WVD (bit 7)

From PP002 – pp2pp Horizontal DSM (channel 5)

(0-7) EC, ED, IEH, IWH, EHO, EHI, WHO, WHI

Registers:

R0: (8 bits) bit-mask for turning elastic/inelastic components on/off

Bit 0 = EA, Bit 1 = EB, Bit 2 = IEV, Bit 3 = IWV

Bit 4 = EC, Bit 5 = ED, Bit 6 = IEH, Bit 7 = IWH

R1: (8 bits) bit-mask for turning individual hits on/off

Bit 0 = EVU, Bit 1 = EVD, Bit 2 = WVU, Bit 3 = WVD

Bit 4 = EHO, Bit 5 = EHI, Bit 6 = WHO, Bit 7 = WHI

LUT: 1:1

Action

1st Clock

Latch inputs

2nd Clock

OR MTD input bits together

Delay IEV and IEH to 4th clock

Mask all the pp2pp bits with the appropriate bit in the bit-masks

EA-masked = EA and R0(0)

IEV-masked = IEV and R0(2)

WVU-masked = WVU and R1(2), etc...

3rd Clock:

Delay MTD bit to 4th clock

Create ET, IT and single-HIT bits:

ET = EA-masked or EB-masked or EC-masked or ED-masked

IT = (IEV-masked or IEH-masked) and (IWV-masked or IWH-masked)

HIT = EVU-masked or EVD-masked or WVU-masked or WVD-masked or EHO-masked or EHI-masked or WHO-masked or WHI-masked

4th Clock:

Latch Output

Output (32 bits)

(0) Combined MTD bit
(1) ET bit
(2) IT bit
(3) IEV (delayed, NOT masked)
(4) IEH (delayed, NOT masked)
(5) HIT
(6-31) Unused

Layer 2 DSM L1_CB201

RBT File: l1_cb201_2008_b.rbt

Task: Pass through CTB ADC sum and LED bit
Provide decision on CTB topology
Apply 2 windows to VPD TAC difference
Pass through VPD ADC sum threshold bits
Pass through MTD and pp2pp bits

Input: 32 bits for CTB (Ch 0 and 1)

(14-0) ADC sum
(15) LED bit
(16) out-of-time bit
(22-17) Unused
(26-23) Topology bits:
0 = South, 1 = Bottom, 2 = North, 3 = Top
(30-27) Unused
(31) Topology overflow bit

6 bits for MTD and pp2pp (Ch 4)

(0) MTD bit

The next 5 bits are pp2pp bits:

(1) ET bit
(2) IT bit
(3) IEV bit
(4) IEH bit

(5) Single hit bit
(6-15) Unused

16 bits for VPD (Ch 7)
NOTE: The BB101 algorithm that is used by VP101 passes its data to the next level on JP6 not JP1. For CB201 this means the data arrives on Ch 7, not Ch 6.
(8-0) TAC difference
(11-9) Unused
(15-12)Threshold bits

Registers:
R0: topology selection (3)
Bit 0 = 1 'veto out-of-time' hits
Bit 1 = 1 'veto topology overflow
Bit 2 = 1 'use UPC algorithm for topology decision
The default setting is R0=0x7 ('111')
R1: VPD TAC Difference Min0 (9)
R2: VPD TAC Difference Max0 (9)
R3: VPD TAC Difference Min1 (9)
R4: VPD TAC Difference Max1 (9)

Action:

1st Latch Inputs

2nd Delay CTB ADC sum to 4th clock
Delay CTB LED bit to 4th clock
Delay CTB out-of-time bits to 3rd clock
Delay CTB topology overflow bit to 3rd clock
Build CTB topology bit
topology = (not Top) and (not Bottom) and (North and South)
Delay VPD ADC threshold bits to 4th clock
Compare VPD TAC difference to thresholds (Regs 1:4)
Delay MTD bit to 4th clock
Delay pp2pp bits to 4th clock

3rd Gate out-of-time bit, topology-bit and topology overflow bit with reg0 and then combine to make final topology bit
Combine VPD TAC difference bits to make windows

4th Latch output

Output:
(0-14) 15 bit ADC sum
(15) Unused
(16) VPD TAC difference inside window 0 (Registers 1 and 2)

(17) VPD TAC difference inside window 1 (Registers 3 and 4)
(18) VPD East ADC Sum greater than threshold 0
(19) VPD West ADC Sum greater than threshold 0
(20) VPD East ADC Sum greater than threshold 1
(21) VPD West ADC Sum greater than threshold 1
(22) MTD bit
(23) ET bit
(24) IT bit
(25) IEV bit
(26) IEH bit
(27) Single pp2pp hit bit
(28-29) Unused
(30) topology bit
(31) LED bit