Second Bunch Crossing Counter DSM Algorithm

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Input Bits

Input Channel	Bit Description
0	Lower 16 bits of BC_1 output
1	Upper 16 bits of BC_1 output
2:6	Unused
7	Bit 0 – RHIC synchronization bit

Registers

Register	Register Description
0	Initial counter value, 16 bits.

Output Bits

Bit	Description
Bits 0:15	Current 16-bit bunch crossing counter value
Bits 16:22	Current 7-bit bunch type counter value
Bits 23	Unused
Bits 24:30	2nd copy of Current 7-bit bunch type counter value
Bits 31	Unused

Internal Logic

- 16-bit bunch crossing counter increments by one only when input from BC_1 changes from 0xffffffff to 0x00000000.
  - Counts only when DSM is running.
  - Counter starts at a user defined value (Reg0).
  - Current counter value is output on output bits 0:15
- 7-bit bunch type counter increments by one on each tick of the RHIC clock.
  - Counts only when DSM is running
  - Counter always starts from zero (0)
  - Counting doesn't begin until the first RHIC synchronization signal is received AFTER the DSM board starts running. All subsequent RHIC synchronization signals are ignored.
  - Resets to zero (0) when it reaches 119
  - Current counter value is output on bits 16:22 and 24:30