

Implementation of STAR EM-Calorimeter Trigger 2008 PP Configuration

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30th January 2008

The description of the last EMC DSM (EM201) which combines the Endcap and Barrel is at the end. PLEASE REFER TO SKIPS WEBPAGE FOR THE GEOMETRY. (Anti-)clockwise and/or lower/higher hour is determined looking from West towards the IP.

1. Layer 0 DSM BEMC-B001 and EEMC-E001

This DSM algorithm is the same for Endcap and Barrel East and West. It takes 10 12-bit-input channels. It sums up the 6-bit ADC trigger-patch (TP) values in parallel with placing one threshold on them. It places four thresholds on the high-tower (HT) 6-bit ADC values. It combines the high-tower threshold #3 results with the trigger patch threshold results (HT.TP).

RBT File: `bemc_b001_2008_b.rbt`

Input: 10 12-bit EM-Cal channels
bits (5-0) high-tower, bits (11-6) trigger-patch

LUT: Pedestal subtraction and energy calibration is done in the EMC readout electronics. Therefore the LUT's are 1:1. Missing/Dead/Non-instrumented channels are zeroed out.

Registers: There are 5 registers in total:

- 4 thresholds for 6-bit, high-tower ADC values. **THE FIRST THREE THRESHOLDS ARE SIZE ORDERED!** i.e. $th_2 > th_1 > th_0$. If the size order is not obeyed the trigger will not fire. The fourth threshold (used in the HT.TP logic) is completely independent of the other three thresholds.
- 1 threshold for 6-bit, trigger-patch ADC values.

For the Barrel **BCW** and (!) **BCE**; index: 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e

R0: BEMC-High-Tower-th0 (6-bits)

R1: BEMC-High-Tower-th1 (6)

R2: BEMC-High-Tower-th2 (6)

R3: BEMC-High-Tower-th3 (6)

R4: BEMC-Trigger-Patch-th0 (6)

For the Endcap **EEC**; index: 0x17, 0x18, 0x19, 0x1a, 0x1b, 0x1c, 0x1d, 0x1e, 0x1f

R0: EEMC-High-Tower-th0 (6)

R1: EEMC-High-Tower-th1 (6)

R2: EEMC-High-Tower-th2 (6)
R3: EEMC-High-Tower-th3 (6)
R4: EEMC-Trigger-Patch-th0 (6)

Action:

- 1st Latch input
- 2nd Place four thresholds on each high-tower value
Place one threshold on each trigger-patch value.
Intermediate trigger-patch ADC sum
NOTE: An input value of 63 (i.e. all 6 bits high) is ignored in the threshold comparison logic but is included in the sum.
- 3rd 'or' threshold bits for all 10 high-towers
'or' threshold bits for all 10 trigger-patches
'and' each bit from the high-tower threshold #3 comparison with its associated trigger-patch bit, and then 'or' the results for all 10 trigger patches: i.e.
$$\text{HT3.TP0} = (\text{ht}(0) > \text{ht_th3} \text{ AND } \text{tp}(0) > \text{tp_th0}) \text{ OR } (\text{ht}(1) > \text{ht_th3} \text{ AND } \text{tp}(1) > \text{tp_th0}) \text{ OR } \dots (\text{ht}(9) > \text{ht_th3} \text{ AND } \text{tp}(9) > \text{tp_th0})$$

Code the information about the first three HT thresholds into 2 bits ('00' ADC<th0, '01' ADC>th0, '10' ADC > th1, '11' ADC>th2)
Total ADC sum for trigger patches
- 4th Latch output

Output: (9-0) ADC-sum Trigger patches
(11-10) High-tower threshold bits (thresholds #0, #1 and #2, encoded)
(12) High-tower threshold #3 bit
(13) Trigger-patch threshold #0 bit
(14) High-tower AND Trigger-patch threshold bit (HT3.TP0)
(15) Unused

2. Layer 0 DSM BEMC-B(E/W)003-8-13

This DSM algorithm is similar to BEMC-B001. The input is split into to two separate 0.2x1.0 jet patches.

RBT File: bemc_b003_2008_b.rbt

Input: 10x12 bit channels. The two 0.2 patches are labeled J1 and J3.
Even input channels J1: ch0/2/4/6/8; odd channels J3: ch1/3/5/7/9
The geometry/position for J1 and J3 is swapped between East and West, which plays a role when forming jet-patches in layer1.
West J1: clockwise side, higher hour J3: anti-clockwise side, lower hour
East J3: clockwise side, higher hour J1: anti-clockwise side, lower hour

LUT: 1:1; Zero out missing channels

Registers: The registers are identical to BEMC-B001 and they are listed there.

Action: same as B001

Output: Two cables:

J3: West=Anti-clockwise/low hour; East=clockwise/high hour
(8-0) ADC-sum Trigger patches J3
(9) empty (sum one bit shorter than in B001)
(11-10) High-tower threshold bits J3
(12) High-tower threshold #3 bit J3
(13) Trigger-patch threshold #0 bit J3
(14) High-tower AND Trigger-patch threshold bit (HT3.TP0) J3
(15) Unused
J1: West=Clockwise/high hour; East=anti-clockwise/low hour
(24-16) ADC-sum Trigger patches J1
(25) empty (sum shorter than B001)
(27-26) High-tower threshold bits J1
(28) High-tower threshold #3 bit J1
(29) Trigger-patch threshold #0 bit J1
(30) High-tower AND Trigger-patch threshold bit (HT3.TP0) J1
(31) Unused

3. Layer 0 DSM EEMC-E002-5-8

This DSM algorithm is similar to B001. The input is split into to two separate 0.3x1.0 6-tower jet patches.

RBT Files: eemc_e002_2008_b.rbt

Input: 10x12 bit channels. The two 0.3x1 patches are labeled (J0 anti-clockwise side/low hour) and J1 (clockwise side/high hour) J0: ch0/1/2/3/4
J1: ch5/6/7/8/9

LUT: 1:1, zero out missing channels

Registers: The registers are identical to BEMC-B001 and they are listed there.

Action: same as B001

Output: Two cables:

Anti-clockwise part/low hour
(8-0) ADC-sum Trigger patches J0
(9) empty (sum one bit shorter than in BB001)
(11-10) High-tower threshold bits J0
(12) High-tower threshold #3 bit J0
(13) Trigger-patch threshold #0 bit J0
(14) High-tower AND Trigger-patch threshold bit (HT3.TP0) J0
(15) Unused

Clockwise part/high hour
 (24-16) ADC-sum Trigger patches J1
 (25) empty (sum shorter than B001)
 (27-26) High-tower threshold bits J1
 (28) High-tower threshold #3 bit J1
 (29) Trigger-patch threshold #0 bit J1
 (30) High-tower AND Trigger-patch threshold bit (HT3.TP0) J1
 (31) Unused

4. Layer 1 DSM BEMC-B(E/W)101-103

This algorithm combines two 1x1 barrel jet patches (jp0-anti-clockwise/lower hour and jp1-clockwise/higher hour): it combines their high tower bits, their trigger-patch bits and their “HT.TP” bits as well as placing thresholds on their ADC sums. There are two different algorithms for east and west to take care of the switch in geometry position of the J1/J3 half modules from input channels ch2 and ch3. The West algorithm combines channels 0, 1 and 2 for jet patch 0 and channels 3, 4 and 5 for jet patch 1. The East algorithm combines channels 0, 1 and 3 for jet patch 0 and channels 2, 4 and 5 for jet patch 1.

Input: ch0-B001 - 0.4x1.0
 ch1-B002 - 0.4x1,0
 ch2-B003 - lower bits, J3 0.2x1.0 West: anti-clockwise; East: clockwise
 ch3-B003 - upper bits, J1 0.2x1.0 West: clockwise; East: anti-clockwise
 ch4-B004 - 0.4x1.0
 ch5-B005 - 0.4x1.0
 ch6/7 not used
 same for B006-15

from B001/002/004/005
 (9-0) = TP ADC sum
 (11-10) High-tower threshold bits (thresholds #0, #1 and #2, encoded)
 (12) High-tower threshold #3 bit
 (13) Trigger-patch threshold #0 bit
 (14) High-tower AND Trigger-patch threshold bit (HT3.TP0)
 (15) Unused

from B003
 (8-0) ADC-sum Trigger patches J3
 (9) empty (sum one bit shorter than in B001)
 (11-10) High-tower threshold bits J3
 (12) High-tower threshold #3 bit J3
 (13) Trigger-patch threshold #0 bit J3
 (14) High-tower AND Trigger-patch threshold bit (HT3.TP0) J3
 (15) Unused

J1: West=Clockwise/high hour; East=anti-clockwise/low hour
 (24-16) ADC-sum Trigger patches J1
 (25) empty (sum shorter than B001)
 (27-26) High-tower threshold bits J1
 (28) High-tower threshold #3 bit J1
 (29) Trigger-patch threshold #0 bit J1

- (30) High-tower AND Trigger-patch threshold bit (HT3.TP0) J1
- (31) Unused

LUT: 1:1

Registers: **BC1**, index East 0x21, 0x10, 0x11; West 0x12, 0x13, 0x14

Three thresholds for 12-bit jet patch ADC values.

R0: BEMC-Jet-Patch-th0 (12)

R1: BEMC-Jet-Patch-th1 (12)

R2: BEMC-Jet-Patch-th2 (12)

Action:

- 1st Latch input
- 2nd Sum the ADC sums from the trigger patches to the two separate 1x1 jet patch energies (12 bits).
Decode and combine the HT0, 1 and 2 bits for each jet patch separately
Combine the HT3 bits from all channels.
Combine the TP0 bits from all channels.
Combine the HT3.TP0 bits from all channels.
- 3rd Sum both jet patch energies to a 13-bit energy sum for the 2x1 barrel segment and then select bits 2:6. If ANY of bits 7:12 are on then the result is 31, i.e. all 5 bits on.
Place three Jet-Patch ADC thresholds on the individual jet patch energies and combine the three thresholds into two bits.
Code the 3 bits for HT0, 1 and 2 back into a 2-bit integer.
Delay the bits for HT3, TP0 and HT3.TP
- 4th Latch output

Output: (4-0) Middle 5 bits of the total energy sum

(5-6) empty

(7) HT3 bit, jp0 and jp1 combined

(8) TP0 bit, jp0 and jp1 combined

(9) HT3.TP0 bit, jp0 and jp1 combined

(11-10) Jet patch threshold bits, jp0 and jp1 combined

(13-12) High-tower threshold bits jp0

(15-14) High-tower threshold bits jp1

5. Layer 1 DSM EEMC-E101/E102

This algorithm combines three 0.9x1 Endcap jet patches: it combines their high tower bits, their trigger-patch bits and their “HT3.TP0” bits as well as and placing thresholds on their ADC sums.

Input: (E101)

ch0-E001 - 0.6x1.0

ch1-E002 - 0.3x1,0 bits(15-0), jp0 anti-clockwise

ch2-E002 - 0.3x1.0 bits(31-16),jp1 clockwise
ch3-E003 - 0.6x1.0
ch4-E004 - 0.6x1.0
ch5-E005 - 0.3x1.0 bits(15-0), jp0 anti clockwise
ch6/7 not used

Input: (E102)
ch0-E005 - 0.3x1.0 bits(31-16),jp1 clockwise
ch1-E006 - 0.6x1,0
ch2-E007 - 0.6x1.0
ch3-E008 - 0.3x1.0 bits(15-0), jp0 anti-clockwise
ch4-E008 - 0.3x1.0 bits(31-16),jp1 clockwise
ch5-E009 - 0.6x1.0
ch6/7 not used

from E001/003/004/006/007/009
(9-0) = TP ADC sum
(11-10) High-tower threshold bits (thresholds #0, #1 and #2, encoded)
(12) High-tower threshold #3 bit
(13) Trigger-patch threshold #0 bit
(14) High-tower AND Trigger-patch threshold bit (HT3.TP0)
(15) Unused
from E002/005/008
(8-0) ADC-sum Trigger patches J0
(9) empty (sum one bit shorter than in BB001)
(11-10) High-tower threshold bits J0
(12) High-tower threshold #3 bit J0
(13) Trigger-patch threshold #0 bit J0
(14) High-tower AND Trigger-patch threshold bit (HT3.TP0) J0
(15) Unused
(24-16) ADC-sum Trigger patches J1
(25) empty (sum shorter than B001)
(27-26) High-tower threshold bits J1
(28) High-tower threshold #3 bit J1
(29) Trigger-patch threshold #0 bit J1
(30) High-tower AND Trigger-patch threshold bit (HT3.TP0) J1
(31) Unused

LUT: 1:1

Registers: **EEC**; index lower half 0x15, upper 0x16 (not in 2003)

Three thresholds for 11bit 1x0.9 jet patch ADC sum.

R0: EEMC-Jet-Patch-th0 (11)

R1: EEMC-Jet-Patch-th1 (11)

R2: EEMC-Jet-Patch-th2 (11)

Action:

1st Latch input

2nd Sum the ADC sums from the trigger patches to the three separate 0.9x1 jet patch energies (11 bits).

- Decode the HT0, 1 and 2 bits from all channels
 - Combine the HT3 bits from all channels.
 - Combine the TP0 bits from all channels.
 - Combine the HT3.TP0 bits from all channels.
- 3rd
- Sum the three jet patch energies to a 13-bit energy sum for the 0.9x3 Endcap segment and then select bits 2:6. If ANY of bits 7:12 are on then the result is 31, i.e. all 5 bits on.
 - Place three thresholds on the individual jet patch energies and code the three thresholds into two bits.
 - Combine the HT0, 1 and 2 bits from all channels and encode the 3 bits back into a 2-bit integer.
 - Delay the HT3, TP0 and HT3.TP0 bits
- 4th Latch output

Output: (4-0) Middle 5 bits of the total energy sum
 (5-6) empty
 (7) HT3 threshold bit, jp0, jp1 and jp2 combined
 (8) TP0 threshold bit, , jp1 and jp2 combined
 (9) HT3.TP0 threshold bit, jp0, jp1 and jp2 combined
 (11-10) Jet Patch threshold bits, jp0, jp1 and jp2 combined
 (13-12) High-tower threshold bits jp0, jp1 and jp2 combined
 (15-14) empty

6. Layer 2 DSM L1-EM201 (2008)

This is the third layer algorithm for the EMC tree for the 2008 proton run. The HT, TP, HT.TP and jet patch threshold bits for Endcap and Barrel are going separately into the TCU. The total energy sum trigger is enabled for Barrel, Endcap and their sum.

Input ch0- 1.0x2.0 BEMC-BE101 10' and 12'
 ch1- 1.0x2.0 BEMC-BE102 2' and 4'
 ch2- 1.0x2.0 BEMC-BE103 6' and 8'
 ch3- 1.0x2.0 BEMC-BW101 10' and 12'
 ch4- 1.0x2.0 BEMC-BW102 2' and 4'
 ch5- 1.0x2.0 BEMC-BW103 6' and 8'
 ch6- 0.9x3.0 EEMC-E101 4', 6' and 8'
 ch7- 0.9x3.0 EEMC-E102 10', 12' and 2'

from B101/102/103
 (4-0) = JP ADC sum middle 5 bits
 (6-5) = empty
 (7) HT3 bit, jp0 and jp1 combined
 (8) TP0 bit, jp0 and jp1 combined
 (9) HT3.TP0 bit, jp0 and jp1 combined
 (11-10) Jet patch threshold bits, jp0 and jp1 combined
 (13-12) High-tower threshold bits jp0
 (15-14) High-tower threshold bits jp1

from E101/102
(4-0) = JP ADC sum middle 5 bits
(6-5) = empty
(7) HT3 threshold bit, jp0, jp1 and jp2 combined
(8) TP0 threshold bit, , jp1 and jp2 combined
(9) HT3.TP0 threshold bit, jp0, jp1 and jp2 combined
(11-10) Jet Patch threshold bits, jp0, jp1 and jp2 combined
(13-12) High-tower threshold bits jp0, jp1 and jp2 combined
(15-14) empty

LUT: 1:1

Registers: **L1**; index: 0x1a: five thresholds and mode setting bits, for explanation see below

R0: BEMC Energy Sum Threshold (8)
R1: EEMC Energy Sum Threshold (6)
R2: J/Ψ Threshold Select (2)
Values: 0 – th0; 1 – th1; 2 – th2; 3 – J/Ψ logic OFF
Select which BEMC High-Tower threshold (BEMC B001, B003-8-13:R0-2) is used for the J/Ψ topology trigger
R3: Total Energy Sum Select (3)
Bit 0 – Barrel East on/off
Bit 1 – Barrel West on/off
Bit 2 – Endcap on/off
Selects which pieces of the calorimeter are used in the BEMC energy sum and the BEMC+EEMC total energy sum.
R4: BEMC+EEMC Energy Sum Threshold (8)

Action: Sum the jet patch energies for the six 2x1 Barrel segments using R3 to select which halves of the Barrel are included.

Place threshold $e_{\text{Barrel}} > \text{BEMC-Energy-Sum-th (R0)}$

Sum the jet patch energies for the two Endcap segments

Place threshold $e_{\text{Endcap}} > \text{EEMC-Energy-Sum-th (R1)}$

Add e_{Barrel} and e_{Endcap} to get e_{Total} using R3 to define if the Endcap should be included or not.

Place threshold $e_{\text{Total}} > \text{BEMC+EEMC-Energy-Sum-th (R4)}$

Combine the jet patch thresholds bits for the Barrel and separately for the Endcap

Combine the HT0, 1 and 2 threshold bits for the Barrel and separately for the Endcap

Combine the HT3 threshold bits for the Barrel and separately for the Endcap.

Combine the TP0 threshold bits for the Barrel and separately for the Endcap.

Combine the HT3.TP0 threshold bits for the Barrel and separately for the Endcap.

The J/Ψ trigger uses just the high tower threshold bits of the Barrel, not the Endcap. R2 selects ONE of the high-tower thresholds for this trigger (see above). The J/Ψ trigger fires if two non-neighboring jet patches have high towers above the selected threshold:

– vector bits (0-5) correspond to positions 2,4,6,8,10,12 o'clock
J/Ψ trigger = (ht-jpsi(0) and (ht-jpsi(2) or ht-jpsi(3) or ht-jpsi(4))) or
(ht-jpsi(1) and (ht-jpsi(3) or ht-jpsi(4) or ht-jpsi(5))) or
(ht-jpsi(2) and (ht-jpsi(4) or ht-jpsi(5))) or
(ht-jpsi(3) and ht-jpsi(5))

Where ht-jpsi(X) = Barrel-East-ht-jpsi(X) OR Barrel-West-ht-jpsi(X)

Output: Available in the last DSM/TCU!

EEMC and BEMC are kept separate and get separate bits in the TCU

(1-0) jet patch threshold bits BARREL

(3-2) high tower threshold bits BARREL

(4) energy sum threshold bit BARREL

(5) J/Ψ topology bit (Barrel East and West, no Endcap)

(6) HT3.TP0 threshold bit BARREL

(8-7) jet patch threshold bits ENDCAP

(10-9) high tower threshold bits ENDCAP

(11) energy sum threshold bit ENDCAP

(12) HT3.TP0 threshold bit ENDCAP

(13) HT3 threshold bit BARREL

(14) HT3 threshold bit ENDCAP

(15) energy sum threshold bit BARREL+ENDCAP

Scalers:

Duplicate Output, see above