Algorithms for the FMS DSM Tree
RHIC 2017 p+p Run

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Change Log:

Date	Description
February 6, 2015	First version for 2015. There are big changes this year to both the hardware and software. The connections from the FMS modules to the QT boards have been re-arranged. A 4th DSM board has been added to layer-1 and the connections within the DSM tree have been adjusted accordingly. The FPD-East detector logic has been removed entirely.
February 23, 2015	Changes to the FM101 and FP201 algorithms, making the "b" versions. Bit 0 going from FM101 to FP201 is stuck high (1) so the BS3 bit has been moved to Bit 13. Since the FM101 algorithm is also used by FM102 this meant changes to FP201 in 2 places.
November 8, 2016	Modifications for 2017 to improve the efficiency of the topology bit (FMS-DiBS) for selecting Drell-Yan and J/Psi events. There are no changes to any cabling or to the layer-2 algorithm. There are minor changes to the layer-0 and -1 algorithms that are all associated with how the intermediate board sums are combined.
April 5, 2017	The FM103 layer-0 algorithm has been re-implemented to fix some bit problems. Steps 2 and 3 have been combined, and the merged Step is given 2 ticks of the clock instead of 1. There are no changes to any registers, the definitions of any I/O bits or any logic. The algorithm has been in use from March 9 onward.

FMS Cell to QT Board Assignment Scheme

The FMS cells are assigned to QT boards using a geometrical scheme composed of a large set of simple rectangles. The assignment of FMS cells to the 4 QT8 cards within each QT board has been done using a "striping" scheme, where the stripes run along the length of the rectangles. This scheme is shown in Figure 1.

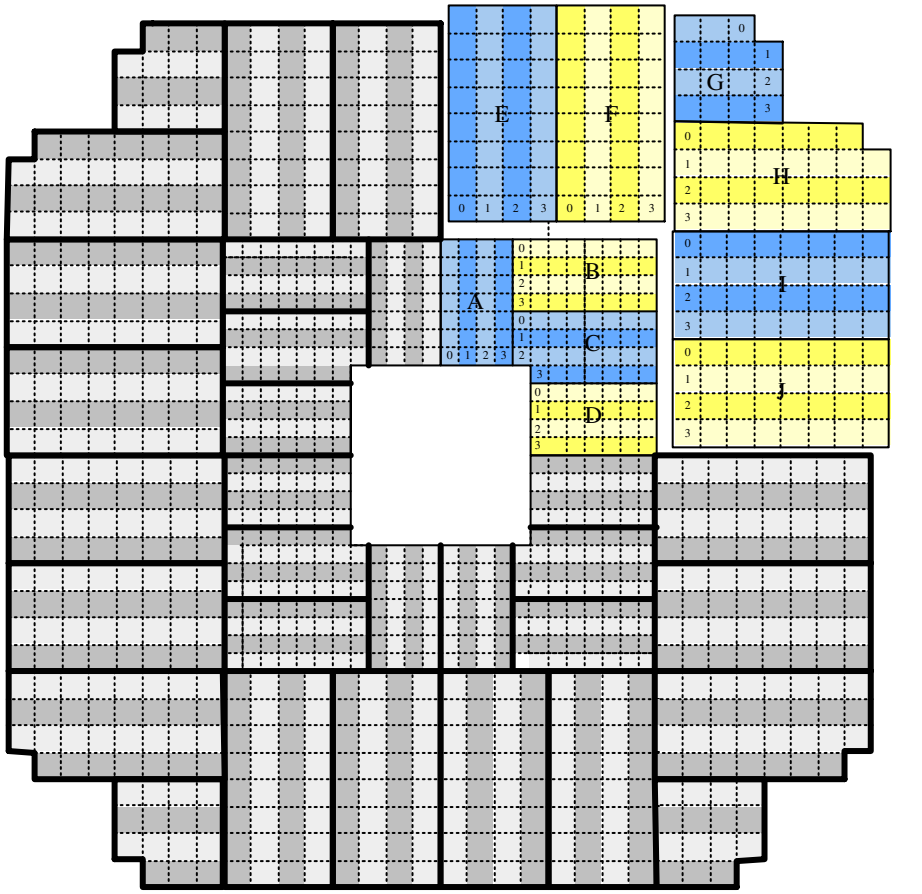

Figure 1: FMS Cell to QT and Layer-0-DSM Assignment Scheme

- All of the FMS cells that connect to the DSM tree are shown in Figure 1.
- The cells contained within a thick solid line are all connected to one QT board.
- In 3 of the 4 quadrants the stripes, indicating which QT8 card a cell is assigned to, are shown in light and dark gray.
- In the upper right quadrant the stripes are shown in shades of blue and yellow.
- In this quadrant each QT board has a label from A to J. The 4 stripes in each QT board (representing the 4 QT8 cards) are labeled from 0 to 3.
- Finally, the cells in that upper right quadrant are separated out into 3 groups, indicating which QT board is connected to each of 3 layer-0 DSMS.

The QT algorithm was written by Chris Perkins and is documented at
http://www.star.bnl.gov/public/trg/TSL/Software/qt_v6_e_doc.pdf
It calculates the sum of ADC values from all channels of QT8 cards 0 and 1, and the same for cards 2 and 3. The user has the option to exclude certain channels from the sums. This makes it possible to ignore channels that are dead or noisy. In the rest of this document those sums are referred to using the reference numbers of the relevant QT8 cards, e.g. A(01) refers to the sum of all channels of QT8(0) and QT8(1) of QT-A.

Layer 0 DSM Tree Algorithms

In the layer-0 DSM boards Board Sums (BS) are reconstructed by adding together pairs of the QT8 sums received from the QT boards. Each BS is compared to three thresholds and the results are combined. In parallel larger groups of QT8 sums are added together to form partial jet patches. A subset of bits from those patches is all that is needed to give the required range and resolution, so the results are truncated, with logic to indicate when an overflow has occurred. Table 1 shows the equations that are used.

DSM Board	BS Name	Equation	Jet Patch Name	Equation
Small cell quadrant	BS-A	A(01) + A(23)	JP-AB	A(01) + A(23) + B(01) + B(23)
	BS-B	B(01) + B(23)	JP-CD	C(01) + C(23) + D(01) + D(23)
	BS-BC	B(23) + C(01)		
	BS-C	C(01) + C(23)		
	BS-CD	C(23) + D(01)		
	BS-D	D(01) + D(23)		
Large cell, upper/lower section	BS-E	E(01) + E(23)	JP-EF	E(01) + E(23) + F(01) + F(23)
	BS-EF	E(23) + F(01)		
	BS-F	F(01) + F(23)		
Large cell, side section	BS-G	G(01) + G(23)	JP-GH	G(01) + G(23) + H(01) + H(23)
	BS-GH	G(23) + H(01)	JP-IJ	I(01) + I(23) + J(01) + J(23)
	BS-H	H(01) + H(23)		
	BS-HI	H(23) + I(01)		
	BS-I	I(01) + I(23)		
	BS-IJ	I(23) + J(01)		
	BS-J	J(01) + J(23)		

Table 1: Equations for BS and JP Calculations

There will be 3 slightly different versions of the layer-0 algorithm: one for the DSM board that processes small cell data (QT A-D), a second algorithm for the DSM board that processes the upper/lower section of the large cell array (QT E and F) and a final version for the DSM board that process data from the side of the large cell array (G - J). They will operate as follows:

Small-Cell Layer 0 DSM Board:

- RBT File: fms_fm001_2017_a.rbt
- Users: FM001, FM002, FM003, FM004
- Input: The QT board connections are reversed from what you might expect:
    - Channels 0/1 = QT Board D
    - Channels 2/3 = QT Board C
    - Channels 4/5 = QT Board B
    - Channels 6/7 = QT Board A

  From each board the DSM receives:
    - Bits 0:11 = Sum of QT8(0) and (1)
    - Bits 12:15 = Unused
    - Bits 16:27 = Sum of QT8(2) and (3)
    - Bits 28:31 = Unused
- LUT: 1-to-1 mapping
- Registers: Three threshold registers for the BS logic and a 4th register to control the JP bit selection:
    - R0: FMSsmall-BS-th1 (13 bits)
    - R1: FMSsmall-BS-th2 (13)
    - R2: FMSsmall-BS-th3 (13)
    - R3: FMSsmall-BitSelect (3 bits)
        - Value = 0 means select bits 0:7
        - Value = 1 means select bits 1:8
        - etc…
- Step 1: Latch the input data.
- Step 2: Implement all the small-cell equations shown in Table 1 to make the BS and JP values. In parallel, delay a copy of the D(23) value to the 4th Step.
- Step 3: Compare each BS value to the 3 thresholds. Combine the results to make the following threshold bits:
    - BS3 = at least one BS value greater than th3
    - BS2 = at least one BS value greater than th2
    - BS1-CD = at least one BS value in BS-CD or BS-D greater than th1
    - BS1-ABC = at least one BS value in BS-A, -B, -BC or -C greater than th1

  Use R3 to select 8 bits from each of the 2 JP values. Set the result to 255 (i,e, binary 11111111) if any higher order bits are set.
- Step 4: Latch the output data:
    - Bit 0 = BS3
    - Bit 1 = BS2
    - Bit 2 = BS1-CD
    - Bit 3 = BS1-ABC
    - Bits 4:15 = D(23)

- Bits 16:23 = JP-AB
- Bits 24:31 = JP-CD

Large-Cell Layer 0 DSM Board: Side section of the array

- RBT File: fms_fm005_2017_a.rbt
- Users: FM005, FM007, FM009, FM011
- Input: The QT board connections are reversed from what you might expect:
  - Channels 0/1 = QT Board J
  - Channels 2/3 = QT Board I
  - Channels 4/5 = QT Board H
  - Channels 6/7 = QT Board G

  From each board the DSM receives:
  - Bits 0:11 = Sum of QT8(0) and (1)
  - Bits 12:15 = Unused
  - Bits 16:27 = Sum of QT8(2) and (3)
  - Bits 28:31 = Unused
- LUT: 1-to-1 mapping
- Registers: Three threshold registers for the BS logic and a 4th register to control the JP bit selection:
  - R0: FMSlarge-BS-th1 (13 bits)
  - R1: FMSlarge-BS-th2 (13)
  - R2: FMSlarge-BS-th3 (13)
  - R3: FMSlarge-BitSelect (3 bits)
    - Value = 0 means select bits 0:7
    - Value = 1 means select bits 1:8
    - etc…
- Step 1: Latch the input data.
- Step 2: Implement all the large-cell side-section equations shown in Table 1 to make the BS and JP values. In parallel, delay a copy of the J(23) value to the 4th Step.
- Step 3: Compare each BS value to the 3 thresholds. Combine the results to make the following threshold bits:
  - BS3 = at least one BS value greater than th3
  - BS2 = at least one BS value greater than th2
  - BS1-IJ = at least one BS value in BS-I, –IJ or –J greater than th1
  - BS1-GH = at least one BS value in BS-G, –GH, –H or –HI greater than th1

  Use R3 to select 8 bits from each of the 2 JP values. Set the result to 255 (i,e, binary 11111111) if any higher order bits are set.
- Step 4: Latch the output data:
  - Bit 0 = BS3
  - Bit 1 = BS2
  - Bit 2 = BS1-IJ
  - Bit 3 = BS1-GH
  - Bits 4:15 = J(23)
  - Bits 16:23 = JP-GH

- Bits 24:31 = JP-IJ

Large-Cell Layer 0 DSM Board: Upper/lower section of the array

- RBT File: fms_fm006_2017_a.rbt
- Users: FM006, FM008, FM010, FM012
- Input: The QT board connections are reversed from what you might expect:
  - Channels 0/1 = QT Board F
  - Channels 2/3 = QT Board E
  - Channels 4/5 = Unused
  - Channels 6/7 = Unused

  From each board the DSM receives:
  - Bits 0:11 = Sum of QT8(0) and (1)
  - Bits 12:15 = Unused
  - Bits 16:27 = Sum of QT8(2) and (3)
  - Bits 28:31 = Unused
- LUT: 1-to-1 mapping
- Registers: Three threshold registers for the BS logic and a 4th register to control the JP bit selection:
  - R0: FMSlarge-BS-th1 (13 bits)
  - R1: FMSlarge-BS-th2 (13)
  - R2: FMSlarge-BS-th3 (13)
  - R3: FMSlarge-BitSelect (3 bits)
    - Value = 0 means select bits 0:7
    - Value = 1 means select bits 1:8
    - etc…
- Step 1: Latch the input data.
- Step 2: Implement all the large-cell upper/lower-section equations shown in Table 1 to make the BS and JP values.
- Step 3: Compare each BS value to the 3 thresholds. Combine the results to make the following threshold bits:
  - BS3 = at least one BS value greater than th3
  - BS2 = at least one BS value greater than th2
  - BS1-EF = at least one BS value in BS-E, -EF or –F greater than th1

  Use R3 to select 8 bits from each of the 2 JP values. Set the result to 255 (i,e, binary 11111111) if any higher order bits are set.
- Step 4: Latch the output data:
  - Bit 0 = BS3
  - Bit 1 = BS2
  - Bit 2 = BS1-EF
  - Bit 3 = Unused
  - Bits 4:15 = Unused
  - Bits 16:23 = JP-EF
  - Bits 24:31 = Unused

Layer 1 DSM Tree Configuration and Algorithm

From Figure 1 it can be seen that there are 3 types of layer 0 DSM board: small cell quadrant, large cell upper/lower section and large cell side section. There are 4 layer 0 DSM boards of each type, one in each of four quadrants. This makes 12 layer 0 DSM boards in total. The connections from the layer 0 DSM boards to the layer 1 DSM boards have been made to separate out the North and South halves of the array as shown in Figure 2.

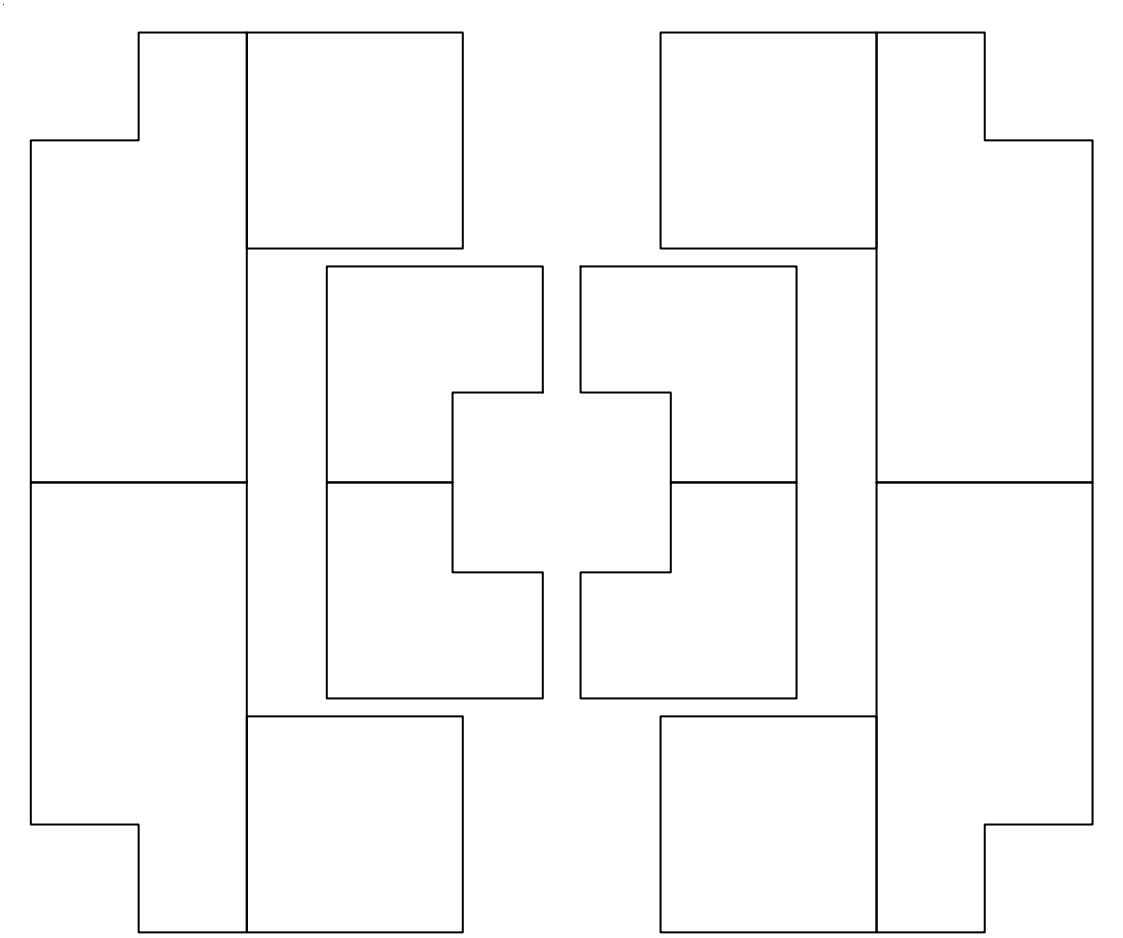

Figure 2: DSM Layer 0 to Layer 1 Assignment Scheme

Both small-cell layer-1 DSMS will use the same algorithm, and the two large-cell DSMS will also share an algorithm. The 2 algorithms are very similar. The partial jet patch values calculated at layer-0 will be combined to make full-sized over-lapping jet patches. The BS values that overlap adjacent layer-0 DSM boards (BS-DD and BS-JJ) will be calculated and the result compared to the same thresholds that are used at layer-0. Those extra threshold bits will then be combined with the existing threshold bits.

The layer 1 DSM algorithms will therefore perform the following steps:

Small-Cell Layer 1 DSM Board

- RBT File: fms_fm101_2017_a.rbt
- Users: FM101 (South), FM102 (North)
- Input:
    - Channels 0/1 = FM001 or FM003 (Top)
    - Channels 2/3 = FM002 or FM004 (Bottom)
    - Channels 4/5 = Unused
    - Channels 6/7 = Unused

  From each board the DSM receives:
    - Bit 0 = BS3
    - Bit 1 = BS2
    - Bit 2 = BS1-CD
    - Bit 3 = BS1-ABC
    - Bits 4:15 = D(23)
    - Bits 16:23 = JP-AB
    - Bits 24:31 = JP-CD
- LUT: 1-to-1 mapping
- Registers: Three threshold registers for the BS logic:
    - R0: FMSsmall-BS-th1 (13 bits)
    - R1: FMSsmall-BS-th2 (13)
    - R2: FMSsmall-BS-th3 (13)
- Step 1: Latch the input data.
- Step 2: Make the DD Board Sum:
    - BS-DD = T-D(23) + B-D(23)

  Make 3 overlapping jet patches that cover the top, middle and bottom of the array:
    - JP-T = T-JP-AB + T-JP-CD
    - JP-M = T-JP-CD + B-JP-CD
    - JP-B = B-JP-AB + B_JP-CD
- Step 3: Compare BS-DD to the 3 thresholds and combine the results with the existing BS threshold bits:
    - BS3 = at least one BS value greater than th3
    - BS2 = at least one BS value greater than th2
    - BS1-T = T-BS1-ABC
    - BS1-M = T-BS1-CD or B-BS1-CD or BS1-DD
    - BS1-B = B-BS1-ABC

  Select the 8 LSB from each of the 3 JP values. Set the result to 255 (i,e, binary 11111111) if any higher order bits are set.
- Step 4: Latch the output data:
    - Bit 0 = Unused (NOTE: This bit is stuck in hardware so it cannot be used)
    - Bit 1 = BS2
    - Bit 2 = BS1-T
    - Bit 3 = BS1-M
    - Bit 4 – BS1-B
    - Bits 5:12 = JP-T

- Bits 13 = BS3
- Bits 14:15 = Unused
- Bits 16:23 = JP-M
- Bits 24:31 = JP-B

Large-Cell Layer 1 DSM Board

- RBT File: fms_fm103_2017_c.rbt
- Users: FM103 (South), FM104 (North)
- Input:
  - Channels 0/1 = FM005 or FM009 (Top/Side)
  - Channels 2/3 = FM006 or FM010 (Top)
  - Channels 4/5 = FM007 or FM011 (Bottom/Side)
  - Channels 6/7 = FM008 or FM012 (Bottom)

  From the Top and Bottom boards the DSM receives:
  - Bit 0 = BS3
  - Bit 1 = BS2
  - Bit 2 = BS1-EF
  - Bit 3 = Unused
  - Bits 4:15 = Unused
  - Bits 16:23 = JP-EF
  - Bits 24:31 = Unused

  From the Side boards the DSM receives:
  - Bit 0 = BS3
  - Bit 1 = BS2
  - Bit 2 = BS1-IJ
  - Bit 3 = BS1-GH
  - Bits 4:15 = J(23)
  - Bits 16:23 = JP-GH
  - Bits 24:31 = JP-IJ
- LUT: 1-to-1 mapping
- Registers: Three threshold registers for the BS logic:
  - R0: FMSlarge-BS-th1 (13 bits)
  - R1: FMSlarge-BS-th2 (13)
  - R2: FMSlarge-BS-th3 (13)
- Step 1: Latch the input data.
- Steps 2 and 3 combined: NOTE that this merged step is given 2 ticks of the clock to complete.
  - Make the JJ Board Sum: BS-JJ = T-J(23) + B-J(23)
    Compare BS-JJ to the 3 thresholds and combine the results with the existing BS threshold bits:

    BS3 = at least one BS value greater than th3
    BS2 = at least one BS value greater than th2
    BS1-T = T-BS1-EF or TS-BS1-GH
    BS1-M = TS-BS1-IJ or BS-BS1-IJ or BS1-JJ
    BS1-B = B-BS1-EF or BS-BS1-GH

- Make 3 overlapping jet patches that cover the top, middle and bottom of the array:
  JP-T = T-JP-EF + TS-JP-GH + TS-JP-IJ
  JP-M = TS-JP-IJ + BS-JP-IJ
  JP-B = B-JP-EF + BS-JP-GH + BS-JP-IJ
  Select the 8 LSB from each of the 3 JP values. Set the result to 255 (i,e, binary 11111111) if any higher order bits are set.

- Step 4: Latch the output data:
  - Bit 0 = BS3
  - Bit 1 = BS2
  - Bit 2 = BS1-T
  - Bit 3 = BS1-M
  - Bit 4 – BS1-B
  - Bits 5:12 = JP-T
  - Bits 13:15 = Unused
  - Bits 16:23 = JP-M
  - Bits 24:31 = JP-B

Layer 2 DSM Algorithm

The layer-2 DSM board will receive data from the FMS small and large cell layer-1 DSMS. The algorithm will combine the BS threshold data to give one set of BS information covering the full array. In parallel, the jet patches from the small and large cells will be combined to get six over-lapping jet patches. Those jet patches will be compared to three thresholds, and the threshold bits will be combined (OR). In addition, various combinations of BS1 and JP0 threshold bits will be flagged to provide a way to trigger on multi-cluster events. The selected combinations of BS1 bits are shown in Table 2, and the combinations of JP0 bits are shown in Table 3. The shaded elements of the table indicate the combinations are ARE selected.

	Small						Large					
	ST	SM	SB	NB	NM	NT	ST	SM	SB	NB	NM	NT
Small-South-T												
Small-South-M												
Small-South-B												
Small-North-B												
Small-North-M												
Small-North-T												
Large-South-T												
Large-South-M												
Large-South-B												
Large-North-B												
Large-North-M												
Large-North-T												

Table 2: Selected combinations of BS bits

	South-T	South-M	South-B	North-B	North-M	North-T
South-T						
South-M						
South-B						
North-B						
North-M						
North-T						

Table 3: Selected combinations of JP bits

The layer-2 algorithm will therefore operate as follows:

- RBT File: l1_fp201_2015_b.rbt
- Users: FP201
- Input:
  - Channels 0/1 = FM102, Small cells, North array
  - Channels 2/3 = FM103, Large cells, South array
  - Channels 4/5 = FM104, Large cells, North array
  - Channels 6/7 = FM101, Small cells, South array

  From each DSM the input is:
  - Bit 0 = BS3 (NOTE: From FM101 & 102 this bit is UNUSED)
  - Bit 1 = BS2
  - Bit 2 = BS1-T
  - Bit 3 = BS1-M
  - Bit 4 – BS1-B
  - Bits 5:12 = JP-T
  - Bits 13 = Unused (NOTE: From FM101 & 102 this is the re-routed BS3)
  - Bits 14:15 = Unused
  - Bits 16:23 = JP-M
  - Bits 24:31 = JP-B
- LUT: 1-to-1 mapping
- Registers: Three threshold registers for the JP logic:
  - R0: FMS-JP-th0 (9 bits)
  - R1: FMS-JP-th1 (9)
  - R2: FMS-JP-th2 (9)
- Step 1: Latch the input data.
- Step 2: Combine (OR) the BS3, BS2 and BS1 bits from all 4 inputs. In addition make the di-BS bit by looking for all the combinations of BS1 bits shown in Table 2.

  Make the six final jet patches by adding together the small and large cell sums for each patch, e.g.

    - JP-South-T = Small-South-JP-T + Large-South-JP-T
- Step 3: Compare each of the six jet patches to the three thresholds. Combine (OR) the results from all six jet patches for each threshold. In addition make the diJet bit by looking for all the combinations of JP0 bits shown in Table 3.
- Step 4: Latch the output data. The output data format is shown in Table 4.

Table 4: Output of Layer-2 FMS DSM Board

Bit	Name	Description
Bit 0	FMSsmall-BS3	FMS small-cell Board Sum threshold-3 bit
Bit 1	FMSsmall-BS2	FMS small-cell Board Sum threshold-2 bit
Bit 2	FMSsmall-BS1	FMS small-cell Board Sum threshold-1 bit
Bit 3	FMSlarge-BS3	FMS large-cell Board Sum threshold-3 bit
Bit 4	FMSlarge-BS2	FMS large-cell Board Sum threshold-2 bit
Bit 5	FMSlarge-BS1	FMS large-cell Board Sum threshold-1 bit
Bit 6	FMS-DiBS	FMS topology bit
Bit 7	FMS-JP2	FMS Jet Patch threshold-2 bit
Bit 8	FMS-JP1	FMS Jet Patch threshold-1 bit
Bit 9	FMS-JP0	FMS Jet Patch threshold-0 bit
Bit 10	FMS-DiJet	FMS Di-Jet topology bit
Bit 11	Unused	Unused
Bit 12	Unused	Unused
Bit 13	Unused	Unused
Bit 14	Unused	Unused
Bit 15	Unused	Unused