Second Bunch Crossing Counter DSM Algorithm

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RBT File: l1_bx202_2020_c.rbt

Users: BX202

Input

Input Channel	Bit Description
0	Lower 16 bits of BX201 output
1	Upper 16 bits of BX201 output
2:6	Unused
7	Bit 0 – RHIC synchronization bit (aka revtick)

LUTS: 1-to-1

Registers

Register	Register Description	Register Name
0	Initial counter value, 16 bits.	BX_StartValueUpper2Bytes
1	Number of filled bunches in a RHIC ring	BX_NumBunches
2	Start delay in units of 4xRHIC clock ticks	BX_7bit_Start_Delay

Output Bits

Bit	Description
Bits 0:15	Current 16-bit bunch crossing counter value
Bits 16:22	Current 7-bit bunch type counter value
Bits 23	Unused
Bits 24:30	2nd copy of Current 7-bit bunch type counter value
Bits 31	Unused

Internal Logic

- 16-bit bunch crossing counter increments by one only when input from BX201 changes from 0xffffffff to 0x00000000.
  - Counts only when DSM is running.
  - Counter starts at a user defined value (Reg0).
  - Current counter value is output on output bits 0:15
- 7-bit bunch type counter increments by one on each tick of the RHIC clock.
  - Logic waits for a user-defined number of 4xRHIC clock ticks (Reg2) AFTER the DSM board goes into RUN mode before it is activated.
  - Counting doesn't begin until the first revtick signal is received AFTER the logic has been activated. All subsequent revtick signals are ignored.
  - Counter always starts from zero (0)
  - Resets to zero (0) when it reaches Reg1 – 1, e.g.:
    - if Reg1 = 120 then the counter values range from 0 to 119
    - if Reg1 = 121 then the counter values range from 0 to 120
    - etc…
  - Current counter value is output on bits 16:22 and 24:30