A Detailed Description of the Cluster Finding Scheme for the FMS Trigger

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Change Log:

Date	Description
25th February 2009	Original version
3rd March 2009	Added in the description of the FE101 algorithm ("a" version) for FPE
25th March 2009	FP201 algorithm changed to reflect the fact that FPE actually comes in on channel 7 and not channel 6 ("b" version)
5th June 2009	Updated the FMS element numbering scheme, and all the equations, in this document to be consistent with the actual cable map. NOTE: the VHDL was always consistent with the cable map. However, this document, which was written before either the VHDL code or the cable map were finalized, was not consistent.
April 5, 2010	Added page numbers and re-formatted the table containing the FP201 output to help with downstream trigger configuration file management.

Starting in the 2009 RHIC running period we are aiming to trigger on clusters in the FMS. A cluster is characterized by a central cell, with a high ADC value, surrounded by eight neighbors with greater-than-average ADC values. The trigger algorithm will aim to detect the central cell, form the sum of the ADC values of all nine cells and then apply a threshold cut to that sum.

The trigger will be implemented at Level 0, i.e. in the QT-DSM tree. In order to maximize the trigger efficiency it will be necessary to trigger on clusters that span boundaries within the electronics chain. Reconstructing clusters that span boundaries is relatively difficult to do in the QT-DSM tree so it seems sensible to arrange the connections between the FMS cells, the QT boards and the DSM boards in such a way as to minimize the probability of a cluster spanning boundaries. The scheme that is described here has therefore been optimized to minimize the number of clusters that are split between multiple layer-0 DSM boards. The scheme also makes it as easy as possible to reconstruct those clusters that do still span multiple layer-0 DSM boards. There are two negative consequences of this optimization. One is that it will not be possible to reconstruct clusters that span the boundary between large and small cells. The other is that it will not be possible to reconstruct clusters that span the boundary between the North and South sides of the large-cell array. It should be noted that the small-cell array, and the two halves of the large-cell array, are physically distinct and separately enclosed with material in the boundary region. As a result there are currently no plans to analyze such clusters, so this is not considered to be a serious effect.

FMS Cell to QT Board Assignment Scheme

The FMS cells are assigned to QT boards using a geometrical scheme composed of a large set of simple rectangles. The assignment of FMS cells to the 4 QT8 cards within each QT board has been done using a "striping" scheme, where the stripes run along the length of the rectangles. This scheme is shown in Figure 1.

- All of the FMS cells that connect to the DSM tree are shown in Figure 1.
- The cells contained within a thin solid line are all connected to one QT board.
- Within each QT board the thick solid line marks the locations of clusters that are totally contained by that QT board.
- In 3 of the 4 quadrants the stripes, indicating which QT8 card a cell is assigned to, are shown in light and dark gray.
- In the upper right quadrant the stripes are shown in shades of blue and yellow.
- In this quadrant each QT board has a label from A to J. The 4 stripes in each QT board (representing the 4 QT8 cards) are labeled from 0 to 3. In the rest of this document individual QT8 cards are referred to using these reference numbers, e.g. A(1), E(0), etc….
- Finally, the cells are separated out into 3 groups, indicating which QT board is connected to each of 3 layer-0 DSMS.

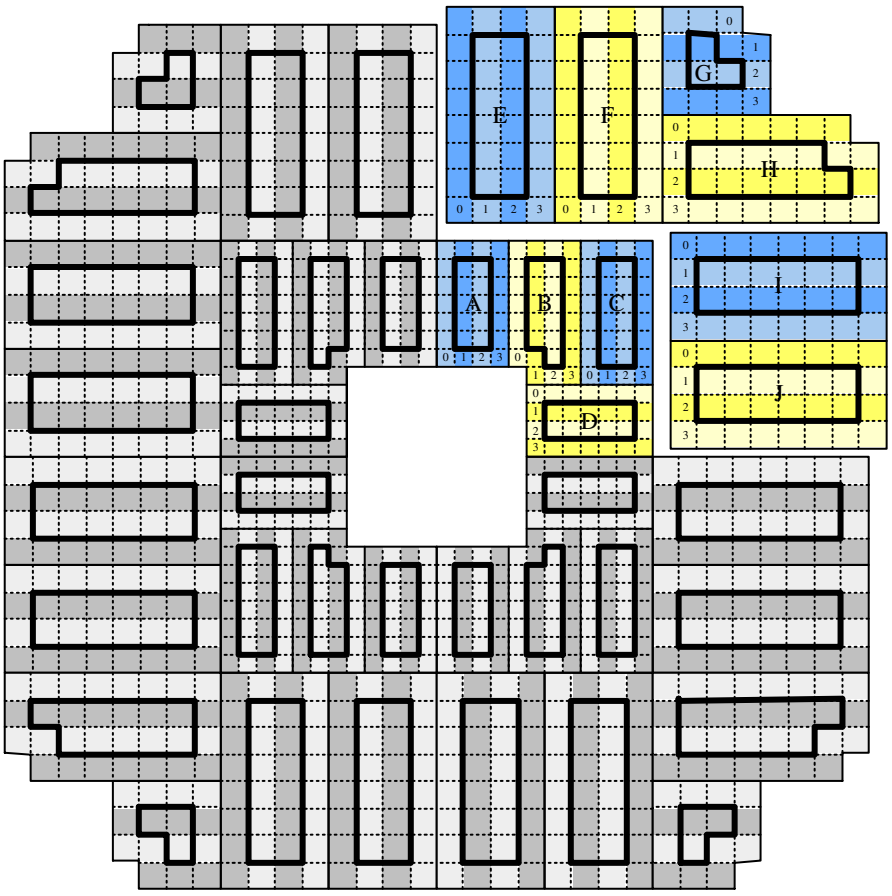

Figure 1: FMS Cell to QT and Layer-0-DSM Assignment Scheme

The algorithm in the QT boards is split between the QT8 daughter cards and the motherboard. The sum of ADC values from each QT8 card is calculated. In parallel, the cell with the highest ADC value is identified. The user has the option to exclude certain cells from the search for the highest ADC value. This makes it possible to ignore cells that fall on the boundaries as well as dead and noisy cells. A more detailed description will be provided by Chris Perkins.

The output of each QT board, which is sent to the layer 0 DSM boards, contains the following information:

QT8(0:3)	Sum of the ADC values from each of the 4 QT8 cards	4 x 5 bits
HT	ADC value from cell with the highest value	7 bits
HTID	ID of cell with the highest ADC value	5 bits

Within each QT board the numbering scheme used to assign ID values to the 8 channels of each of the four QT8 cards is:

ID	QT8
0:7	0
8:15	1
16:23	2
24:31	3

Layer 0 DSM Tree Algorithms

In the layer 0 DSM boards a cluster is then reconstructed by summing together the QT8-sum from the stripe that contains the highest cell with the stripes on either side of it:

Cluster-sum = QT8-sum(stripe(HTID)) + QT8-sum(stripe-1) + QT8-sum(stripe+1)

This logic is relatively simple to code in VHDL. So long as all 3 stripes are within one layer 0 DSM board it doesn't matter which QT board they come from. However, when the cell that contains the highest ADC value lies on the edge of a DSM's region, then things become more complicated. Data must be passed up to the layer 1 DSM board so the cluster can be completed there. In addition, if a cell is located where the orientation of the stripes changes, more than 3 stripes may need to be added together.

Table 1 shows the list of QT8 sums that need to be used to reconstruct a cluster located in any of the cells of the upper-right quadrant of the FMS, i.e. the colored part of Figure 1.

The columns in Table 1 are:

- DSM Board: The region of the FMS covered by this layer 0 DSM board
- QT: QT board reference letter from A to J
- HTID: ID of cell with the highest ADC value, which then forms the center of the cluster:

- Loc.: Geometric location of this cell (HTID) within the block of cells connected to this QT board:

TL = top left	T = top	TR = top right
LHS = left hand side	I = internal	R = right hand side
BL = bottom left	B = bottom	BR = bottom right

- List: A list of the QT8 sums that need to be added together to reconstruct this cluster. Only those QT8 sums that are available within this layer-0 DSM board are shown. If the cluster happens to lie on a boundary that the trigger will not span (e.g. the large-small cell boundary) then "Ignored by QT" will be listed, meaning the DSM will never receive those HTID values.
- No.: The number of cells that use this list.
- Action: A description of the action that is still needed to complete this cluster. This may include a list of QT8 sums from other layer 0 DSMS that need to be added in at layer 1. "Done" means that the cluster is complete. "Not feasible" means that it is not possible to add together all the necessary QT8 sums (5) in the time available so just the most useful subset are used.

Table 1: QT8 Lists for Cluster Reconstruction in Upper-Right Quadrant of the FMS

DSM Board	QT	HTID	Loc.	List	No.	Action
Small-cell quadrant	A	0,6,8,14,16,22,24,30	T,B	Ignored by QT	8	Not applicable
		1:5	LHS	A(0), A(1)	5	Add in A(0) from the next quadrant at layer 1
		9:13	I	A(0), A(1), A(2)	5	Done
		17:21	I	A(1), A(2), A(3)	5	Done
		25:29	RHS	A(2), A(3), B(0)	5	Done
	B	0,6,8,9,15,23,31	T,B	Ignored by QT	7	Not applicable
		1:5	LHS	A(3), B(0), B(1)	5	Done
		10:14	I	B(0), B(1), B(2)	5	Done
		16	B	B(1), B(2), B(3), D(0)	1	Done
		17:22	I	B(1), B(2), B(3)	6	Done
		24	BR	B(2), B(3), C(0), D(0)	1	Done
		25:30	RHS	B(2), B(3), C(0)	6	Done
	C	7,15,23,24:31	T,RHS	Ignored by QT	11	Not applicable
		0	BL	B(3), C(0), C(1), D(0)	1	Done
		1:6	LHS	B(3), C(0), C(1)	6	Done
		8	B	C(0), C(1), C(2), D(0)	1	Done
		9:14	I	C(0), C(1), C(2)	6	Done
		16	B	C(1), C(2), C(3), D(0)	1	Done
		17:22	I	C(1), C(2), C(3)	6	Done
	D	0,6,8,14,16,22,24,30	RHS, LHS	Ignored by QT	8	Not applicable
		1	T	B(1),B(2),B(3),D(0),D(1)	1	Not feasible. Use just D(0)+D(1)
		2	T	B(2),B(3),C(0),D(0),D(1)	1	Not feasible. Use just D(0)+D(1)

		3	T	B(3),C(0),C(1),D(0),D(1)	1	Not feasible. Use just D(0)+D(1)
		4	T	C(0),C(1),C(2),D(0),D(1)	1	Not feasible. Use just D(0)+D(1)
		5	T	C(1),C(2),C(3),D(0),D(1)	1	Not feasible. Use just D(0)+D(1)
		9:13	I	D(0), D(1), D(2)	5	Done
		17:21	I	D(1), D(2), D(3)	5	Done
		25:29	B	D(2), D(3)	5	Add in D(3) from the next quadrant at layer 1
Large-cell horizontal section	E	0:7,8,15,16,23,24,31	LHS,T,B	Ignored by QT	14	Not applicable
		9:14	I	E(0), E(1), E(2)	6	Done
		17:22	I	E(1), E(2), E(3)	6	Done
		25:30	RHS	E(2), E(3), F(0)	6	Done
	F	0,7,8,15,16,23,24,31	T,B	Ignored by QT	8	Not applicable
		1:6	LHS	E(3), F(0), F(1)	6	Done
		9:14	I	F(0), F(1), F(2)	6	Done
		17:22	I	F(1), F(2), F(3)	6	Done
		25	RHS	F(2),F(3),H(1),H(2),H(3)	1	Not feasible. Use just F(2)+F(3)
		26	RHS	F(2),F(3),H(0),H(1),H(2)	1	Not feasible. Use just F(2)+F(3)
		27	RHS	F(2),F(3),G(3),H(0),H(1)	1	Not feasible. Use just F(2)+F(3)
		28	RHS	F(2),F(3),G(2),G(3),H(0)	1	Not feasible. Use just F(2)+F(3)
		29	RHS	F(2),F(3),G(1),G(2),G(3)	1	Not feasible. Use just F(2)+F(3)
		30	RHS	F(2),F(3),G(0),G(1),G(2)	1	Not feasible. Use just F(2)+F(3)
	G	0:2,8,9,16,24	T,RHS	Ignored by QT	7	Not applicable
		10	I	G(0),G(1),G(2)	1	Done
		11	LHS	G(0), G(1), G(2), F(3)	1	Done
		17:18	I	G(1), G(2), G(3)	2	Done
		19	LHS	G(1), G(2), G(3), F(3)	1	Done

		25:26	B	G(2), G(3), H(0)	2	Done
		27	BR	G(2), G(3), H(0), F(3)	1	Done
	H	3:6,14,15,23,24,31	T,RHS,BL	Ignored by QT	9	Not applicable
		0	TL	F(3), G(3), H(0), H(1)	1	Done
		1:2	T	G(3), H(0), H(1)	2	Done
		8	LHS	F(3), H(0), H(1), H(2)	1	Done
		9:13	I	H(0), H(1), H(2)	5	Done
		16	LHS	F(3), H(1), H(2), H(3)	1	Done
		17:22	I	H(1), H(2), H(3)	6	Done
		25:30	B	H(2), H(3)	6	Add in I(0) at layer 1
Large-cell vertical section	I	0,7,8,15,16,23,24,31	LHS,RHS	Ignored by QT	8	Not applicable
		1:6	T	I(0), I(1)	6	Add in H(3) at layer 1
		9:14	I	I(0), I(1), I(2)	6	Done
		17:22	I	I(1), I(2), I(3)	6	Done
		25:30	B	I(2), I(3), J(0)	6	Done
	J	0,7,8,15,16,23,24,31	LHS,RHS	Ignored by QT	8	Not applicable
		1:6	T	I(3), J(0), J(1)	6	Done
		9:14	I	J(0), J(1), J(2)	6	Done
		17:22	I	J(1), J(2), J(3)	6	Done
		25:30	B	J(2), J(3)	6	Add in J(3) from the next quadrant at layer 1

Table 2 summarizes some information from Table 1. It can be seen that 88 out of the 293 total cells lie on a boundary and cannot be used for triggering. Half of these cells (42) lie on the outside edges of the array, i.e. the inner edge of the small cell array or the outer edge of the large cell array. The others lie on either the boundary between the large and small cells, or on the dividing line between the North and South sides of the large cell array. 166 of the remaining 207 cells (80%) produce clusters that can be fully reconstructed by the layer-0 DSM boards. These are the clusters listed as "Done" in Table 1. Another 28 clusters will be completed at layer 1. The last column of Table 2 has a count of the number of clusters that cannot be completed. All of these clusters lie in the regions were the orientation of the stripes switches between vertical and horizontal. Completing these clusters would require adding together five QT8 sums, and it was not possible to implement that logic in the algorithms given the timing constraints. They make up around 5% of the 207 non-boundary cells.

Table 2: Statistics for each Layer 0 DSM

DSM Board	Total Cells	Boundary Cells	Clusters completed in this DSM board	Clusters to be completed at layer 1	Clusters that cannot be completed
Small Cell quadrant	119	34	70	10	5
Large Cell horizontal section	110	38	60	6	6
Large Cell vertical section	64	16	36	12	0
Totals	293	88	166	28	11

Table 3 then shows which QT8 sums each layer 0 DSM board needs to pass up to layer 1 in order to complete those clusters that lie on the boundaries.

Table 3: QT8 Sums to be passed on to Layer 1

DSM Board	QT8 Sums passed to Layer 1
Small Cell quadrant	A(0) D(3)
Large Cell horizontal section	H(3)
Large Cell vertical section	I(0) J(3)

There will be 3 slightly different versions of the layer 0 algorithm: one for the DSM board that processes small cell data (QT A-D), a second algorithm for the DSM board that processes the upper/lower section of the large cell array (QT E-H) and a final version for the DSM board that process data from the side of the large cell array (QT I and J). They will operate as follows:

Small-Cell Layer 0 DSM Board: FMS_FM001

- RBT File: fms_fm001_2009_a.rbt
- Users: FM001, FM002, FM003, FM004
- Input: The QT board connections are reversed from what you might expect:
    - Channels 0/1 = QT Board D
    - Channels 2/3 = QT Board C
    - Channels 4/5 = QT Board B
    - Channels 6/7 = QT Board A

  From each board the DSM receives:
    - Bits 0:4 = QT8(0) sum
    - Bits 5:9 = QT8(1) sum
    - Bits 10:14 = QT8(2) sum
    - Bits 15:19 = QT8(3) sum
    - Bits 20:26 = HT
    - Bits 27:31 = HTID
- LUT: 1-to-1 mapping
- Registers: One register for the simple HT logic that runs in parallel to the cluster finding logic:
    - R0: FMSsmall-HT-th (7 bits)
- Step 1: Latch the input data.
- Step 2: Compare the HT values to each other, in pairs, and also compare each HT value to the threshold specified in R0. In parallel with this comparison logic, compute all the cluster sums that involve just 2 or 3 QT8 sums. Delay the HTID values and QT8 sum D(0) to Step 3. Delay QT8 sums A(0) and D(3) to Step 4.
- Step 3: Use the pair comparisons from Step 2 to determine which of the four QT boards produced the highest HT value. Use that information to select the associated cluster sum and the HT threshold bit. If the cluster sum is one of those that needs to be completed by adding in a 4^{th} QT8 sum, D(0), then add it in. In parallel with this, construct the extended HTID of the highest HT by prefixing the original HTID with a 2-bit integer to specify which of the 4 QT boards produced it (0 = A, 1 = B, 2 = C, 3 = D).
- Step 4: Latch the output data:
    - Bits 0:7 = Cluster sum associated with selected (highest) HT
    - Bits 8:14 = Extended HTID of selected HT
    - Bits 16:20 = QT8 sum A(0)
    - Bits 21:25 = QT8 sum D(3)
    - Bit 26 = HT threshold bit from selected HT

Large-Cell Layer 0 DSM Board: FMS_FM005 (Upper/Lower section of the array)

- RBT File: fms_fm005_2009_a.rbt
- Users: FM005, FM007, FM009, FM011
- Input: The QT board connections are reversed from what you might expect:
    - Channels 0/1 = QT Board H
    - Channels 2/3 = QT Board G
    - Channels 4/5 = QT Board F

- Channels 6/7 = QT Board E

From each board the DSM receives:

- Bits 0:4 = QT8(0) sum
- Bits 5:9 = QT8(1) sum
- Bits 10:14 = QT8(2) sum
- Bits 15:19 = QT8(3) sum
- Bits 20:26 = HT
- Bits 27:31 = HTID

- LUT: 1-to-1 mapping
- Registers: One register for the simple HT logic that runs in parallel to the cluster finding logic:
  - R0: FMSlarge-HT-th (7 bits)
- Step 1: Latch the input data.
- Step 2: Compare the HT values to each other, in pairs, and also compare each HT value to the threshold specified in R0. In parallel with this comparison logic, compute all the cluster sums that involve just 2 or 3 QT8 sums. Delay the HTID values and QT8 sum F(3) to Step 3. Delay QT8 sum H(3) to Step 4.
- Step 3: Use the pair comparisons from Step 2 to determine which of the four QT boards produced the highest HT value. Use that information to select the associated cluster sum and the HT threshold bit. If the cluster sum is one of those that needs to be completed by adding in a 4^{th} QT8 sum, F(3), then add it in. In parallel with this, construct the extended HTID of the highest HT by prefixing the original HTID with a 2-bit integer to specify which of the 4 QT boards produced it (0 = E, 1 = F, 2 = G, 3 = H).
- Step 4: Latch the output data:
  - Bits 0:7 = Cluster sum associated with selected (highest) HT
  - Bits 8:14 = Extended HTID of selected HT
  - Bits 16:20 = Unused
  - Bits 21:25 = QT8 sum H(3)
  - Bit 26 = HT threshold bit from selected HT

Large-Cell Layer 0 DSM Board: FMS_FM006 (Side section of the array)

- RBT File: fms_fm006_2009_a.rbt
- Users: FM006, FM008, FM010, FM012
- Input: The QT board connections are reversed from what you might expect:
  - Channels 0/1 = QT Board J
  - Channels 2/3 = QT Board I
  - Channels 4/5 = Unused
  - Channels 6/7 = Unused

  From each board the DSM receives:
  - Bits 0:4 = QT8(0) sum
  - Bits 5:9 = QT8(1) sum
  - Bits 10:14 = QT8(2) sum
  - Bits 15:19 = QT8(3) sum
  - Bits 20:26 = HT
  - Bits 27:31 = HTID

- LUT: 1-to-1 mapping
- Registers: One register for the simple HT logic that runs in parallel to the cluster finding logic:
    - R0: FMSlarge-HT-th (7 bits)
- Step 1: Latch the input data.
- Step 2: Compare the two HT values to each other, and also compare each HT value to the threshold specified in R0. In parallel with this comparison logic, compute all the cluster sums that involve just 2 or 3 QT8 sums. Delay the HTID values to Step 3. Delay QT8 sums I(0) and J(3) to Step 4.
- Step 3: Use the pair comparison from Step 2 to determine which of the two QT boards produced the highest HT value. Use that information to select the associated cluster sum and the HT threshold bit. In parallel with this, construct the extended HTID of the highest HT by prefixing the original HTID with a 2-bit integer to specify which of the 2 QT boards produced it (0 = I, 1 = J).
- Step 4: Latch the output data:
    - Bits 0:7 = Cluster sum associated with selected (highest) HT
    - Bits 8:14 = Extended HTID of selected HT
    - Bits 16:20 = QT8 sum I(0)
    - Bits 21:25 = QT8 sum J(3)
    - Bit 26 = HT threshold bit from selected HT

Layer 1 DSM Tree Configuration and Algorithm

From Figure 1 it can be seen that there are 4 layer 0 DSM boards of each type (Small Cell quadrant, etc…), one in each of four quadrants. This makes 12 layer 0 DSM boards in total. Since there are no plans to trigger on clusters that span the boundary between large and small cells there is no immediate need to bring the large and small cell data together in the DSM tree. By the same logic, there is no need to bring the data from the North and South sides of the large-cell array together. The connections from the layer 0 DSM boards to the layer 1 DSM boards have therefore been made as simple and as tightly packed as possible. The 4 boards covering the small cells will all connect to one layer 1 DSM board: FM101. The 4 boards covering the South side of the large cell array will connect to a second layer 1 DSM board (FM102), and the 4 boards covering the North side of the array will connect to the third and final layer 1 DSM board (FM103). This is shown in Figure 2. The blue stripes highlight the FMS regions covered by the QT8 sums that need to be passed from layer 0 to layer 1 in order to allow boundary clusters to be completed.

The layer 1 algorithms will complete the boundary clusters and apply three thresholds to each cluster sum. The output data will include both the cluster threshold bits and the HT threshold bits for each quadrant. The algorithm in the small cell layer 1 DSM board will be somewhat different from the algorithm in the large cell layer 1 DSM boards. The small cell layer 1 DSM board will receive data from four independent quadrants. It can treat each one separately and easily produce results for each quadrant. The large cell layer 1 DSM boards each receive data covering two quadrants of the detector, but that data is

split into four separate sections. They will each combine the data from their four sections to produce results for two quadrants.

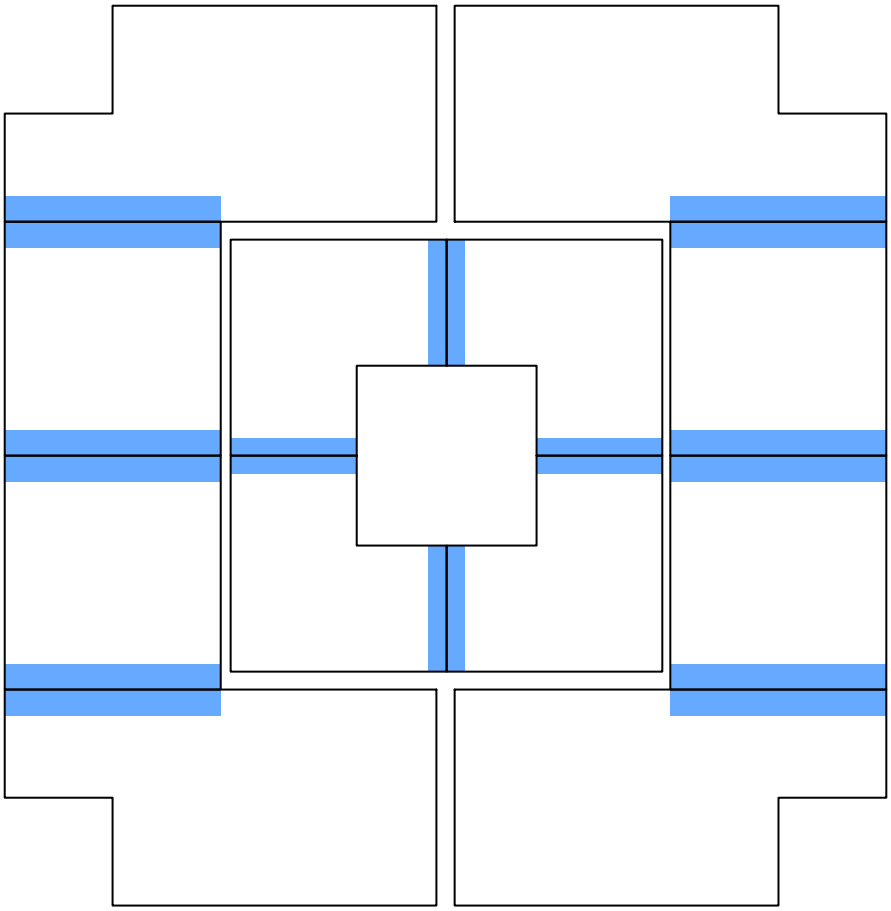

Figure 2: DSM Layer 0 to Layer 1 Assignment Scheme

The layer 1 DSM algorithms will therefore perform the following steps:

Small-Cell Layer 1 DSM Board: FMS_FM101

- RBT File: fms_fm101_2009_a.rbt
- Users: FM101
- Input:
    - Channels 0/1 = FM001, South-Top
    - Channels 2/3 = FM002, South-Bottom
    - Channels 4/5 = FM003, North-Top
    - Channels 6/7 = FM004, North-Bottom

  From each board the DSM receives:
    - Bits 0:7 = Cluster sum associated with selected (highest) HT
    - Bits 8:14 = Extended HTID of selected HT

    - Bits 16:20 = QT8 sum A(0)
    - Bits 21:25 = QT8 sum D(3)
    - Bit 26 = HT threshold bit from selected HT
- LUT: 1-to-1 mapping
- Registers: Three 8-bit registers for applying thresholds to the cluster sums:
    - R0: FMSsmall-cluster-th0
    - R1: FMSsmall-cluster-th1
    - R2: FMSsmall-cluster-th2
- Step 1: Latch the input data.
- Step 2: Delay the HTID values and the four input cluster sums to Step 3. In parallel, use those same input cluster sums and the input QT8 sums to complete all possible boundary clusters. For example, the input cluster sum from the South-Top quadrant is added to the QT8 A(0) sum from the North-Top quadrant. Separately it is also added to the QT8 D(3) sum from the South-Bottom quadrant. The result is 12 cluster sums; the 4 original input sums and 8 boundary sums. Delay the HT threshold bits to Step 4.
- Step 3: Compare each of the 12 cluster sums to the three thresholds specified in the registers. For each quadrant, use the HTID value to determine if the cluster lies on a boundary, and if so which one. Based on that determination, select the threshold bits from either the input cluster sum, the sum combined with A(0) or the sum combined with D(3).
- Step 4: Latch the output data:
    - Bits 0:2 = Cluster threshold bits from South-Top (ST) quadrant
    - Bits 3:5 = Cluster threshold bits from South-Bottom (SB) quadrant
    - Bits 6:8 = Cluster threshold bits from North-Top (NT) quadrant
    - Bits 9:11 = Cluster threshold bits from North-Bottom (NB) quadrant
    - Bits 12:15 = HT threshold bits (ST, SB, NT, NB)

Large-Cell Layer 1 DSM Board: FMS_FM102

- RBT File: fms_fm102_2009_a.rbt
- Users: FM102 (South), FM103 (North)
- Input:
    - Channels 0/1 = Top (FM005 and FM009)
    - Channels 2/3 = Upper-Side (FM006 and FM010)
    - Channels 4/5 = Bottom (FM007 and FM011)
    - Channels 6/7 = Lower-Side (FM008 and FM012)

  From the Top and Bottom boards the DSM receives:
    - Bits 0:7 = Cluster sum associated with selected (highest) HT
    - Bits 8:14 = Extended HTID of selected HT
    - Bits 16:20 = Unused
    - Bits 21:25 = QT8 sum H(3)
    - Bit 26 = HT threshold bit from selected HT

  From the Side boards the DSM receives:
    - Bits 0:7 = Cluster sum associated with selected (highest) HT
    - Bits 8:14 = Extended HTID of selected HT
    - Bits 16:20 = QT8 sum I(0)

    - Bits 21:25 = QT8 sum J(3)
    - Bit 26 = HT threshold bit from selected HT
- LUT: 1-to-1 mapping
- Registers: Three 8-bit registers for applying thresholds to the cluster sums:
    - R0: FMSlarge-cluster-th0
    - R1: FMSlarge-cluster-th1
    - R2: FMSlarge-cluster-th2
- Step 1: Latch the input data.
- Step 2: Delay the HTID values and the four input cluster sums to Step 3. In parallel, use those same input cluster sums and the input QT8 sums to complete all possible boundary clusters. For example, the input cluster sum from the Upper-Side section is added to the QT8 H(3) sum from the Top section. Separately it is also added to the QT8 J(3) sum from the Lower-Side section. The result is 10 cluster sums; the 4 original input sums and 6 boundary sums. Combine (OR) the HT threshold bits from the Top and Upper-Side sections to get a bit covering the whole Top quadrant. Also combine the Bottom and Lower-Side section threshold bits to get the bit for the Bottom quadrant.
- Step 3: Compare each of the 10 cluster sums to the three thresholds specified in the registers. For each section, use the HTID value to determine if the cluster lies on a boundary, and if so which one. Based on that determination, select the threshold bits from either the input cluster sum, or one of the boundary sums. Finally, combine (OR) the selected cluster threshold bits from the Top and Upper-Side sections to get the bits covering the whole Top quadrant. Do the same thing for the Bottom quadrant using the Bottom and Lower-Side sections. Delay the two HT threshold bits to Step 4.
- Step 4: Latch the output data:
    - Bits 0:2 = Cluster threshold bits from Top quadrant
    - Bits 3:5 = Cluster threshold bits from Bottom quadrant
    - Bits 6:7 = HT threshold bits (Top and Bottom)

FPD-East QT Algorithm

In parallel with the FMS, the FPD-East detector will also be taking data. The electronics chain involves 4 QT boards passing data to a layer 1 DSM board, which then sends its output to a common layer 2 DSM board, shared with the FMS. The QT board algorithm will add all 32 12-bit ADC values to produce a 17-bit sum. The user has the option, through the use of a register-settable mask, to exclude certain channels from the sum. This makes it possible to ignore dead or noisy cells. A more detailed description will be provided by Chris Perkins.

FPD-East Layer 1 DSM Algorithm

The layer 1 algorithm for FPD-East will combine the 4 input sums from the 4 QT boards to make two 18-bit module sums. Each of those sums will be compared to a threshold, and the threshold bits will be passed on to layer 2. The details of the FPD-East layer 1 DSM algorithm are as follows:

FPD-East Layer 1 DSM Board: MIX_FE101

- RBT File: mix_fe101_2009_a.rbt
- Users: FE101
- Input:
    - Channels 0/1 = Section 1 (FEQ-QT1)
    - Channels 2/3 = Section 2 (FEQ-QT2)
    - Channels 4/5 = Section 3 (FEQ-QT3)
    - Channels 6/7 = Section 4 (FEQ-QT4)

  From each board the DSM receives:
    - Bits 0:16 = Sum of 32 12-bit ADC values
- LUT: 1-to-1 mapping
- Registers: Two registers that are combined to make one 18-bit threshold value. NOTE: the maximum size of any register is 16 bits, which is too small for an 18-bit value.
    - R0: FPE-threshold-12LSB
    - R1: FPE-threshold-6MSB
- Step 1: Latch the input data.
- Step 2: Add the 17-bit input sums from QT1 and QT2 to produce the 18-bit sum for module 1. Add the 17-bit input sums from QT3 and QT4 to produce the 18-bit sum for module 2.
- Step 3: Compare each of the two module sums to the 18-bit threshold value formed by concatenating the values specified in R0 and R1.
- Step 4: Latch the output data:
    - Bit 0 = Threshold bit from module 1
    - Bit 1 = Threshold bit from module 2

Layer 2 DSM Algorithm

The layer 2 DSM board will receive data from the FMS small and large cell layer 1 DSMS and the FPE layer 1 DSM. The algorithm will combine the FMS data from the quadrants to give one set of threshold data covering the small cell array, and another set covering the large cell array. In addition, the number of quadrants with cluster threshold bits set will be counted. This will provide a way to trigger on multi-cluster events. The two FPE threshold bits will just be combined (OR) together. Therefore, the layer 2 algorithm will operate as follows:

- RBT File: l1_fp201_2009_b.rbt
- Users: FP201
- Input:
    - Channels 0/1 = FM101, FMS Small cells
    - Channels 2/3 = FM102, FMS Large cells, South side
    - Channels 4/5 = FM103, FMS Large cells, North side
    - Channel 6 = Unused
    - Channel 7 = FE101, FPE

From the small cell DSM the input is:
  - Bits 0:2 = Cluster threshold bits from South-Top (ST) quadrant
  - Bits 3:5 = Cluster threshold bits from South-Bottom (SB) quadrant
  - Bits 6:8 = Cluster threshold bits from North-Top (NT) quadrant
  - Bits 9:11 = Cluster threshold bits from North-Bottom (NB) quadrant
  - Bits 12:15 = HT threshold bits (ST, SB, NT, NB)

From the large cell DSMs the input is:
  - Bits 0:2 = Cluster threshold bits from Top quadrant
  - Bits 3:5 = Cluster threshold bits from Bottom quadrant
  - Bits 6:7 = HT threshold bits (Top and Bottom)

From the FPE DSM the input is:
  - Bit 0 = FPE module 1 threshold bit
  - Bit 1 = FPE module 2 threshold bit

- LUT: 1-to-1 mapping
- Registers: None
- Step 1: Latch the input data.
- Step 2: Combine (OR) the two FPE bits.
  For the FMS small and large cells separately:
  - Combine (OR) the FMS HT threshold bits from the Top and Bottom quadrants to make bits that cover the South and North sides.
  - Combine (OR) the FMS cluster threshold bits from the Top and Bottom quadrants to make bits that cover the South and North sides. These bits mean “at least one cluster was over threshold”.
  - In parallel, for each cluster threshold separately, count how many of the quadrant-based threshold bits are actually on.
- Step 3: Delay the FPE bit to Step 4. Combine the data for the North and South sides of each part of the FMS to make HT-threshold and cluster-threshold bits that cover the whole small cell array and the whole large cell array. For the small and large cells separately, for each cluster threshold, set a bit if the count of the number of “on” threshold bits is greater than 1. These bits mean “at least two quadrants had at least one cluster over threshold”.
- Step 4: Latch the output data. The output data format is shown in Table 4 (next page). In parallel, send a copy of this set of bits to the scaler system.

Table 4: Output of Layer 2 FPD/FMS DSM Board

Bit	Name	Description
Bit 0	FmsSmlCluster-th0	FMS small-cell cluster threshold-0 bit
Bit 1	FmsSmlCluster-th1	FMS small-cell cluster threshold-1 bit
Bit 2	FmsSmlCluster-th2	FMS small-cell cluster threshold-2 bit
Bit 3	FmsSmlMultCluster-th0	FMS small-cell multi-cluster threshold-0 bit
Bit 4	FmsSmlMultCluster-th1	FMS small-cell multi-cluster threshold-1 bit
Bit 5	FmsSmlMultCluster-th2	FMS small-cell multi-cluster threshold-2 bit
Bit 6	FmsSmlHiTwr-th	FMS small-cell HT threshold bit
Bit 7	FmsLrgCluster-th0	FMS large-cell cluster threshold-0 bit
Bit 8	FmsLrgCluster-th1	FMS large-cell cluster threshold-1 bit
Bit 9	FmsLrgCluster-th2	FMS large-cell cluster threshold-2 bit
Bit 10	FmsLrgMultCluster-th0	FMS large-cell multi-cluster threshold-0 bit
Bit 11	FmsLrgMultCluster-th1	FMS large-cell multi-cluster threshold-1 bit
Bit 12	FmsLrgMultCluster-th2	FMS large-cell multi-cluster threshold-2 bit
Bit 13	FmsLrgHiTwr-th	FMS large-cell HT threshold bit
Bit 14	FPE	FPE trigger bit
Bit 15	Unused	Unused