

Implementation and Algorithms for the FPD DSM Tree 2008 High Towers for FMS and Sums for FPDE

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Description: For FPD-East the first two layers of DSM boards build the ADC sum for the 2 remaining detector modules: North-East and South-East. Both of these sums are available in the third layer, which sets 3 thresholds on each sum and a 4th threshold on the sum of the North-East and South-East modules. For FMS the first layer of DSM boards compares the input ADC values to 2 thresholds. The results are OR'ed together as they move through the layers. A bit-mask is used to define which of the input ADC values contributes to the "OR". 5 bits are then sent to the last DSM; 3 from FPD-East and 2 from FMS. In parallel 7 threshold bits are sent to the scaler boards.

1. FPD East-layer0, FPE-FE001, 002, 003, 005, 006, 007, 008

Input: 16 8-bit ADC values

Registers: None

LUT: Pedestal subtraction

Action:

1 st Clock:	Latch input
2 nd Clock:	Form intermediate sums
3 rd Clock:	Add intermediate sums to 12-bit total sum
4 th Clock:	Latch output

Output (0-11) ADC sum,
(12-15) empty

2. FPD-East-layer0, FPE-FE004

Input: 2x7 8-bit ADC values; split module
Ch0-6 First sum
Ch7-13 Second sum
Ch14-15 Unused

Registers: None

LUT: Pedestal subtraction

Action:

1 st Clock:	Latch input
2 nd Clock:	Form intermediate sums

3rd Clock: Add intermediate sums to 11-bit total sum separately for channels 0-6 and channels 7-13
4th Clock: Latch output

Output (2 cables)
Lower bits First Sum
(0-10) ADC sum
(11-15) empty
Upper bits Second Sum
(16-26) ADC sum
(27-31) empty

3. FPD-East-layer1, FPE-FE101

Input: 8 ADC sums: 6 12-bit sums and 2 11-bit sums

Registers: **FPE**: Index 23
R0: Module mask (8)
This is a bit mask for the 8 inputs. For each input/bit: 0 => do not use this input in the sums logic, 1 => do use this input in the sum logic

LUT: 1:1

Action:
1st Clock: Latch input
2nd Clock: Zero out those inputs whose bit in R0 is 0 and then form intermediate sums
3rd Clock: Add intermediate sums to 14-bit module sums separately for inputs 0-3 and inputs 4-7.
4th Clock: Latch output

Output (2 cables)
Lower bits: sum of channels 0-3
(0-13) ADC sum
(14-15) empty
Upper bits: sum of channels 4-7
(16-29) ADC sum
(30-31) empty

4. FMS-layer0, FMS-FM001-011

Input: 4 12-bit ADC values

Registers: **FMS**: Indices 16, 17, 18, 20, 21, 22, 24, 25, 26, 28, 29, 30
R0: Threshold 0 (12 bits)
R1: Threshold 1 (12 bits)
R2: On/Off bit-mask (4 bits)

LUT: Pedestal subtraction

Action:

1st Clock: Latch input
2nd Clock: Compare each of the 4 ADC values to the 2 thresholds.
3rd Clock: Combine the results for each ADC with its bit in the mask (register 2) and then OR the results for each threshold
Bit(0) = (ADC(0) > th0 AND reg2(0) = 1) OR
(ADC(1) > th0 AND reg2(1) = 1) OR
etc...
4th Clock: Latch output

Output (0) At least 1 un-masked ADC > threshold 0
(1) At least 1 un-masked ADC > threshold 1
(2-15) empty

5. FMS layer1, FMS-FM101, 102, 103 and 104

Input: 3 pairs of threshold bits

Registers:

None

LUT: 1:1

Action:

1st Clock: Latch input
2nd Clock: OR the bits for threshold 0
OR the bits for threshold 1
3rd Clock: Delay output
4th Clock: Latch output

Output (2 cables)

(0) At least 1 ADC > threshold 0
(1) At least 1 ADC > threshold 1
(2-31) Empty

6. FPD-layer2, L1-FP201

NOTE: In 2007 this algorithm used 4 override cycles to make time to compute all the large sums and do the threshold comparisons. To compensate for the extra time 1 of the 2 blanks in the output FIFO was removed. This year, 2008, the large sums for FPD++ have been removed, and replaced with the much simpler high-tower logic for FMS, so the override cycles are no longer used and the blank must be returned to the FIFO.

Input: One ADC sum per FPD-East detector module

ch0: East-North

ch1: East-South

ch2: Unused

ch3: Unused

A pair of high-tower bits from each FMS quadrant

ch4: ? quadrant

ch5: ? quadrant
ch6: ? quadrant
ch7: ? quadrant

Registers: **L1**: index: 30

R0: East ADC-threshold 0 (14)
R1: East ADC-threshold 1 (14)
R2: East ADC-threshold 2 (14)
R3: Sum_E threshold 0 (15)

LUT: 1:1

Action:

1st Clock: Latch input
2nd Clock: Place 3 thresholds (R0, R1 and R2) on each of the 2 FPD East inputs.
Form sum Sum_E = East-North + East-South
Combine (OR) the 4 FMS bits for threshold 0 and, separately, the 4 bits for threshold 1
3rd Clock: Compare FPD Sum_E to R3
Combine FPD-East threshold bits to form desired trigger bits and scaler bits (see output list below)
Delay FMS HT bits
4th Clock: Latch output

Output (2 cables)

Lower bits to last DSM LD301
(0) At least one FMS ADC > threshold 0
(1) At least one FMS ADC > threshold 1
(2-4) Unused
(5) Either FPD-East module > R1
(6) Either FPD-East module > R2
(7) NE > R0 and SE > R0 and Sum_E > R3
(8-15) empty

Upper bits to FPD scaler

(0) NE > R1
(1) SE > R1
(2) NE > R2
(3) SE > R2
(4) NE > R0 and SE > R0 and Sum_E > R9
(5) At least one FMS ADC > threshold 0
(6) At least one FMS ADC > threshold 1
(7-15) Unused