

Last DSM Algorithm  
2007 Version

4<sup>th</sup> June 2007

Input Bits

NOTE: Only those bits that are used are listed here.

Input Channel	Bit Description
0	CTB Information Bits 0:15 – CTB ADC sum
1	VTX Information Bit 0 – BBC TAC difference in window Bit 1 – ZDC TAC difference in window Bits 2:3 – Unused Bit 4 – BBC East large-tile ADC sum over threshold 0 Bit 5 – BBC West large-tile ADC sum over threshold 0 Bit 6 – ZDC East ADC sum over threshold 0 Bit 7 – ZDC West ADC sum over threshold 0 Bit 8 – ZDC East TAC in window Bit 9 – ZDC West TAC in window Bits 10:13 – Unused Bit 14 – ZDC East ADC sum over threshold 1 Bit 15 – ZDC West ADC sum over threshold 1
2	VPD and MTD Information Bit 0 – VPD TAC difference in window 0 Bit 1 – VPD TAC difference in window 1 Bits 2:5 – Unused Bit 6 – MTD bit Bits 7:15 - Unused
3	EMC Information Bits 0:1 – Unused Bits 2:3 – BEMC high-tower threshold bits Bits 4:8 – Unused Bits 9:10 – EEMC high-tower threshold bits Bits 11:15 – Unused
4	Scaler Source Patch Panel Bits 0:1 – Unused Bits 2:9 – Detector Groups 0:7 status (1=Live, 0=Busy) Bit 10 – Unused Bit 11 – FMS LED Bits 12:15 - Unused
5	FPD Information Bit 0:7 – Various FPDE and FPD++ threshold bits Bits 8:15 - Unused
6	Special Trigger Requests Bits 0:13 - Unused Bit 14 – Zero-bias bit Bit 15 - Unused
7	Unused

## Registers

Register	Register Description
0	8-bit mask for FPD
1	16-bit CTB threshold
2	16-bit CTB threshold for lower edge of UPC window
3	16-bit CTB threshold for upper edge of UPC window
4	Bitmask to include/exclude detector groups from the live logic
5	Pre-scale for ZDCxLive logic

## Output Bits

Bit	Description
Bits 0:15	
0	MTD
1	FMS LED
2	FPD
3	CTB
4	BBC-Large Coincidence
5/6	BEMC HT bits (coding three thresholds)
7	DetLive
8	UPC
9	EEMC HT > low threshold
10	BBC TAC difference in window
11	VPD TAC difference in window 0
12	VPD TAC difference in window 1
13	ZDCxLive Pre-scale
14	ZDC
15	Zero bias
Bits 16:31	Same definitions as bits 0:15

## Internal Logic

- The MTD input bit received on channel 2 is passed through to the output unmodified
- The FMS LED input bit received on channel 4 is passed through to the output unmodified
- The 8-bit FPD input is masked with register 0  
The bits in the masked set are then OR'ed together to create the FPD bit, i.e.:  
FPD = (masked bit 0) OR (masked bit 1) OR (masked bit 2) OR etc...
- The 16-bit CTB ADC sum is compared to the threshold in register 1 and the result is "1" if the multiplicity is greater than the threshold.
- The BBC coincidence bit is set if both of the large tile ADC sums are over threshold.
- The BEMC high tower input bits received on channel 3 are passed through to the output unmodified

- The 8 detector group status bits are masked with the corresponding bits in register 4 and the results for the included detectors are combined to generate one bit meaning “all included detector groups are live”, i.e.

$$\text{DetLive} = ((\text{status}(0) \text{ and } \text{reg4}(0)) \text{ or } \text{not } \text{reg4}(0)) \text{ AND} \\ ((\text{status}(1) \text{ and } \text{reg4}(1)) \text{ or } \text{not } \text{reg4}(1)) \text{ AND etc....}$$
- The 16-bit CTB ADC sum is compared to the thresholds in registers 2 and 3. The result of each comparison is “1” if the multiplicity is greater than the threshold. The results are combined to determine if the CTB multiplicity is inside a window defined by the two thresholds, i.e.:

$$\text{CTB-in-UPC-window} = \text{multiplicity greater than } \text{reg2} \text{ AND NOT greater than } \text{reg3}$$

The BBC veto is set if either of the large tile ADC sums are over threshold  
The ZDC veto is set if either of the ZDC ADC sums is over the second threshold (th1)  
The UPC bit is generated by combining all of these bits with the ZDC bit (see below for definition of the ZDC bit). i.e.:

$$\text{UPC} = \text{ZDC and not ZDC-veto and not BBC-veto and CTB-in-UPC-window}$$
- The EEMC bit is an OR of the two EEMC HT bits received from EM201 on Input Channel 3.
- The BBC TAC difference bit is a copy of the one received from VT201 on Input Channel 1. It is formed from the difference between the TAC values of the fastest GOOD hits on each side (East and West). A “good” hit is defined as one in which the ADC value was over threshold and its associated TAC value was inside a window.  
NOTE: The BBC TAC difference bit has not been combined with any of the BBC ADC sum threshold bits. As a result the logic can be satisfied if there is exactly one good hit on each side of the BBC.
- The two VPD TAC difference bits are formed in the same way as the single BBC TAC difference bit. Two bits are produced for the VPD by applying two separate windows, as opposed to the single window applied to the BBC.
- The ZDC bit is created from an AND of many incoming ZDC bits, i.e.:

$$\text{ZDC} = \text{ZDC TAC difference in window AND} \\ \text{ZDC East ADC sum over threshold 0 AND} \\ \text{ZDC West ADC sum over threshold 0 AND} \\ \text{ZDC East TAC in window AND} \\ \text{ZDC West TAC in window}$$
- The ZDC and DetLive bits are combined, i.e.:

$$\text{ZDCxLive} = \text{ZDC AND DetLive}$$

The ZDCxLive bit is pre-scaled using the 8-bit value specified in register 5. The output bit is set when the pre-scale counter reaches 1, at which point the counter is reset to the starting value specified in register 5.
- The zero-bias input bit received on channel 6 is passed through to the output unmodified.