

Last DSM Algorithm
 2008 Version G – PP2PP Running
 L1_ld301_2008_g.rbt

6th March 2008

Input Bits

NOTE: Only those bits that are used in this algorithm are listed here.

Input Channel	Bit Description
0	CTB Information Bits 0:15 – CTB multiplicity
1	VTX Information Bit 0 – BBC TAC difference in window Bits 1:15 – Unused
2	VPD and pp2pp Information Bit 0 – VPD TAC difference in window-0 Bit 1:6 – Unused Bit 7 – pp2pp ET Bit 8 – pp2pp IT Bit 9 – pp2p IEV Bit 10 – pp2pp IEH Bit 11 – pp2pp Single HIT Bits 12:15 – Unused
3	EMC Information Bits 0:1 – Barrel JP bits (thresholds #0, #1 and #2 coded into 2 bits) Bits 2:3 – Barrel HT bits Bits 4:8 – Unused Bits 9:10 – Endcap HT bits Bits 11:15 – Unused
4	RAT Board Bits 0 - TOF Bits 1:10 – Unused Bit 11 – FMS LED Bits 12:15 - Unused
5	FPD Information Bit 0 – Unused Bit 1 – FMS HT threshold-1 Bits 2:15 – Unused
6	Special Trigger Requests Bits 0:13 - Unused Bit 14 – Zero-bias bit Bit 15 - Random
7	Unused

Registers

Register	Register Description
0	CTB Multiplicity Threshold (16 bits)

Output Bits

Bit	Description
Bits 0:15	
0	Pp2pp-ET
1	Pp2pp-IT
2	Pp2pp-IEV
3	Pp2pp-IEH
4	Pp2pp-single-HI
5	CTB
6	VPD
7	BBC
8	FMS
9	BEMC HT0
10	BEMC JP0
11	EEMC HT0
12	RAT0
13	RAT11
14	Random
15	Zero bias
Bits 16:31	Same definitions as bits 0:15

Internal Logic

- The CTB multiplicity received on channel 0 is compared to the threshold specified in register 0. The result is 1 if the input multiplicity is greater than the threshold value.
- The BEMC and EEMC HT and JP bits received on channel 3 are unpacked and the lowest-threshold bits are selected for output
- All the remaining bits are passed through to the output unmodified.