

Last DSM Algorithm  
2009 Version A – PP Running

26<sup>th</sup> February 2009

Input Bits

NOTE: Only those bits that are used in this algorithm are listed here.

Input Channel	Bit Description
0	TOF Information Unused
1	VTX Information Bit 0 – BBC TAC difference in window Bit 1 – BBC East ADC sum > threshold Bit 2 – BBC West ADC sum > threshold Bits 3:5 – Unused Bit 6 – ZDC TAC difference in window Bit 7 – ZDC East ADC sum > threshold Bit 8 – ZDC West ADC sum > threshold Bit 9 – ZDC East Front ADC > threshold Bit 10 – ZDC East Back ADC > threshold Bit 11 – ZDC West Front ADC > threshold Bit 12 – ZDC West Back ADC > threshold Bit 13 – VPD TAC difference in window Bit 14 – VPD East ADC sum > threshold Bit 15 – VPD West ADC sum > threshold
2	TOF Information Unused
3	EMC Information Bits 0:3 – Barrel HT bits (NOTE: these bits are NOT packed) Bits 4:5 – Endcap HT bits (NOTE: these bits are NOT unpacked) Bits 6:15 – Unused
4	RAT Board Unused
5	FMS/FPD Information Bit 0 – FMS small-cell cluster > threshold Bits 1:6 – Unused Bit 7 – FMS large-cell cluster > threshold Bits 8:15 – Unused
6	Special Trigger Requests Bits 0:13 – Unused Bit 14 – Zero-bias bit Bit 15 – Unused
7	Unused

Registers

None

## Output Bits

Bit	Description
Bits 0:15	
0	BBC TAC difference in window
1	BBC East ADC sum > threshold
2	BBC West ADC sum > threshold
3	ZDC TAC difference in window
4	ZDC East ADC sum > threshold
5	ZDC West ADC sum > threshold
6	ZDC East Front ADC > threshold
7	ZDC East Back ADC > threshold
8	ZDC West Front ADC > threshold
9	ZDC West Back ADC > threshold
10	VPD TAC difference in window
11	VPD East ADC sum > threshold
12	VPD West ADC sum > threshold
13	EMC
14	FMS
15	Zero Bias
Bits 16:31	Same definitions as bits 0:15

## Internal Logic

- The BBC, ZDC and VPD input bits received on channel 1 are passed through to the output unmodified
- The least significant BEMC HT input bit (input channel 3, bit 0) and EEMC HT input bit (input channel 3, bit 4) are combined (OR'ed) to make the EMC bit.
- The two FMS cluster bits received on channel 5 are combined (OR'ed) to make the FMS bit.
- The zero-bias input bit received on channel 6 is passed through to the output unmodified.