

Last DSM Algorithm  
2009 Version I – Tune Algorithm

22<sup>nd</sup> April 2009

Input Bits

NOTE: Only those bits that are used in this algorithm are listed here.

Input Channel	Bit Description	Name
0	TOF Information Unused	
1	VTX Information Bit 0 – BBC TAC difference in window Bit 1 – BBC East ADC sum > threshold Bit 2 – BBC West ADC sum > threshold Bits 3:5 – Unused Bit 6 – ZDC TAC difference in window Bit 7 – ZDC East ADC sum > threshold Bit 8 – ZDC West ADC sum > threshold Bit 9 – ZDC East Front ADC > threshold Bit 10 – ZDC East Back ADC > threshold Bit 11 – ZDC West Front ADC > threshold Bit 12 – ZDC West Back ADC > threshold Bit 13 – VPD TAC difference in window Bit 14 – VPD East ADC sum > threshold Bit 15 – VPD West ADC sum > threshold	BBC-TAC BBCE BBCW  ZDC-TAC ZDCE ZDCW ZDCE-Front ZDCE-Back ZDCW-Front ZDCW-Back VPD-TAC VPDE VPDW
2	TOF Information Unused	
3	EMC Information Bits 0:3 – Barrel HT bits Bits 4:5 – Endcap HT bits Bits 6:15 – Unused	BHT(0:3) EHT2 and EHT4
4	RAT Board Unused	
5	FMS/FPD Information Bit 0:2 – FMS small-cell cluster threshold bits Bit 3:5 – FMS small-cell multi-cluster threshold bits Bit 6 – FMS small-cell HT threshold bit Bits 7:9 – FMS large-cell cluster threshold bits Bit 10:12 – FMS large-cell multi-cluster threshold bits Bit 13 – FMS large-cell HT threshold bit Bits 14:15 – Unused	FMS-small(0:2) FMS-s-multi(0:2) FMS-small-HT FMS-large(0:2) FMS-l-multi(0:2) FMS-large-HT
6	Special Trigger Requests Bits 0:13 – Unused Bit 14 – Zero-bias bit Bit 15 – Unused	
7	Unused	

## Registers

Register Number	Name	Size (bits)
0	FMS-Select	3

## Output Bits

Bit	Description
Bits 0:15	
0	BBC TAC difference in window
1	BBC East ADC sum > threshold
2	BBC West ADC sum > threshold
3	ZDC TAC difference in window
4	ZDC East ADC sum > threshold
5	ZDC West ADC sum > threshold
6	ZDC East Front ADC > threshold
7	ZDC East Back ADC > threshold
8	ZDC West Front ADC > threshold
9	ZDC West Back ADC > threshold
10	VPD TAC difference in window
11	VPD East ADC sum > threshold
12	VPD West ADC sum > threshold
13	EMC
14	FMS
15	Zero Bias
Bits 16:31	Same definitions as bits 0:15

## Internal Logic

- The BBC, ZDC and VPD input bits received on channel 1 are passed through to the output unmodified
- The least significant BEMC HT input bit (input channel 3, bit 0) and EEMC HT input bit (input channel 3, bit 4) are combined (OR'ed) to make the EMC bit.
- The FMS bit is a combination (OR) of bits from the FMS single-cluster, multi-cluster and high tower logic. The bits in register 0 are used to turn each component on and off.  
**FMS** = ([FMS-small(1) or FMS-large(1)] and reg0(0)) or  
([FMS-small-HT or FMS-large-HT] and reg0(1)) or  
([FMS-s-multi or FMS-l-multi or (FMS-small(0) and FMS-large(0))] and reg0(2))
- The zero-bias input bit received on channel 6 is passed through to the output unmodified.