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Implementation of QT Algorithm for STAR BBC Large Tiles

QT Code Version: 0x5f
MCS File: qt32b_l0_v5_f.mcs

Description:

This algorithm outputs the Maximum TAC value from daughter cards A and B, the Maximum TAC value from daughter cards C and D, a Good Hit bit from daughter cards A and B, and a Good Hit bit from daughter cards C and D. This corresponds to the maximum TAC for East and West and Good Hit bits for East and West because of the way the daughter cards are cabled.

Only channels that satisfy the "Good Hit" requirement are considered for the Maximum TAC value. If there are no channels that satisfy the "Good Hit" requirement, the corresponding Maximum TAC value will be zero. A "Good Hit" is defined as one where the ADC value is greater than some threshold and the corresponding TAC value is greater than TAC_MIN and less than TAC_MAX.

The Good Hit bit is high when any channel on the corresponding daughter cards satisfies the "Good Hit" requirement as defined above.

The channel mask register can be used but note that the ADC and TAC channels must be masked individually.

Inputs:

QT8A :
- Ch 0/1/2/3 : BBC Large Tile East ADC
- Ch 4/5/6/7 : BBC Large Tile East TAC

QT8B :
- Ch 0/1/2/3 : BBC Large Tile East ADC
- Ch 4/5/6/7 : BBC Large Tile East TAC

QT8C :
- Ch 0/1/2/3 : BBC Large Tile West ADC
- Ch 4/5/6/7 : BBC Large Tile West TAC

QT8D :
- Ch 0/1/2/3 : BBC Large Tile West ADC
- Ch 4/5/6/7 : BBC Large Tile West TAC

Registers (1 Set Per Daughter Card)**:**

Alg. Reg. 0 (Reg 13): "Good Hit" ADC_Threshold	(12 bits, unsigned)
Alg. Reg. 1 (Reg 14): "Good Hit" TAC_Min	(12 bits, unsigned)
Alg. Reg. 2 (Reg 15): "Good Hit" TAC_Max	(12 bits, unsigned)

Reg. 11 : Channel Mask

LUT:

TAC timing adjustment/ADC Pedestal subtraction for each channel

Algorithm Latch: 1

L0 Output to DSM:

(0-11)	:	Maximum TAC From Daughters A and B (East)
(12-23)	:	Maximum TAC From Daughters C and D (West)
(24)	:	Good Hit Bit From Daughters A and B (East)
(25)	:	Good Hit Bit From Daughters C and D (West)
(26-31)	:	'0'