Implementation of QT Algorithm for ZDC SMD
Run 2011
qt32b_l0_v6_3.mcs

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(Updated output bit list in documentation 09/03/2021)

Description:

This algorithm outputs the ID of the highest channel from each daughter card. If either all the channels on QT8A OR all the channels on QT8B are '0', the QT8B max ID is set to '7'. If either all the channels on QT8C OR all the channels on QT8D are '0', the QT8D max ID is set to '7'. This corresponds to the LED channel for both East and West and is masked from the algorithm. In this case, the QT8A (or QT8C) max ID may or may not be valid and should be ignored.

In the production configurations, the LED channel is masked from the algorithm for the East and West strips.

Inputs:

QT8A: WH1, WH2, WH3, WH4, WH5, WH6, WH7, WH8
QT8B: WV1, WV2, WV3, WV4, WV5, WV6, WV7, WLED
QT8C: EH1, EH2, EH3, EH4, EH5, EH6, EH7, EH8
QT8D: EV1, EV2, EV3, EV4, EV5, EV6, EV7, ELED

Registers (1 Set Per Daughter Card)**:**

None

LUT:

Pedestal subtraction for each channel

Algorithm Latch: 1

Action (21x RHIC Clock)**:**

1st: Mask channels and Latch inputs
If mask bit = 1, channel data = 0

2nd: Max(ch0, ch1) → Int_max_0
Max(ch2, ch3) → Int_max_1
Max(ch4, ch5) → Int_max_2
Max(ch6, ch7) → Int_max_3

3rd: Max(Int_max_0, Int_max_1) → Int_max_4
Max(Int_max_2, Int_max_3) → Int_max_5

4th: Max(Int_max_4, Int_max_5) → Int_max_6
5th: Delay Int_max_6 for DB, DD → Int_max_6_del1
Latch out Int_max_6 and ID for DA, DC

6th: Delay Int_max_6 for DB, DD → Int_max_6_del2
Latch in Int_max_6 and ID for DA, DC into DB, DD

7th: If Int_max_6 is '0' for DA or DB : ID_B_OUT → "111"
Else ID_B_OUT → Int_max_6_del2
If Int_max_6 is '0' for DC or DD : ID_D_OUT → "111"
Else ID_D_OUT → Int_max_6_del2
Delay Int_Max_6 for DA, DC on DB, DD → ID_A_OUT, ID_C_OUT

8th: Latch out ID_A_OUT, ID_B_OUT from DB
Delay ID_C_OUT, ID_D_OUT on DD

9th: Latch in ID_A_OUT, ID_B_OUT into DC
Delay ID_C_OUT, ID_D_OUT on DD

10th: Latch out ID_A_OUT, ID_B_OUT from DC
Delay ID_C_OUT, ID_D_OUT on DD

10th: Latch in ID_A_OUT, ID_B_OUT into DD
Delay ID_C_OUT, ID_D_OUT on DD

12th: Latch all bits out to L0 FPGA from DD

L0 Output to DSM:

(0-2) : Max DA ID
(3-5) : Max DB ID
(6-8) : Max DC ID
(9-11) : Max DD ID
(12-15) : '0'
(16-18) : Max DA ID
(19-21) : Max DB ID
(22-24) : Max DC ID
(25-27) : Max DD ID
(28-31) : '0'