Implementation of QT Algorithm for Test Pulse Input
qt32b_l0_v7_c.mcs

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Description:

This algorithm is design for use with a generic test pulse input. An ADC threshold cut is applied to all 32 channels. An output bit is set to 1 if any of those ADC values are above threshold. The output bit can be delayed by up to 15 full RHIC clock ticks in order to align it with any other layer in the STAR Level-0 Trigger System. The standard channel mask registers can be used for each channel to mask out that channel completely from the trigger but retain the data in the data-stream.

An outline of the steps followed by this algorithm is:

1. Apply channel masks
2. Compare ADC values to thresholds
3. OR the threshold bits
4. Optionally, delay the result by several full RHIC clock ticks
5. Delay the result to wait for data from the preceding QT8 daughter card
6. Combine the local and external data
7. Drive the output to the next QT8 daughter card or the mother board

NOTE: The existing delays, which are common to all QT algorithms, are unchanged by the addition of the extra delay in this algorithm and still function as normal. The Algorithm Latch on each QT8 daughter card is therefore still used to make sure the data trickles down correctly through all the daughter cards to the mother board. The Output Latch Delay on the mother board is still used to phase-adjust the final mother board output bits so they can be properly latched into a downstream DSM or TCU board.

Inputs:
QT8A: 8 PMT ADC
QT8B: 8 PMT ADC
QT8C: 8 PMT ADC
QT8D: 8 PMT ADC

Registers (1 Set Per Daughter Card)**:**
Reg. 11: Channel Mask (8 bits)
Alg. Reg. 0 (Reg 13): Test_QT_ADC_Threshold (12 bits)
Alg. Reg. 1 (Reg 14): Test_QT_RS_Delay (4 bits)
NOTE: The Channel Mask register is a bitmask.
A "0" turns a channel ON in the logic and a "1" turns it off.

LUT:
Timing adjustments/pedestal subtraction for each PMT

Algorithm Latch: TBD

L0 Output to DSM:
(0) OR of all 32 threshold bits
(1-31) '0'

Actions:

Tick	QT8A	QT8B	QT8C	QT8D
1	Latch inputs	Same as QT8A	Same as QT8A	Same as QT8A
2	Apply Channel_Mask	Same as QT8A	Same as QT8A	Same as QT8A
3	ADC > R0 -> ADC_GOOD	Same as QT8A	Same as QT8A	Same as QT8A
4	Combine (OR) ADC_Good bits	Same as QT8A	Same as QT8A	Same as QT8A
5	Select current OR or RS-delayed OR as specified by R1	Same as QT8A	Same as QT8A	Same as QT8A
6	Latch selected OR bit	Delay selected OR bit	Delay selected OR bit	Delay selected OR bit
7	Delay selected OR bit	Delay	Delay	Delay
8	Latch out OR bit	Delay	Delay	Delay
9		Latch in OR bit from upstream QT8 Latch selected OR bit	Delay	Delay
10		Combine (OR) selected & upstream bits	Delay	Delay
11		Latch out OR bit	Delay	Delay
12			Latch in OR bit from upstream QT8 Latch selected OR bit	Delay
13			Combine (OR) selected & upstream bits	Delay
14			Latch out OR bit	Delay
15				Latch in OR bit from upstream QT8 Latch selected OR bit
16				Combine (OR) selected & upstream bits
17				Latch out OR bit