TCU 09 memory map (28 April 2009)

Overview

Memory Block	*Starting Address*	*Ending Address*	*Number of Addresses*	*Data Mask*
Mother CSRs	0x YY00 0000	0x YY00 00FC	64	Various
Daughter CSRs	0x YY00 0100	0x YY00 01FC	64	Various
Trigger Registers	0x YY10 0000	0x YY1F FFFC	2^18 (256K)	Various
Input Memory	0x YY40 0000	0x YY5F FFFC	2^19 (512K)	0x FFFF FFFF
Output Memory	0x YY60 0000	0x YY7F FFFC	2^19 (512K)	0x FFFF FFFF

Mother CSRs

ID: Name	*Address*	*Functionality (default)*	*Access*
0:Mother firmware rev	0x YY00 0000	0xABCDmmmm	R
1:Status	0x YY00 0004	D0: RCC_halt D1: RCC_latch D2: RCC_run_stop (these default to '1' when unconnected)	R
2:Halt status/control	0x YY00 0008	TBD	
3:RCC/Local clock mode	0x YY00 000C	D0: 0=RCC, 1=Local	RW
4:Local mode run/stop	0x YY00 0010	D0: 0=Stop, 1=Run	RW
5:Operation Control	0x YY00 0014	D0: 0=Load, 1=Armed	RW
6:Prom prog 1	0x YY00 0018	D(31,0):status	R
7:Prom prog 2	0x YY00 001C	D(7,0):TDI bitstream length	W
8:Prom prog 3	0x YY00 0020	D(31,0):prog bitstream in	W
9:Prom prog 4	0x YY00 0024	D(31,0):prog readback	R
	0x YY00 0028		

Daughter CSRs

ID: Name	*Address*	*Functionality (default)*	*Access*
0: Daughter firmware rev	0x YY00 0100	0xDCBAmmmm	R
1: Status	0x YY00 0104	TBD	R
2: DSM Cables Connected	0x YY00 0108	D(7,0)	R
3: Read/writable test reg	0x YY00 010C		RW
4: FIFO Status	0x YY00 0110	D0: Token FIFO Empty D1: Token FIFO Full D2: Response FIFO Empty D3: Response FIFO Full D4: Info FIFO 1 Empty D5: Info FIFO 1 Full D6: Info FIFO 2 Empty	R

		D7: Info FIFO 2 Full D8: Info FIFO 3 Empty D9: Info FIFO 3 Full D10: Info FIFO 4 Empty D11: Info FIFO 4 Full D12: Info FIFO 5 Empty D13: Info FIFO 5 Full D14: Info FIFO 6 Empty D15: Info FIFO 6 Full D16: Info FIFO 7 Empty D17: Info FIFO 7 Full D18: Info FIFO 8 Empty D19: Info FIFO 8 Full D20: Info FIFO 9 Empty D21: Info FIFO 9 Full D22: Info FIFO 10 Empty D23: Info FIFO 10 Full	
5: FIFO Reset	0x YY00 0114	D0: Clear Token FIFO D1: Clear Response FIFOs D2: Clear Info FIFOs	W
6: Token FIFO	0x YY00 0118	D(11,0): Token	W
7: Response FIFO 1	0x YY00 011c	D(23,0): Action Word	W
8: Response FIFO 2	0x YY00 0120	D(11,0): Token	W
9: Info FIFO 1	0x YY00 0124	D(15,0): AW Det Bitmask D(19,16): AW DAQ Command D(23,20): AW TRG Command	R
10: Info FIFO 2	0x YY00 0128	D(11,0): Token	R
11: Info FIFO 3	0x YY00 012c	D(31,0): DSM tree bits (31,0)	R
12: Info FIFO 4	0x YY00 0130	D(31,0): DSM tree bits (63,32)	R
13: Info FIFO 5	0x YY00 0134	D(31,0): DSM tree bits (95,64)	R
14: Info FIFO 6	0x YY00 0138	D(31,0): DSM tree bits (127,96)	R
15: Info FIFO 7	0x YY00 013c	D(31,0): Active triggers (31,0)	R
16: Info FIFO 8	0x YY00 0140	D(31,0): Active triggers (63,32)	R
17: Info FIFO 9	0x YY00 0144	D(15,0): External BUSY D(32,16): Internal BUSY	R
18: Info FIFO 10	0x YY00 0148	D(15,0): DSM address	R
19: Internal Busy	0x YY00 014c	D(15,0): Enable per detector	RW
20: Internal Busy Length	0x YY00 0150	D(31,0): in RS units	RW
21: Local Address Control	0x YY00 0154	D0: Reset to zero D1: Copy current value to CSR22	W
22: Read Local Address	0x YY00 0158	D(15,0): Address counter value	R
23: TCD clock source	0x YY00 015c	D0: 0=TCUI, 1=TCU	RW
24: Snoop DSM inputs	0x YY00 0160	D(31,0): DSM tree bits (31,0)	R
25: Snoop DSM inputs	0x YY00 0164	D(31,0): DSM tree bits (63,32)	R
26: Snoop DSM inputs	0x YY00 0168	D(31,0): DSM tree bits (95,64)	R
27: Snoop DSM inputs	0x YY00 016c	D(31,0): DSM tree bits (127,96)	R
28: Snoop Busy inputs	0x YY00 0170	D(15,0): External BUSY	R

29: Token FIFO count	0x YY00 0174	D(11,0) : count	R

Counter Registers

Counter FIFO status	0x YY00 0200	D0: FIFO empty D1: FIFO full	R
Counter FIFO control	0x YY00 0204	D0: Clear all counters	W
Counter FIFO 1 (hi)	0x YY00 0208	D(31,24): Counter ID D(7,0) : Counter bits (39,32)	R
Counter FIFO 2 (lo)	0x YY00 020c	D(31,0) : Counter bits (31,0)	R

Counter IDs

ID	*Counter*	*ID*	*Counter*	*ID*	*Counter*	*ID*	*Counter*
0x00	(unassigned through 0x0b)	0x20	Trg 0 Phys	0x40	Trg 0 Phys + Live	0x60	Trg 0 After Prescale
0x01		0x21	Trg 1 Phys	0x41	Trg 1 Phys + Live	0x61	Trg 1 After Prescale
0x02		0x22	(and so on)	0x42	(and so on)	0x62	(and so on)
0x03		0x23		0x43		0x63	
0x04		0x24		0x44		0x64	
0x05		0x25		0x45		0x65	
0x06		0x26		0x46		0x66	
0x07		0x27		0x47		0x67	
0x08		0x28		0x48		0x68	
0x09		0x29		0x49		0x69	
0x0a		0x2a		0x4a		0x6a	
0x0b		0x2b		0x4b		0x6b	
0x0c	Bunch	0x2c		0x4c		0x6c	
0x0d	Trgs issued	0x2d		0x4d		0x6d	
0x0e	Resps issued	0x2e		0x4e		0x6e	
0x0f	Trg FIFO empty	0x2f		0x4f		0x6f	
0x10	Det 0 busy	0x30		0x50		0x70	
0x11	Det 1 busy	0x31		0x51		0x71	
0x12	(and so on)	0x32		0x52		0x72	
0x13		0x33		0x53		0x73	
0x14		0x34		0x54		0x74	
0x15		0x35		0x55		0x75	
0x16		0x36		0x56		0x76	
0x17		0x37		0x57		0x77	
0x18		0x38		0x58		0x78	
0x19		0x39		0x59		0x79	
0x1a		0x3a		0x5a		0x7a	

0x1b		0x3b		0x5b		0x7b	
0x1c		0x3c		0x5c		0x7c	
0x1d		0x3d		0x5d		0x7d	
0x1e		0x3e		0x5e		0x7e	
0x1f		0x3f		0x5f		0x7f	

Trigger Registers
(for trigger xx)

ID: Name	*Address*	*Functionality*	*Access*
0: Condition 1, on	0x YY10 xx00	D(31,0): bits (31,0)	RW
1: Condition 1, on	0x YY10 xx04	D(31,0): bits (63,32)	RW
2: Condition 1, on	0x YY10 xx08	D(31,0): bits (95,64)	RW
3: Condition 1, on	0x YY10 xx0c	D(31,0): bits (127,96)	RW
4: Condition 1, off	0x YY10 xx10	D(31,0): bits (31,0)	RW
5: Condition 1, off	0x YY10 xx14	D(31,0): bits (63,32)	RW
6: Condition 1, off	0x YY10 xx18	D(31,0): bits (95,64)	RW
7: Condition 1, off	0x YY10 xx1c	D(31,0): bits (127,96)	RW
8: Condition 2, on	0x YY10 xx20	D(31,0): bits (31,0)	RW
...			
~~16: Condition 3, on~~	~~0x YY10 xx40~~	~~D(31,0): bits (31,0)~~	~~RW~~
...			
~~24: Condition 4, on~~	~~0x YY10 xx60~~	~~D(31,0): bits (31,0)~~	~~RW~~
...			
32: Detector on	0x YY10 xx80	D(15,0)	RW
33: Detector off	0x YY10 xx84	D(15,0)	RW
34: Prescale	0x YY10 xx88	D(31,0)	RW
35: Action Word	0x YY10 xx8c	D(15,0): AW Det Bitmask D(19,16): AW DAQ Command D(23,20): AW TRG Command	RW
36: Counter phys (hi)	0x YY10 xx90	D(7,0): bits (39,32)	R C*
37: Counter phys (lo)	0x YY10 xx94	D(31,0): bits (31,0)	R C*
38: Counter phys&det (hi)	0x YY10 xx98	D(7,0): bits (39,32)	R C*
39: Counter phys&det (lo)	0x YY10 xx9c	D(31,0): bits (31,0)	R C*

C*: These counters are cleared by writing anything to their memory locations. Either hi or lo will reset the entire counter.