last update 081222

Startup tasks for Run9: we have all new QT boards replacing CDBs,
And a new TCU incorporating old LD301 + TCU

000. Some software checks;
1.definition of all DSM registers in GUI
2.verify GUI info going to correct register for critical ones
threshold for BBCE,W in BB101
threshold for VPDE,W in VP101
threshold for ZDCE,W in ZD101
BBC delta T min and max in VT201
ZDC delta T min and max in VT201
3.DSM tree logic
4. V124 setup (from Angelika D)

00. DAQ checks
1. run trigger detectors with DAQ and check output files
2. run each detector with DAQ and trigger and check output files

0. Some signals to check:
0. check timing of TRGPD cables into DAQ room
1. GLINK connections to and from daq room and platform
2. alignment of blue and yellow fill signals – use blue PET to align
3. yellow, blue, and rev-tick on platform
4. check alignment of all QT gates for BBC, VPD, ZDC
5. check each bit coming into TCU
6. check that BBCW1 signal and gate and BBCE1 signal and gate
are being shipped to daq room from driver board
7. check gate widths and vary using QT config files
8. measure TAC sensitivity

1. PMT HV
start with "best guess" demand file for BBC, VPD, ZDC
HV files: /export/home/users/sysuser/epics/R3.12.2-LBL/TRGhvApp/src

2. ADC gate timing – use Yellow timing as driver
check BBC E and W coincidence
vary yellow bit timing (fine delay on PET page)
check gate and signal relative timing on oscilloscope
get edges of ADC range response – select PET settings
establish BBCE.W coincidence using fiber signals
use BBC coincidence to trigger scope and look at:
ZDCE gate with ZDCE1 signal
determine time from gate leading edge to signal
set QT delay to get signal at front of gate
measure earliest start and latest stop for BBCE1 TAC

wrt BBCE1 ADC gate
earliest start should come ~12ns following
leading edge of BBCE1 signal
OK to let gate trailing edge act as stop

3. DSM alignment
    check that ZDC, BBC and VPD all fall in same
        crossing in data stream
4. Blue/Yellow bits
    time these into the trigger
        start with all buckets “on” in PET page
        then remove to reveal “real” fill pattern
5. TAC range
    check range of TAC
    if gate stop is too late, need to set delay on TAC stop
        to reduce range (needs access)
6. Check calibration of BBC, VPD, ZDC
    check single neutron peak in ZDCs, mip peaks in BBC, VPD
    align all TAC edges so TAC minimum works for vertex
7. Find “earliest hit” for each TAC channel
    histogram TAC values , decide on “early” edge
    set LUT so this earliest hit maps to same max value
        for each channel
    set LUT for delta-T to map to 16 bins
    correlate BBC vertex with TPC vertex
    correlate VPD vertex with TPC vertex
    correlate ZDC vertex with TPC vertex
8. Diamond definition
    check diamond shape using TAC
9. Min bias definition
    check consistency of all layers of DSM input
    check consistency of TCU input bits with DSM tree layers
    investigate vertex definition using BBC, VPD, ZDC
        decide which detector works best for trigger
10. Scalers
    program RAT as desired
    check definition of each scaler channel
    check readout and file integrity based on pattern input
11. check timing on FMS, PP2PP, MTD
12. check EMC, TOF data in triggered crossing