Last revised: 12 March 2009

Requirements for Year 2009 TCU

H.J. Crawford, J.M. Engelage, E.G. Judd, J.M. Landgraf,
J. Nelson, M. Ng, C. Perkins, G.Visser

This document establishes the requirements for an upgraded STAR Trigger Control Unit (TCU). The primary reason for this upgrade is to allow more simultaneously running triggers at STAR. Secondary reasons include a requirement for more bits in the user-accessible selection process and an increased number of independent detectors. The new TCU must be compatible with existing DSMI input and TCUI output to allow using the new TCU prior to implementing a new TCD system.

Notable similarities to previous TCU versions:
1. The token handling logic remains identical
2. The VME interface remains as similar as possible to the existing version, given the modifications due to hardware & firmware changes.

Notable changes from previous version:
1. Change: **Preceded / Followed** - No longer require preceded / followed logic.
2. Change: **Limitations** – The following limitations will be increased
* 8 detector groups – new limit set by action word length: will be ≥ 16
* Prescale value range increased to >26 bits
3. Change: **Logic** – The state-machine concept is altered, and we now will issue a trigger whenever any specified combination of input bits has a prescale value of 1. This means that a crossing may have more than 1 valid trigger condition.

Definitions:
1. Trigger: a specified combination of physics bits and detector-LIVE bits and pre-scale conditions
2. Physics bits: bits that originate from fast detectors, primarily from the DSM tree
3. Detector-live bit: bit to assert when a detector is ready to be triggered, the so-called Live bit.
4. Action word: one word for each trigger: a bit-mask specification of each detector that must respond to this trigger, accompanied by a 4-bit trigger command, a 4-bit daq command, and a 12-bit token.
5. RS == RHIC strobe: this is the 9.4 MHz system clock at STAR.
6. TCD == Trigger-Clock Distribution system

Brief description: The TCU will take input bits, presumably but not necessarily from the DSM tree, and Live status bits from the detectors, and it will generate a level0 trigger for STAR. Any combination of input and Live bits can define a trigger. Any number of triggers (up to at least 50) may be simultaneously satisfied. The trigger command must be sent to the detectors specified in the action word for this trigger within 1.5 microseconds of the occurrence of the triggering interaction. For crossings when there is no trigger, the TCU will distribute other commands from its stack, such as abort or accept commands. We use 128 input bits and 128 output bits in our current model, (128 on P3, 64 on P2, 64 on front panel) with their meaning fully programmable. These may run at multiples of the RHIC clock, increasing the I/O count accordingly.

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TCU Requirements

1. Requirement: **Format** - The TCU must be a 9U VME board.

Justification: Easy integration with existing trigger system.

2. Requirement: **Data Input** - The TCU must be able to accept at least 128 physics input bits.

Justification: To remove existing constraints on what triggers may be implemented and to support detector and trigger upgrades for years to come.
Status: 090312: initial tests showed we could handle more than 50 triggers of 128 bits each, but we are unable to route them onto the FPGA. We have succeeded with 32 triggers of 128 bits for routing. We do not need more than 96 bits and have agreed we will ignore bits 0-15 and 112-127 in the current scheme.

3. Requirement: **Detector-Live Input** - The TCU must accept independent input bits representing each of the non-trigger detector system's LIVE/BUSY status.

Justification: No trigger may be issued to any detector while it is dead.
Status: we intend to implement at least 16 detector LIVE bits in a manner that allows expansion.

4. Requirement: **RCC input –** The TCU must accept standard input from the RHIC Clock and Control board (clock, RUN/STOP, HALT)

Justification: need to operate synchronously with the Level0 trigger electronics

5. Requirement: **Input Standard:** A single standard will be selected for routing physics and LIVE bits into and out of the TCU. This will be TTL for VME compatibility.

Justification: Want simple interface, consistent with current trigger standard. Note that a single ended standard allows us to use more pins as bits.
Status: We expect to employ 2 boards, a brain and a router. We bring data into the TCU brain from a DSMI, and put it out to the TCD through a TCUI on the Router board, with a copy available for a spy board.

6. Requirement: **Differential Clock input** – The TCU must accept the RCC Clock input on a differential pin-set

Justification: need clean clock on the board
Status: 090312: suggest adding a delay line to allow software phase adjust for input clock.

7. Requirement: **Local Oscillator** – The TCU must include a software-selectable local oscillator (>9.4 MHz) for operation without the RCC.

Justification: useful for test mode.

8. Requirement: **Speed** - The TCU must accept input data and produce a trigger decision based on its input every tick its clock: for RHIC this means 9.4 MHz.

Justification: Every RHIC clock represents a possible collision.
Status: data latching will be under FPGA control, so the board can operate over a range of frequencies.

9. Requirement: **Latency in TCU**: The TCU must distribute a trigger within 2.5 RS of receiving the 128 input bits.

Justification: The 1.5 microsecond limit allows 260ns latency in TCU since it takes the place of both the last DSM and the current TCU. This is also required to keep timing the same as the current system.

10. Requirement: **Supported Triggers** – The TCU must support at least 50 simultaneous running triggers.

Justification: To support star operations.

11. Requirement: **Internal BUSY** - The TCU must generate an internal BUSY state of either 0 or a register-selectable duration (in RS units, up to 7 ms.) for each detector to cover the time it takes between the issuing of the trigger and the raising of that detector's external busy signal.

Justification: No trigger may be issued to any detector while it is dead. We want the delay to be a fixed value to minimize confusion, since the TCD can be programmed for any delay length for each detector.
Status: 090312: we have 16 such counters working.

12. Requirement: **Trigger Independence** – The behavior of a trigger should be fully defined by the input bits (physics + Live bits) presented to the TCU. This criterion must remain true for each trigger individually, no matter how many, or which other triggers are specified.

Justification: This is necessary to ensure unbiased triggering.
Status: care must be taken for triggers that include 2-bit encoding.

13. Requirement: **Detector Action** – If an L0 trigger condition is met, each detector in the trigger's action word must be sent the command identified with that trigger. Since multiple trigger conditions may be met in a single crossing, a hierarchy of commands must be imposed to resolve conflict.

Justification: To support triggers with differing detector requirements
Status: 090312: Currently if we have simultaneous triggers with conflicting trg commands then we ignore the event. We need to fix this so we can interleave lasers.

14. Requirement: **Detector Selection** - The set of detectors reacting in any bunch crossing must be the logical "OR" of the action words detector bit mask of each satisfied trigger, or the action word associated with a queued command.

Justification: The detector requirements are part of the specification of a trigger.
Status: action word includes 16 bits for detector bit mask plus 4 bit trigger and daq commands plus 12 bit token

15. Requirement: **Token Based Resource Management** - The TCU will manage the resources of the entire trigger system by tagging events with one of 4095 tokens. Tokens are taken from the token FIFO whenever a command is issued to the detectors. The depth of the token FIFO is 4096.

Justification: Existing trigger protocols must be maintained.
Status: A token may not be reused until the event has been aborted or stored by DAQ. Loading the Token FIFO is controlled by L1.

16. Requirement: **Prescale** - The TCU must be capable of prescaling each defined trigger independently from a maximum of 10 MHz down to less than 0.1 Hz, (2^{27}=1.28x10^{8}).

Justification: The only way to control the detector dead time is to manage the Level0 trigger rate.
Status: 090312: have implemented 32-bit prescales

17. Requirement: **Halt** – A nearly-bullet-proof mechanism must be implemented for ensuring that the DSM data read out by the DSM CPUs is not stale.

Justification: Data is saved in the DSM circular input buffers for 7 ms after it is written. A scheme must be in place to ensure that the <0.01% of the data is stale.
Status: we use software scheduling to ensure this now, because we do not demand notification from each CPU when it has sent its data to L2. We are considering a 24-bit counter in the DSMs and TCU that counts the RHIC clock to go to the data stream to allow checking for consistency offline. EJ is now putting this code into the DSMs. This appears to require 4095 – 40 bit deep counters – not likely to happen.

18. Requirement: **Output to Detectors** - When the TCU issues a trigger or other command it must distribute information to the trigger system. This includes providing the trigger command (4-bit), daq command (4-bit), token (12-bit), and detector bit mask (>=16-bit), as well as a copy of the clock used by the TCU, to the TCD fanout. It also includes making the same information, as well as a list of triggers and detectors fired, and the current DSM buffer address available over VME so that other trigger components may be notified via the trigger network.

Justification: The existing trigger protocol must be obeyed.

19. Requirement: **Command Distribution** - A mechanism must be provided to distribute commands via the VME interface for events in the system.

Justification: We employ a 4bit trigger command (trg-cmd) and a 4 bit daq command (daq-cmd). Commands are output to the TCD and trigger detectors in association with a Level 0 trigger, or from the queue of secondary commands awaiting distribution for crossings which do not generate a Level 0 trigger, such as abort and accept commands. These are sent to the detectors whenever they appear on the response

FIFO, which has a depth of at least 4096 to match the token FIFO. The abort and accept decisions are made by other trigger components and routed via VME to the TCU for distribution.

20. Requirement: **Null Event** - If the current event is not triggered, and there are no other commands queued for distribution, the TCU must actively send zeros to the TCD fanout.

Justification: If the TCU does not actively send zeros, the detectors may fire erroneously.

21. Requirement: **Output to Scalers**: At least 17 bits (LIVE + Token-FIFO-MT) must be available for scaler input.

Justification: Want to record LIVE combinations, including when the trigger is alive as indicated by the Token FIFO being non-empty.
Status: expect these to be available on DSMI – 32 bits driven by TCU onto DSMI

22. Requirement: **Interface**: Communication between the TCU and the detectors and other outside components (RCC, RAT, etc) must be driven through an interface card. The pinout for this board must be compatible with the existing TCUI (interface card) and the existing DMSI.

Justification: to maintain flexibility and eliminate drivers from the TCU design. We need to maintain compatibility to allow staging of the new hardware.
Status: The TCU will place a single copy of the output on the VME backplane. An interface board will take these and drive them to a TCD distribution system.

23. Requirement: **VME Specification** – VME standards should be respected:

* Polling the event FIFO during VME downloads should not lock the crate
* The TCU should respond unconditionally to the SYSreset line by performing a power-on reset, which includes configuring all FPGAs.
* The board must not interfere with VME power or communication lines
* Avoid conflict with VME64 transactions

Justification: To eliminate the necessity to power-cycle the VME crate on errors and maintain VME standards compatibility.
Justification: need to respect VME standards and eliminate need for power cycling to reset.

24. Requirement: **Counters**:
    a. For each trigger: The number of bunch crossings for which the physics input bits satisfied the physics on/off bit requirements for that trigger while the detector live/dead requirements were NOT satisfied.
    b. For each trigger: The number of bunch crossings for which the physics input bits satisfied the physics on/off bit requirements for that trigger while the detector live/dead requirements were satisfied.
    c. The number of bunch crossings for which the TCU was not able to fire an event (whether because of the TCU fifo being empty or any other reason including bunch crossings spent writing out counter data)
    d. The number of bunch crossings.
    e. For each detector: the number of bunch crossings that detector was dead.

Justification: This unit must allow calculation of cross sections for different triggers.
Status: 090312: MN has implemented this as counter for physics+live and counter for physics, so the deadtime can be found by subtraction.

25. Requirement: **Counter Reads**- It must be possible to read these counters out during the run on time scales of approximately every 5-10 seconds (register selectable rate). The protocol for doing this should not incur significant dead time.

Justification: Want continuous monitor of performance to catch errors quickly.
Status: We are using a front-panel Ethernet connection for these with dedicated FPGA interface.

26. Requirement (If practical): **Overlaps** – For each pair of triggers, the number of bunch crossing for which the physics input bits satisfied the physics on/off bit requirements for BOTH triggers. (This constitutes ntriggers * (ntriggers-1)/2 ~ 1225 counters).

Justification: Counting the first order trigger overlaps would also be useful:

27. Requirement: **Start/Stop control from RCC**: The TCU must obey the RCC for starting and stopping operation.

Justification: Need to maintain synchronous operation with trigger electronics.

28. Requirement: **Configure in <<60 sec**: The TCU must fully configure at run start in less than 1 minute.

Justification: beamtime requires that the whole trigger configure in fewer than 60 sec.

29. Requirement: **Configure at Reset**: The TCU must re-configure on sysrest in <60 sec.

Justification: Want to configure all non-run-specific portions to speed run start-up configuration.

30. Requirement: **PROM programming** – JTAG on front for loading VME initializer prom.

Justificaiton: ease of operation.

31. Requirement: **Front Panel**: The front panel should have, at least,
    a. LEDs - Run/Load (green/blue), VME access (blue), token FIFO mt (red), Halt (red)
    b. Lemo's - trigger out, clock out, trigger in, auxiliary in, auxilary out (drive or terminate 50 Ω)
    c. Hex 40-bit (10 char) display for TCD out

Justification: ease of trouble-shooting

Status: need 5 LEDs for clarity.

32. Requirement: **TCU input in data stream**: The TCU must place its input and output bits into the data stream for any triggered event. It must also put the DSM address of the triggered data into the data stream. It must also place a bit mask in the data stream indicating which triggers had a prescale of 1 for this event.

Justification: we need to be able to reconstruct why an event was triggered.

Status: 090312: implemented as 32-bit mask in Info Fife 7 and 8.

33. Requirement: **Input and Output memories:** The TCU needs to have enough memory to save all of its input and output data (and maybe an intermediate stage) from 64k crossings. A register-selectable option to suppress NULL crossings must be implemented to allow the memory to store a longer time period. The output memory must also be configurable to operate as input to the TCD for tests.

Justification: need to be able to debug and test the board.

Status: 090312: not yet implemented