TO DO @ BNL for Run 10

1. TCU
    a. Determine/fix L0 crash problem (>800Hz)
    b. Check configuration PROM problem
    c. Implement Counters
    d. Test internal busy logic (jml – 090427)
    e. Test external busy logic
    f. Configure for run 10 and test with sample input data and external detector system
    g. Check TCU input buffer with layer 3 DSM output
2. Software
    a. DRORC drivers in new L2ana01
    b. Check STP operation in new L2ana01
    c. QT algos for run 10
        i. Add "killer bits" to QT algos for vertex detectors
    d. New TCU codes
    e. DSM algos for run 10
    f.
3. Simulation data
    a. Create simulated data and tier1 file for putting ramps into trigger system to test that all bits are working and flow correctly thru tree
    b. Create simulated data and tier1 file to test algorithms (i.e. mock up full production configuration)
4. Computer work
    a. Install AFS on trgscratch
    b. Upgrade disk on trgscratch
    c. Build new l2ana01 machine
    d. Build new startrg machine
        i. Connect startrg2/startrg to UPS
        ii. Replace startrg2 monitor/video-card?
    e. Order network equipment to restock spares inventory
5. TOF
    a. DRORC connection to l2ana01
    b. Fix TF001 & TF006
    c. Test bits from all new trays into DSMs
6. Fabricate 3rd stp concentrator (for spare)
7. FHC
    a. Test FHC cables from west wall to L1
    b. CR tests with miniTrg system
    c. Replace two 8port Ethernet switches with 16/32 port switch in SW racks
8. Setup miniTRG
    a. Obtain roll around rack
    b. Outfit rack with 2 VME crates (1 QT-type, 1 DSM type)
    c. Electronics
        i. 4 QTs, 1 DSM/DSMI, 1TCU/TCUI, RCC/RCF
        ii. 2306 cpus(2), 8 port switch, surge suppressor, etc.

9 VPD
    a. Install splitters and test with AWG
    b. Include killer bits in QT algorithms
10 Normal run startup tasks
    a. test TCD/QT/QT-TAC-adapter for all systems (VPD, ZDC, MTD, PP2PP)
    b. standalone tests (e.g. QT, DSM, TAC, etc.)
    c. check QT and DSM connections by inputting ramps
    d. board repair
11 Documentation
    a. RAT cabling
    b. update crate layout, cable connections, test procedures on web
    c. eta-phi plot of all trigger detectors
    d. update timing plots for various detector DSM layers
    e. update general trigger section of web
    f. Check cable documentation on QT->DSM connections
        i. Check QT 0x18 and 0x19 wiring and order to FMS crate
12 Miscellaneous
    a. Reinstall ordo on l2ana02 to daqman mailer
    b. Setup DSM tests in ken's lab to test complex algo's on 1st run DSM boards
    c. Design/fabricate strain relief for positronix cable connections to QTs
    d. Re-establish PMD preTrigger
    e. connect myrinet monitors
    f. cleanup starp network change to new switch on platform
        i. track cable origins
        ii. remove unused cables

List for others: