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Requirements for Year 2009 TCU

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This document establishes the requirements for an upgraded STAR Trigger Control Unit (TCU). The primary reason for this upgrade is to allow more simultaneously running triggers at STAR. Secondary reasons include a requirement for more bits in the user-accessible selection process and an increased number of independent detectors. The new TCU must be compatible with existing DSMI input and TCUI output to allow using the new TCU prior to implementing a new TCD system.

Notable similarities to previous TCU versions:

1. The token handling logic remains identical
2. The VME interface remains as similar as possible to the existing version, given the modifications due to hardware and firmware changes.

Notable changes from previous version:

1. Change: Preceded / Followed – No longer require preceded / followed logic
2. Change: Limitations – The following limitations will be increased
    - 8 detector groups – new limit set by action word length: will be >= 16
    - Prescale value range increased to > 26 bits
3. Change: Logic – The state-machine concept is altered, and we now issue a trigger whenever any specified combination of input bits has a prescale value of 1. This means that a crossing may have more than 1 valid trigger condition.

Definitions:

1. Trigger: a specified combination of physics bits and detector-LIVE bits and pre-scale conditions
2. Physics bits: bits that originate from fast detectors, primarily from the DSM tree
3. Detector-live bit: bit to assert when a detector is ready to be triggered, the so-called Live bit.
4. Action word: one word for each trigger: a bit-mask specification of each detector that must respond to this trigger, accompanied by a 4-bit trigger command, a 4-bit daq command, and a 12-bit token.
5. RS == RHIC strobe: this is the 9.4 MHz system clock at STAR.
6. TCD == Trigger-Clock Distribution system

Brief description: The TCU will take input bits, presumably but not necessarily from the DSM tree, and Live status bits from the detectors, and it will generate a level0 trigger for STAR. Any combination of input and Live bits can define a trigger. Any number of triggers (up to at least 50) may be simultaneously satisfied. The trigger command must be sent to the detectors specified in the action word for this trigger within 1.5 microseconds of the occurrence of the triggering interaction. For crossings where there is no trigger, the TCU will distribute other commands from its stack, such as abort or accept commands. We use 128 input bits and 128 output bits in our current model, (128 on P3, 64 on P2, 64 on front panel) with their meaning fully programmable. These may run at multiples of the RHIC clock, increasing the I/O count accordingly.

Change Log:

Date	Description
14 March 2008	Original version
10 April 2008	Added “RCC input” requirement Changed “Status” of “Input Standard” requirement to remove backplane-overlay description and add in description of 2 board system: one for routing and one for calculations. Added “Differential Clock input” and “Local Oscillator” requirements. Added “Status” to the “Detector Selection” requirement Added “Status” to the “Token Based Resource Management” requirement. Added description of a possible 18-bit crossing counter in the DSMs to the “Status” of the “Halt” requirement. Added detector bit mask and copy of the TCU clock to the list of data sent to the TCDs in the “Output to Detectors” requirement. Changed the “Justification” for the “Command Distribution” requirement to make it clear that new trigger commands are sent to the TCD immediately, and are not placed in a FIFO. Changed the “Output to Scalers” requirement from 64 bits down to 17 bits and changed the “Justification” to indicate we only want to record LIVE combinations. Added compatibility with the existing DSMI to the “Interface” requirement. Added support of 64-bit Chain-Block-Transfer to the “VME Specification” requirement. Expanded the “Counters” requirement to list 5 different types of counter. Added the “VME Reads” and “Overlaps” requirements Added the “PROM programming” requirement Added the “VME access” LED, more LEMO connections and the Hex display to the “Front Panel” requirements
17 April 2008	Changed the size of the DSM crossing counter in the “Status” part of the “Halt” requirement from 18 bits to 24 bits. Also added this counter into the TCU. Removed support of 64-bit Chain-Block-Transfer from the “VME Specification” requirement. Renamed the “VME Reads” requirement to “Counter Reads” and removed the requirement that they be read out over VME. The justification proposes both VME and front-panel Ethernet read-out paths.
22 April 2008	Removed the description of the Command FIFO from the Justification of the “Command Distribution” requirement, because there is no such thing. Added a description of the Response FIFO.
19 May 2008	Added checking the address modifier lines to the “VME Specification” requirement.
23 July 2008	Added Table of Contents listing all requirements Changed the “Input Standard” requirement to specify TTL instead of LVTTL. Also change the wording of the Justification. Changed the “Local Oscillator” requirement to specify that it must be software-selectable, and the frequency must be > 9.4 MHz. Added “Status” to the “Speed” requirement. Changed the “Internal Busy” requirement to specify that the length be register-selectable, not fixed. Changed “Halt” Status to indicate EJ is putting crossing counter into the DSM code. Changed “Output to Detectors” requirement to specify that the detector bitmask is at least 16 bits, instead of exactly 16 bits. Removed reference to the address modifier lines from the “VME Specification” requirement, and just state that the TCU must not interfere with VME64 transactions Removed the number of “detector dead” counters from the description (item e.) in

	the “Counters” requirement. Added “Status” to the “Counter Reads” requirement, and put the Ethernet connection description there. Added “Status” to “Front Panel” requirement
12 March 2009	Added “Status” to the “Data Input” requirement saying we would ignore DSM input bits 0:15 and 112:127 Added “Status” to the “Differential Clock Input” requirement, suggesting that we add a programmable delay line for phase adjustment. Added “Status” to “Internal BUSY” requirement Added “Status” to “Detector Action” requirement Added “Status” to “Prescale” requirement Updated “Halt” status to say that counters were too big and unlikely to happen Added “Status to “Counters” requirement Added “Status to “TCU input in data stream” requirement Added “Status” to “Input and Output memories” requirement, to say it is not done yet.
7 August 2009	Added in this Change Log
25 August 2009	Updated the Prescale requirement to specify that the prescale counters must be disabled when either the token FIFO is empty or the TCU is halted. Changed the Counters requirement to say that the TCU needs to count everything that is necessary for cross-section and dead-time calculations. The actual list of counters that we will implement is moved into the Status section. Changed the Counter Readout requirement to specify that whenever the counters are read out, the values must all be valid at the same moment in time. Changed the “Status” of the “Detector Live Input” requirement to explain how we could increase the number of bits from 16 to 32 if necessary. Changed the “Status” of the “Detector Selection” requirement to state that if the number of bits in the detector bit mask is increased then the size of the action word will increase, and all appropriate FPGA code and VME software will need to change too. Changed the “Status” of the “Output to Detectors” requirement to explain which hardware would need to be changed in order to increase the detector bitmask beyond 16 bits. Added “Status” to “VME Specification” to say that there is no need for the TCU to raise an interrupt, so there is no connection to any of the IRQ lines.
1 September 2009	Corrected a few typos. Moved the “Status” of the “Input Standard” requirement to the “Format” requirement, since it seemed to fit better there. Updated the “Interface” requirement to make it clear that the TCU needs to be compatible with both the existing TCUI and DSMI. Updated the “Front Panel” requirement to specify that the Lemo outputs must be TTL (i.e. not ECL, NIM, etc…)

TCU Requirements

1. **Format**
   Requirement: The TCU must be a 9U VME Board
   Justification: Easy integration with the existing trigger system.
   Status: We expect to employ 2 9U VME boards: a brain and a router. We bring data into the TCU brain from a DSMI and put it out to the TCD through a TCUI on the Router board, with a copy available for a spy board.

2. **Data Input**
   Requirement: The TCU must be able to accept at least 128 input bits
   Justification: To remove existing constraints on what triggers may be implemented and to support detector and trigger upgrades for years to come.
   Status: 090312: initial tests showed we could handle more than 50 triggers of 128 bits each, but we are unable to route them onto the FPGA. We have succeeded with 32 triggers of 128 bits for routing.

3. **Detector-Live Input**
   Requirement: The TCU must accept independent input bits representing each of the non-trigger detector system's LIVE/BUSY status.
   Justification: No trigger may be issued to any detector while it is dead.
   Status: Currently the TCU receives 16 LIVE/BUSY bits on one connector on the TCUI. 16 bits is enough for the current set of detectors, however we may need to increase that number at some point in the future. Currently, those bits are routed through the TCUR and the TCU motherboard, onto the TCU daughter card and into the triggering FPGA. A second connector exists on the TCUI that was originally used to bring DSM data in to the old TCU. Its bits are routed to the same FPGA as the BUSY/LIVE bits, using the exact same circuit. Since this second connector is not currently being used, if necessary it could be used to bring in up to 16 more BUSY/LIVE bits, bringing the total up to 32.

4. **RCC Input**
   Requirement: The TCU must accept standard input from the RHIC Clock and Control board (clock, RUN/STOP, HALT)
   Justification: Need to operate synchronously with the Level0 trigger electronics.

5. **Input Standard**
   Requirement: A single standard will be selected for routing physics and LIVE bits into and out of the TCU. This will be TTL for backwards compatibility with the existing interface cards.
   Justification: Want simple interface, consistent with current trigger standard. Note that a single ended standard allows us to use more pins as bits.

6. **Differential Clock Input**
   Requirement: The TCU must acceot the RCC Clock input on a differential pin set.
   Justification: Need a clean clock on the board
   Status: 090312: suggest adding a delay line to allow software phase adjust for input clock.

7. **Local Oscillator**
   Requirement: The TCU must include a software-selectable local oscillator (> 9.4 MHz) for operation without the RCC.
   Justification: Useful for test mode.

8. **Speed**
   Requirement: The TCU must accept input data and produce a trigger decision based on its input every tick of its clock: for RHIC this means 9.4 MHz.
   Justification: Every RHIC clock represents a possible collision.

Status: Data latching will be under FPGA control, so the board can operate over a range of frequencies.

9. **Latency in TCU**
   Requirement: The TCU must distribute a trigger within 2.5 RS of receiving the 128 input bits.
   Justification: The 1.5 microsecond limit allows 260ns latency in TCU since it takes the place of both the last DSM and the current TCU. This is also required to keep timing the same as the current system.

10. **Supported Triggers**
    Requirement: The TCU must support at least 50 simultaneous running triggers.
    Justification: To support STAR operations.

11. **Internal BUSY**
    Requirement: The TCU must generate an internal BUSY state of either 0 or a register-selectable duration (in RS units, up to 7ms) for each detector to cover the time it takes between the issuing of the trigger and the raising of that detector's external busy signal.
    Justification: No trigger may be issued to any detector while it is dead. We want the delay to be a fixed value to minimize confusion, since the TCD can be programmed for any delay length for each detector.
    Status: 090312: we have 16 such counters working.

12. **Trigger Independence**
    Requirement: The behavior of a trigger should be fully defined by the input bits (physics + Live bits) presented to the TCU. This criterion must remain true for each trigger individually, no matter how many, or which other triggers are specified.
    Justification: This is necessary to ensure unbiased triggering.
    Status: care must be taken for triggers that include 2-bit encoding.

13. **Detector Action**
    Requirement: If an L0 trigger condition is met, each detector in the trigger's action word must be sent the command identified with that trigger. Since multiple trigger conditions may be met in a single crossing, a hierarchy of commands must be imposed to resolve conflict.
    Justification: To support triggers with differing detector requirements
    Status: 090312: Currently if we have simultaneous triggers with conflicting trg commands then we ignore the event. We need to fix this so we can interleave lasers.

14. **Detector Selection**
    Requirement: The set of detectors reacting in any bunch crossing must be the logical "OR" of the action word's detector bit mask of each satisfied trigger, or the action word associated with a queued command.
    Justification: The detector requirements are part of the specification of a trigger.
    Status: The detector bit mask is currently limited to 16 bits. If the number of detectors is increased beyond 16, then the size of the action word will increase, and all FPGA code and VME software that configures and/or uses the action word will need to change accordingly.

15. **Token Based Resource Management**
    Requirement: The TCU will manage the resources of the entire trigger system by tagging events with one of 4095 tokens. Tokens are taken from the token FIFO whenever a command is issued to the detectors. The depth of the token FIFO is 4096.
    Justification: Existing trigger protocols must be maintained.
    Status: A token may not be reused until the event has been aborted or stored by DAQ. Loading the Token FIFO is controlled by L1.

16. **Prescale**
    Requirement: The TCU must be capable of prescaling each defined trigger independently from a maximum of 10 MHz down to less than 0.1 Hz, (227=1.28x108). The prescale logic must be disabled whenever the TCU is unable to issue a trigger, either because there are no tokens in the FIFO or because the TCU has been halted.
    Justification: The only way to control the detector dead time is to manage the Level0 trigger rate.
    Status: 090312: have implemented 32-bit prescales

17. **Halt**
    Requirement: A nearly-bullet-proof mechanism must be implemented for ensuring that the DSM data read out by the DSM CPUs is not stale.
    Justification: Data is saved in the DSM circular input buffers for 7 ms after it is written. A scheme must be in place to ensure that the <0.01% of the data is stale.
    Status: we use software scheduling to ensure this now, because we do not demand notification from each CPU when it has sent its data to L2. We are considering a 24-bit counter in the DSMs and TCU that counts the RHIC clock to go to the data stream to allow checking for consistency offline. EJ is now putting this code into the DSMs. This appears to require 4095 – 40 bit deep counters – not likely to happen.

18. **Output to Detectors**
    Requirement: When the TCU issues a trigger or other command it must distribute information to the trigger system. This includes providing the trigger command (4-bit), daq command (4-bit), token (12-bit), and detector bit mask (>=16-bit), as well as a copy of the clock used by the TCU, to the TCD fanout. It also includes making the same information, as well as a list of triggers and detectors fired, and the current DSM buffer address available over VME so that other trigger components may be notified via the trigger network.
    Justification: The existing trigger protocol must be obeyed.
    Status: In its current state, the TCU can produce a detector bit mask up to 16 bits. It cannot meet the requirement that the detector bit mask be greater than 16. The output FPGA (second FPGA on the daughter card) produces just enough output bits to carry all the existing output data. These bits are routed through the TCU motherboard and then on to either the DSMI or the TCUR/TCUI. There are no spare output connectors that could be used to carry extra detector bit mask bits. In order to meet this requirement, at a minimum some of the existing output bits would need to be re-assigned, and the TCUI would need to be re-designed. If none of the existing output bits can be re-assigned, then the FPGA would need to produce more output bits, in which case all of the TCU daughter card, TCU motherboard, TCUR and TCUI would need to be re-designed.

19. **Command Distribution**
    Requirement: A mechanism must be provided to distribute commands via the VME interface for events in the system.
    Justification: We employ a 4bit trigger command (trg-cmd) and a 4 bit daq command (daq-cmd). Commands are output to the TCD and trigger detectors in association with a Level 0 trigger, or from the queue of secondary commands awaiting distribution for crossings which do not generate a Level 0 trigger, such as abort and accept commands. These are sent to the detectors whenever they appear on the response FIFO, which has a depth of at least 4096 to match the token FIFO. The abort and accept decisions are made by other trigger components and routed via VME to the TCU for distribution.

20. **Null Event**
    Requirement: If the current event is not triggered, and there are no other commands queued for distribution, the TCU must actively send zeros to the TCD fanout.
    Justification: If the TCU does not actively send zeros, the detectors may fire erroneously.

21. **Output to Scalers**
    Requirement: At least 17 bits (LIVE + Token-FIFO-MT) must be available for scaler input.

Justification: Want to record LIVE combinations, including when the trigger is alive as indicated by the Token FIFO being non-empty.
Status: expect these to be available on DSMI – 32 bits driven by TCU onto DSMI

22. Interface

Requirement: Communication between the TCU and the detectors and other outside components (RCC, RAT, etc) must be driven through interface cards. The pin assignments must be compatible with the existing interface cards, .i.e. the TCUI and DSMI.
Justification: to maintain flexibility and eliminate drivers from the TCU design. We need to maintain backwards compatibility to allow staging of the new hardware.
Status: The TCU will place a single copy of the output on the VME backplane. An interface board will take these and drive them to a TCD distribution system.

23. VME Specification

Requirement: VME standards should be respected:
* Polling the event FIFO during VME downloads should not lock the crate
* The TCU should respond unconditionally to the SYSreset line by performing a power-on reset, which includes configuring all FPGAs.
* The board must not interfere with VME power or communication lines
* Avoid conflict with VME64 transactions
Justification: To eliminate the necessity to power-cycle the VME crate on errors and maintain VME standards compatibility.
Status: Currently there is no need for the TCU to raise a VME interrupt, so there is no connection to any of the IRQ lines.

24. Counters

Requirement: The TCU must count every combination of bits necessary to allow the user to monitor the health of the TCU, rates for each trigger, and subsequently calculate cross-sections and dead times.
Justification: This unit must be monitored, and it must allow calculation of cross sections for different triggers.
Status: There are several different ways to implement these counters. We have chosen to implement

a. For each trigger: The number of bunch crossings for which the physics input bits satisfied the physics on/off bit requirements for that trigger.
b. For each trigger: The number of bunch crossings for which the physics input bits satisfied the physics on/off bit requirements for that trigger and the detector live/dead requirements were also satisfied.
c. For each trigger: The number of bunch crossings for which the physics input bits satisfied the physics on/off bit requirements, the detector live/dead requirements were also satisfied and the prescale had counted down to 1, so a trigger could be issued.
d. For each detector: the number of bunch crossings that detector was dead.
e. The number of bunch crossings for which the TCU was not able to fire an event (whether because of the TCU fifo being empty or any other reason, e.g. the TCU was halted)
f. The number of bunch crossings.
g. The number of bunch crossings where the TCU issued a trigger
h. The number of bunch crossings where the TCU issued a response (i.e. accept/abort).

25. Counter Readout

Requirement: It must be possible to read these counters out during the run on time scales of approximately every 5-10 seconds. The protocol for doing this must not interfere with the normal process of incrementing the counters. Also, when the counters are read, the values must all be valid at a single instance in time.
Justification: Want continuous monitor of performance to catch errors quickly. In order to compare rates, the counter values must all cover the same period of time.

Status: We have worked out a simple handshake between the VME client and the TCU that will allow the VME client to initiate saving all the counter values, simultaneously, into static registers, which can then be read out over VME. The hardware connections for an Ethernet link are in place, and this readout path may be implemented in the future.

26. Overlaps

Requirement (If practical): For each pair of triggers, the number of bunch crossing for which the physics input bits satisfied the physics on/off bit requirements for BOTH triggers. (This constitutes ntriggers * (ntriggers-1)/2 ~ 1225 counters).
Justification: Counting the first order trigger overlaps would also be useful:

27. Start/Stop control from RCC

Requirement: The TCU must obey the RCC for starting and stopping operation.
Justification: Need to maintain synchronous operation with trigger electronics.

28. Configure in <<60 sec

Requirement: The TCU must fully configure at run start in less than 1 minute.
Justification: beamtime requires that the whole trigger configure in fewer than 60 sec.

29. Configure at Reset

Requirement: The TCU must re-configure on sysrest in <60 sec.
Justification: Want to configure all non-run-specific portions to speed run start-up configuration.

30. PROM programming

Requirement: JTAG on front for loading VME initializer prom.
Justification: ease of operation.

31. Front Panel

Requirement: The front panel should have, at least,

a. LEDs - Run/Load (green/blue), VME access (blue), token FIFO mt (red), Halt (red)
b. Lemo's - trigger out, clock out, trigger in, auxiliary in, auxilary out (drive or terminate TTL 50 Ω)
c. Hex 40-bit (10 char) display for TCD out

Justification: ease of trouble-shooting
Status: need 5 LEDs for clarity.

32. TCU input in data stream

Requirement: The TCU must place its input and output bits into the data stream for any triggered event. It must also put the DSM address of the triggered data into the data stream. It must also place a bit mask in the data stream indicating which triggers had a prescale of 1 for this event.
Justification: we need to be able to reconstruct why an event was triggered.
Status: 090312: implemented as 32-bit mask in Info Fifo 7 and 8.

33. Input and Output memories

The TCU needs to have enough memory to save all of its input and output data (and maybe an intermediate stage) from 64k crossings. A register-selectable option to suppress NULL crossings must be implemented to allow the memory to store a longer time period. The output memory must also be configurable to operate as input to the TCD for tests.
Justification: need to be able to debug and test the board.
Status: 090312: not yet implemented