- 1 TCU
 - a. Troubleshoot Counters
 - b. Repair/test extra TCU-D cards
 - c. Load 3rd TCU motherboard

d.

- 2 Software
 - a. Service requests for any new QT algos for run 11
 - i. Add "killer bits" to QT algos for vertex detectors
 - b. Service requests for any new DSM algos for run 11

c.

- 3 Simulation data
 - a. Create simulated data and tier1 file to test algorithms (i.e. mock up full production configuration)

b.

- 4 Computer work
 - a. Upgrade disk on trgscratch
 - b. Finish building new startrg machine
 - i. Connect startrg2/startrg to UPS
 - c. Convert network to Christie/Betts
 - d. Start decommissioning process of startrg2
- 5 Board Construction
 - a. Design, fabricate, & test new 30bit scaler boards
 - b. Design, fabricate, & test new RCC/RCF-BOC
 i. Install/rewire existing RCC system
 - c. Fabricate 3rd stp concentrator (for spare)
- 6 TOF
 - a. Complete DRORC connection to l2ana01
 - b. Test bits from all repaired trays into DSMs
 - c.
- 7 MTD
 - a. Add 2^{nd} QT board to system
 - i. Move GEM cables from 1^{st} QT to 2^{nd}
 - ii. Cable in new MRPC units
 - b. Add 2nd TAC board to system for GEM
- 8 FMS ?
- 9 Normal run startup tasks
 - a. test TCD/QT/QT-TAC-adapter for all systems (VPD, ZDC, MTD, PP2PP)
 - b. standalone tests (e.g. QT, DSM, TAC, etc.)
 - c. check QT and DSM connections by inputting ramps
 - d. test glink and opticon fiber connections
 - e. board repair
- 10 Documentation
 - a. RAT cabling
 - b. update crate layout, cable connections, test procedures on web
 - c. post eta-phi plot of all trigger detectors on web

- d. update timing plots for various detector DSM layers
- e. update general trigger section of web
- f. Check cable documentation on QT->DSM connections
 - i. Check QT 0x18 and 0x19 wiring and order to FMS crate
- 11 Miscellaneous
 - a. Setup DSM tests in ken's lab to test complex algo's on 1st run DSMboards – done 08-June-2010
 - b. Design/fabricate strain relief for positronix cable connections to QTs
 - c.