Implementation of STAR MTD QT Algorithm - Run 2011
qt32b_l0_v6_7.mcs

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Description:

This algorithm outputs the maximum TAC sum from three MTD modules and a bitmask of which module had the highest sum. Each module has an East and West end. The three modules are connected to the first two channels (2xADC and 2xTAC) on QT8B, QT8C, QT8D. QT8A is not used in this algorithm.

The standard mask can be used for each channel to mask that channel from the trigger but retain the data in the datastream. Note that separate masks must be used for ADC and TAC channels.

This algorithm assumes the standard configuration where channels 1-4 are signal inputs and channels 5-8 are TAC inputs corresponding to channels 1-4. It uses the standard "Good Hit" definition, which requires that a given channel is greater than some ADC Threshold and the corresponding TAC channel is greater than some TAC_MIN and less than some TAC_MAX. For a module to be considered for the Max TAC Sum, both East AND West must satisfy the "Good Hit" requirement for that module. If either the East or West end of a module doesn't satisfy the "Good Hit" requirement, the TAC sum for that module will be '0'.

The bitmask will be ("001", "010", "100") if the Max TAC Sum is from (QT8B, QT8C, QT8D). If no module satisfies the "Good Hit" requirement, the Max TAC Sum will be '0' and the bitmask will be "000".

Only the first two channels on QT8B, QT8C, and QT8D are used in this algorithm so no channel masks are needed in the production configuration.

Inputs:

QT8A : None
QT8B :
- Ch 1/2 : MTD Module 1 East/West ADC
- Ch 5/6 : MTD Module 1 East/West TAC

QT8C :
- Ch 1/2 : MTD Module 2 East/West ADC
- Ch 5/6 : MTD Module 2 East/West TAC

QT8D :
- Ch 1/2 : MTD Module 3 East/West ADC
- Ch 5/6 : MTD Module 3 East/West TAC

Registers (1 Set Per Daughter Card)**:**

1 : "Good Hit" ADC Threshold
2 : "Good Hit" TAC_MIN
3 : "Good Hit" TAC_MAX

LUT:
TAC timing adjustment/ADC Pedestal subtraction for each channel

Algorithm Latch: 1

L0 Output to DSM:
(0-12) : Maximum TAC Sum (E + W)
(13-15) : Maximum TAC Sum bitmask
(16-31) : '0'