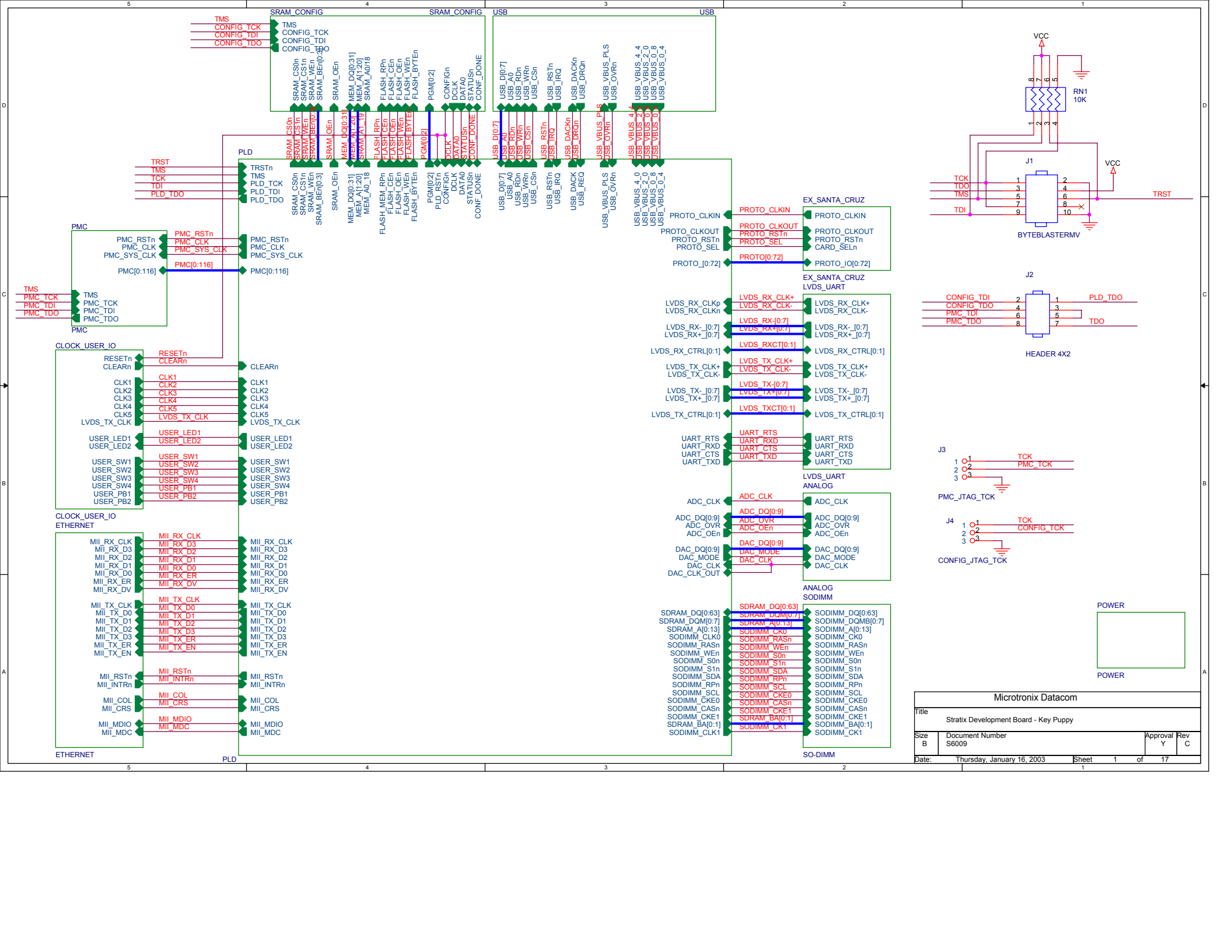
SRAM_CONFIG
USB
PLD
PMC
CLOCK_USER_IO
ETHERNET
EX_SANTA_CRUZ
LVDS_UART
ANALOG
SODIMM
SO-DIMM
BYTEBLASTERMV
HEADER 4X2
PMC_JTAG_TCK
CONFIG_JTAG_TCK
POWER
Microtronix Datacom
Stratix Development Board - Key Puppy
Document Number S6009
Thursday, January 16, 2003

Revision	Date	Author	Revision
A-1	8/22/02	Tim Grant	Initial Creation of Schematic
A-2	8/26/02	Tim Grant	Add notes for all off-page connectors. PMC checked again spec. Change the diodes on page 3 to BAV99. Changed resistors on Analog OpAmp to 1%. Add NAND gates for incoming ADC and DAC clocks. Correct swapped pins on UART. Changed power supplies for current draw.
A-3	9/06/02	Tim Grant	Jtag TCK pull-up changed to pull-down. Add a pull down for the MII_RSTn. Corrected LVDS connector part numbers. Added the following pins to U19 A21, G20, AH6, N28. Remove the pins AA20 and AA11 from multiple locations. Remove the series resistors on the feed back pins. Re-label J40 to PCI_M66EN.
B-1	11/01/02	Tim Grant	Signals VCCA_PLLx and VCCG_PLLx were connected to 1.5 instead of VCC. U6 changed from P149FCT3805AS to P149FCT3805AQ Change C50 and C51 from 10U to 100U. Add 27 pF capacitors to R123 and R4. Change R83 from 4K7 to 5K6 Correct schematic for U28 power and ground are reversed. Change label for USB_IRQn to USB_IRQ. Add 100N capacitors to analog output signals. Remove D1. Add TP11 to the analog section connected to Ground. Part number U7 changed from 50 MHz to 40 MHz. Change pull-up on J39 from +5 to VCC. Updated E7, E9, E11, E18, E20, E22, AE3, W9, AD11, AD9, AD7, AD22, AD20, AD18, W20, R19, P10, K9, E24, K20, to U19 symbol. PLL_FBp and PLL_FBn were switched at connections to the PLD. Capacitors footprint switched from 0603_IPC1/Via to 0602_IPC: C8, C15, C18, C19, C26, C28, C30, C133, C128, C16, C27, C29, C31, C44, C49, C129, C17. Changed D13 from value of 1N4001 to DL4001.
	11/20/02	Tim Grant	Changes C151 to 33P. Changed C154 to 1N. Changed R118 and R117 to 33R.
C	16/01/03	James Martin	- Rename SRAM Address lines to conform to proper 16/32 bit addressing modes - Change layout to plate DB-9 thru holes - pulldowns added to pgm[2:0]signals (RN98) - added pullups on SRAM control signals (RN99) - renamed resistornetworks with RN designation instead of just R - Added Jumper J99 to CSn signal to EPC device so that the EPC flash interface can be tri-stated during programming.

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Title: Stratix Development Board - Notes

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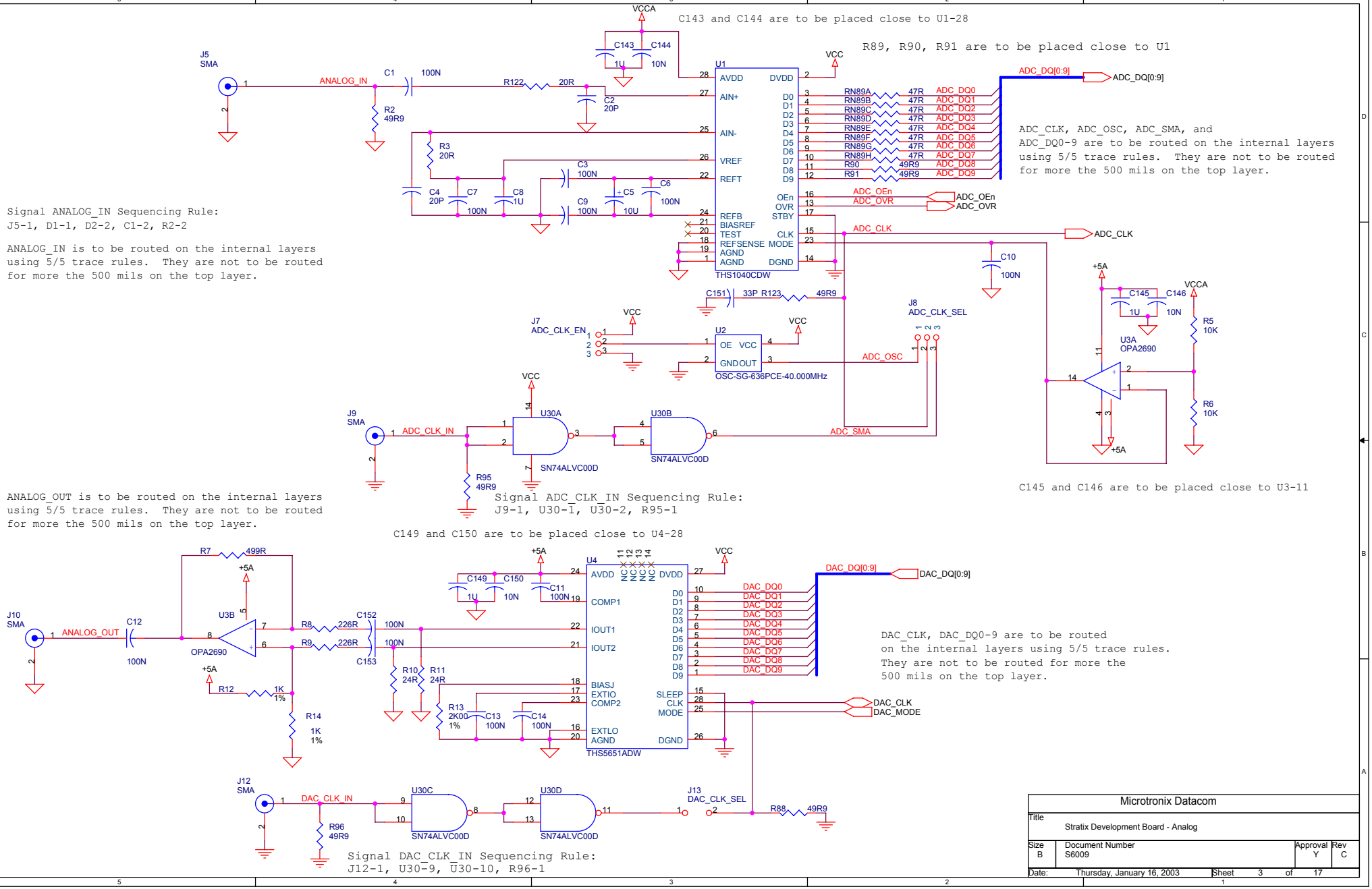

Microtronix Datacom			
Title: Stratix Development Board - Analog			
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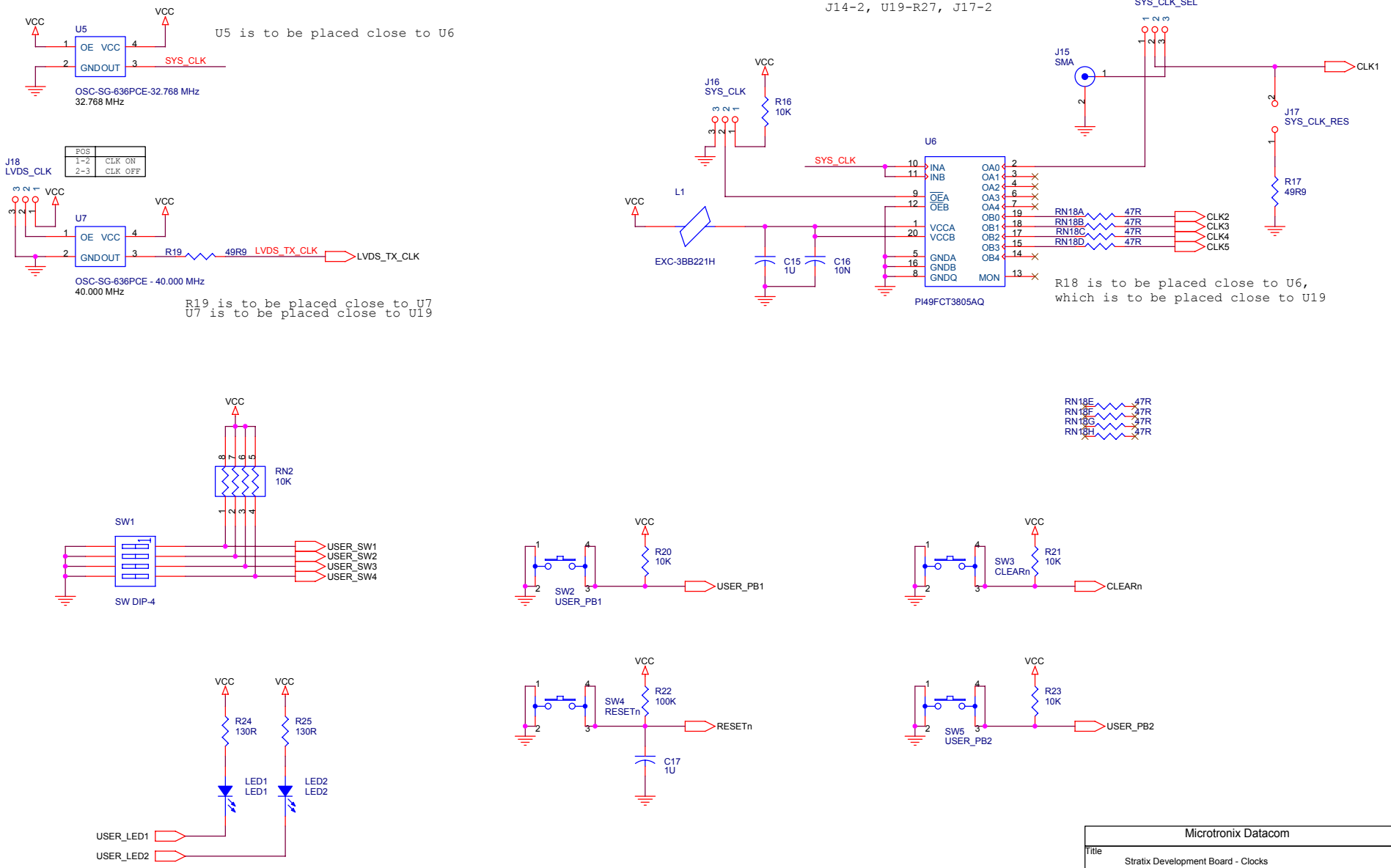

Microtronix Datacom			
Title: Stratix Development Board - Clocks			
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TXOP, TXON, RXIP, and RXIN
are to be routed on the internal layers
using 5/5 trace rules. They are not to be routed
for more the 500 mils on the top layer.
Sequencing rules for the following:
TXOP: U8-61, J19-11, R28-1
TXON: U8-62, J19-10, R29-1
RXIP: J19-7, U8-52, R30-1
RXIN: J19-6, U8-51, R31-1

R32 is to be placed close to U8

Place R33 close to U8

Place U9 close to U8 pin 4

PINS	FUNCTION
SW1[1:5]	PHYAD[0:4]
SW1[6:8]	TECH[0:2]
SW1[9]	ANEGA

Table to be placed on
the board in silk screen

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Title	Stratix Development Board-Ethernet PHY
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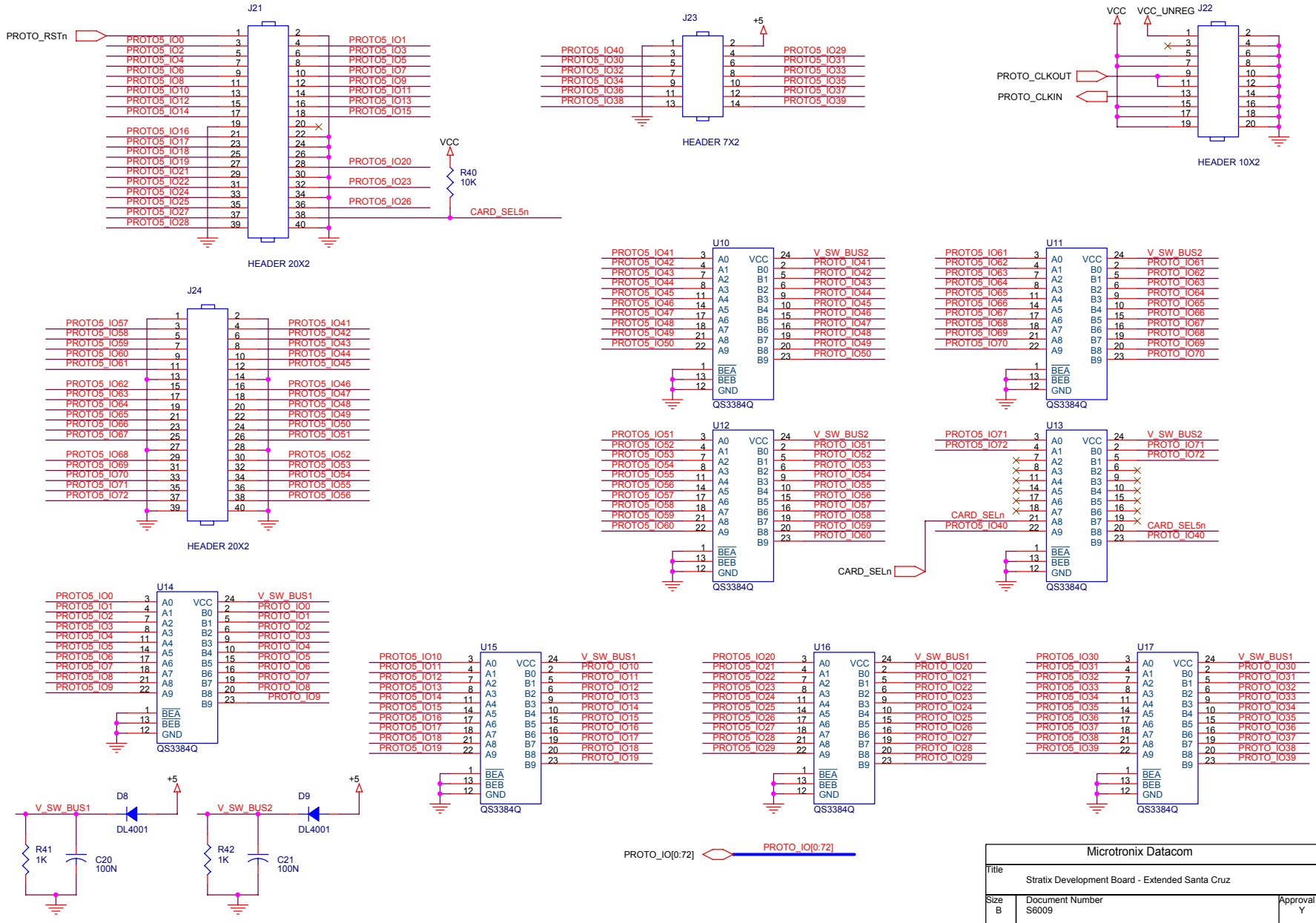

Microtronix Datacom			
Title: Stratix Development Board - Extended Santa Cruz			
Size: B	Document Number: S6009	Approval: Y	Rev: C
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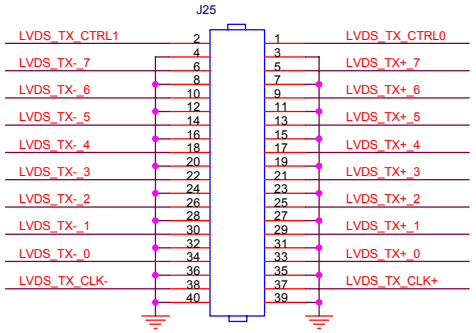
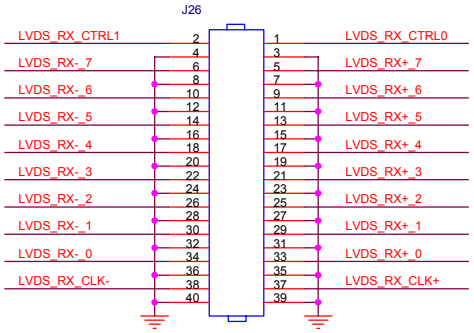
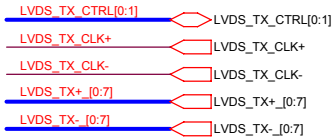


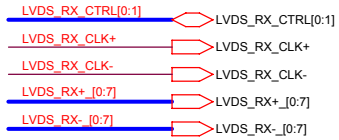


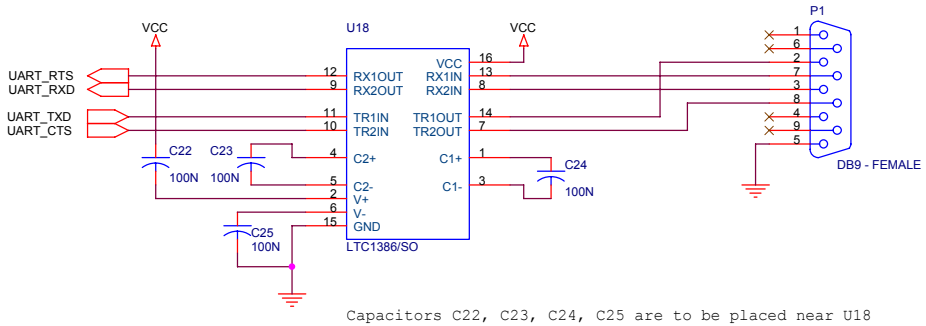
LVDS Rx and Tx signals are to be 5 mils in length, routed on the internal layers, and routed less than 500 mils on the top layer at their ends.

The spacing between LVDS pairs is to be 5 mils, while the spacing between seperate LVDS pairs are to be 8 mils.

All digital signals are to be 20 mils away from any LVDS siganls.







Capacitors C22, C23, C24, C25 are to be placed near U18

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Microtronix Datacom			
Title: Stratix Development Board - PLD I/O 1			
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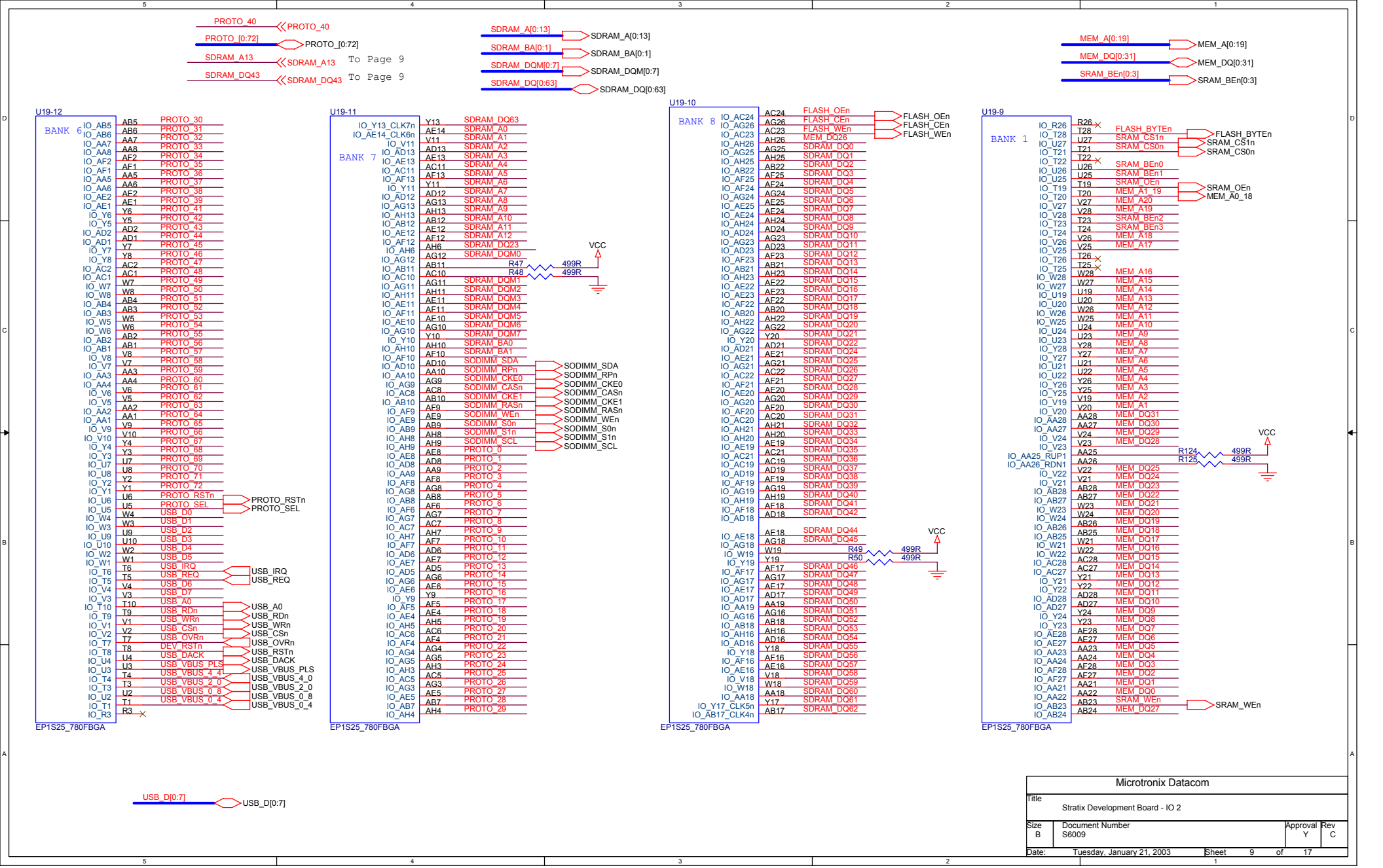

Microtronix Datacom			
Title: Stratix Development Board - IO 2			
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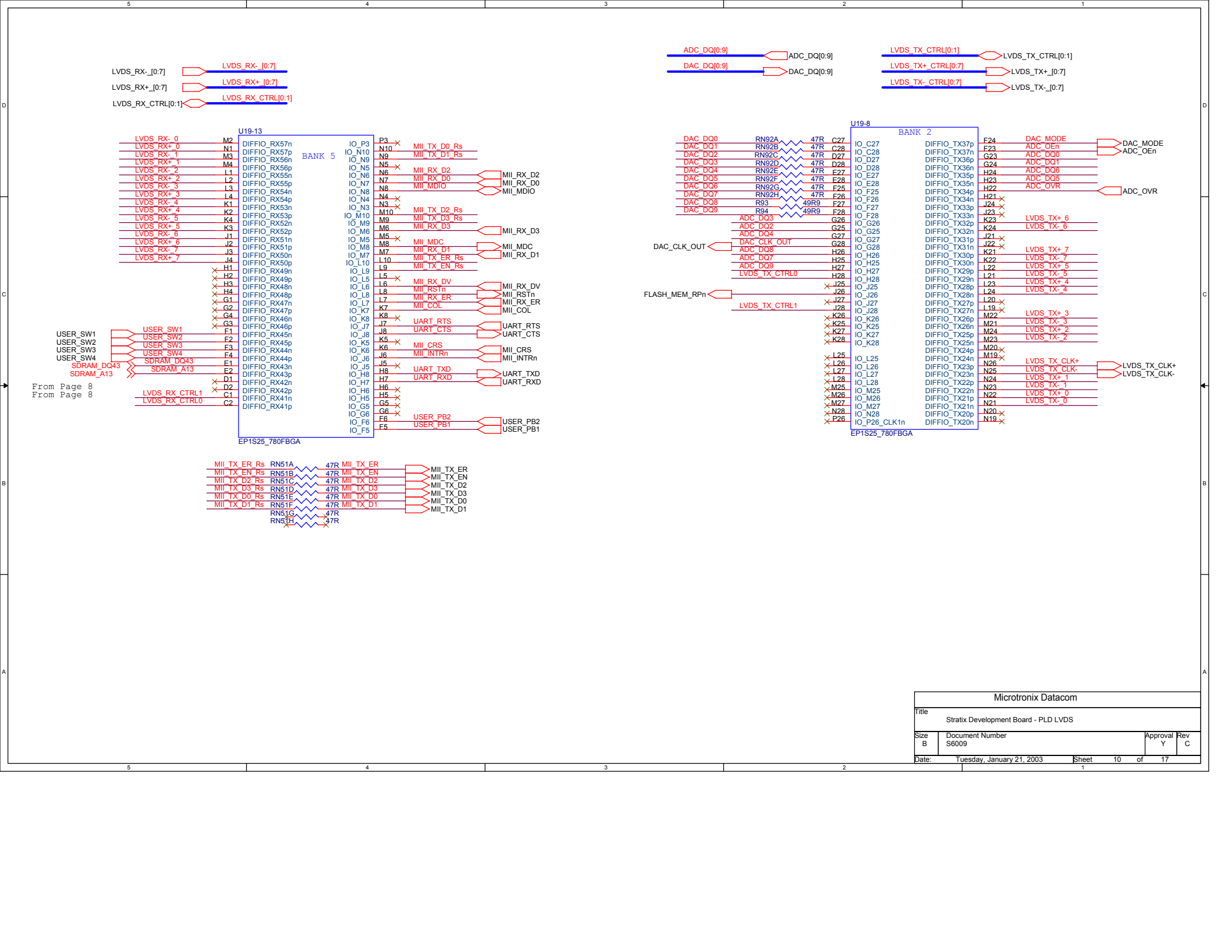
LVDS_RX-_[0:7]
LVDS_RX+_[0:7]
LVDS_RX_CTRL[0:1]
ADC_DQ[0:9]
DAC_DQ[0:9]
LVDS_TX_CTRL[0:1]
LVDS_TX+_CTRL[0:7]
LVDS_TX-_CTRL[0:7]
U19-13
BANK 5
EP1S25_780FBGA
U19-8
BANK 2
EP1S25_780FBGA
From Page 8
From Page 8
FLASH_MEM_RPn
DAC_CLK_OUT
Microtronix Datacom
Stratix Development Board - PLD LVDS
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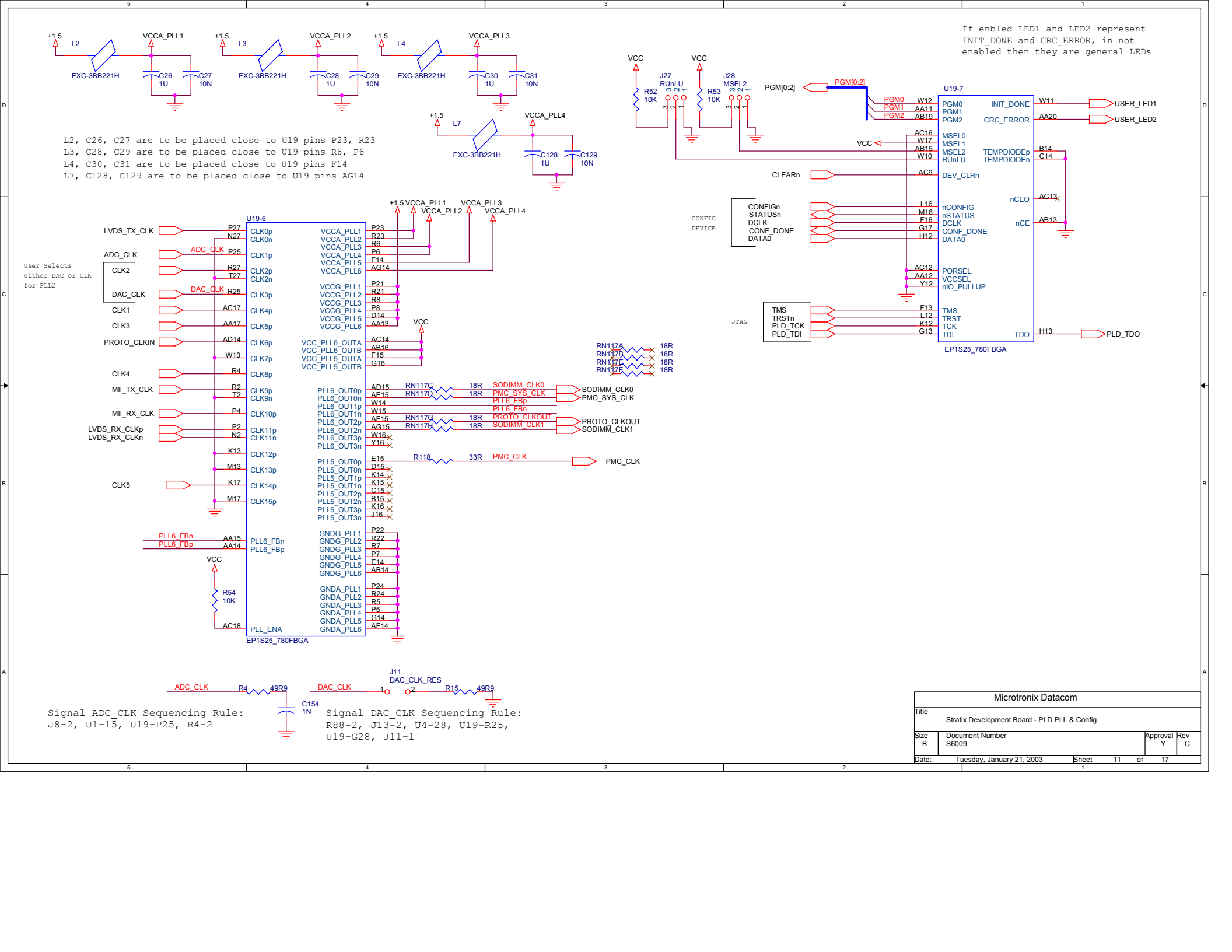
If enbled LED1 and LED2 represent INIT_DONE and CRC_ERROR, in not enabled then they are general LEDs
L2, C26, C27 are to be placed close to U19 pins P23, R23
L3, C28, C29 are to be placed close to U19 pins R6, P6
L4, C30, C31 are to be placed close to U19 pins F14
L7, C128, C129 are to be placed close to U19 pins AG14
User Selects either DAC or CLK for PLL2
Signal ADC_CLK Sequencing Rule:
J8-2, U1-15, U19-P25, R4-2
Signal DAC_CLK Sequencing Rule:
R88-2, J13-2, U4-28, U19-R25,
U19-G28, J11-1
U19-6
EP1S25_780FBGA
U19-7
EP1S25_780FBGA
CONFIG DEVICE
JTAG
Microtronix Datacom
Title
Stratix Development Board - PLD PLL & Config
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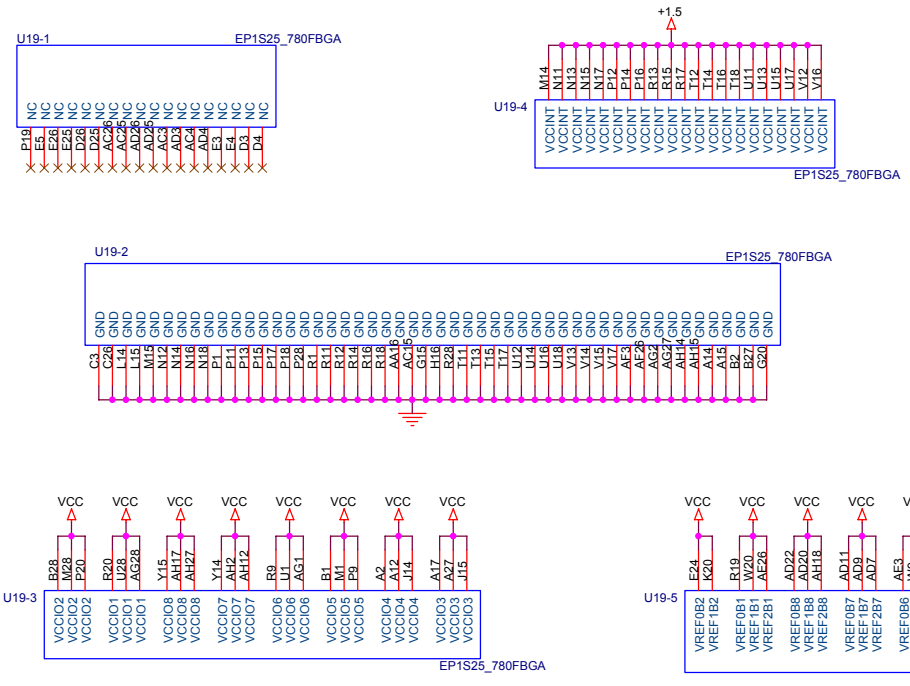

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Title: Stratix Development Board - PLD Power			
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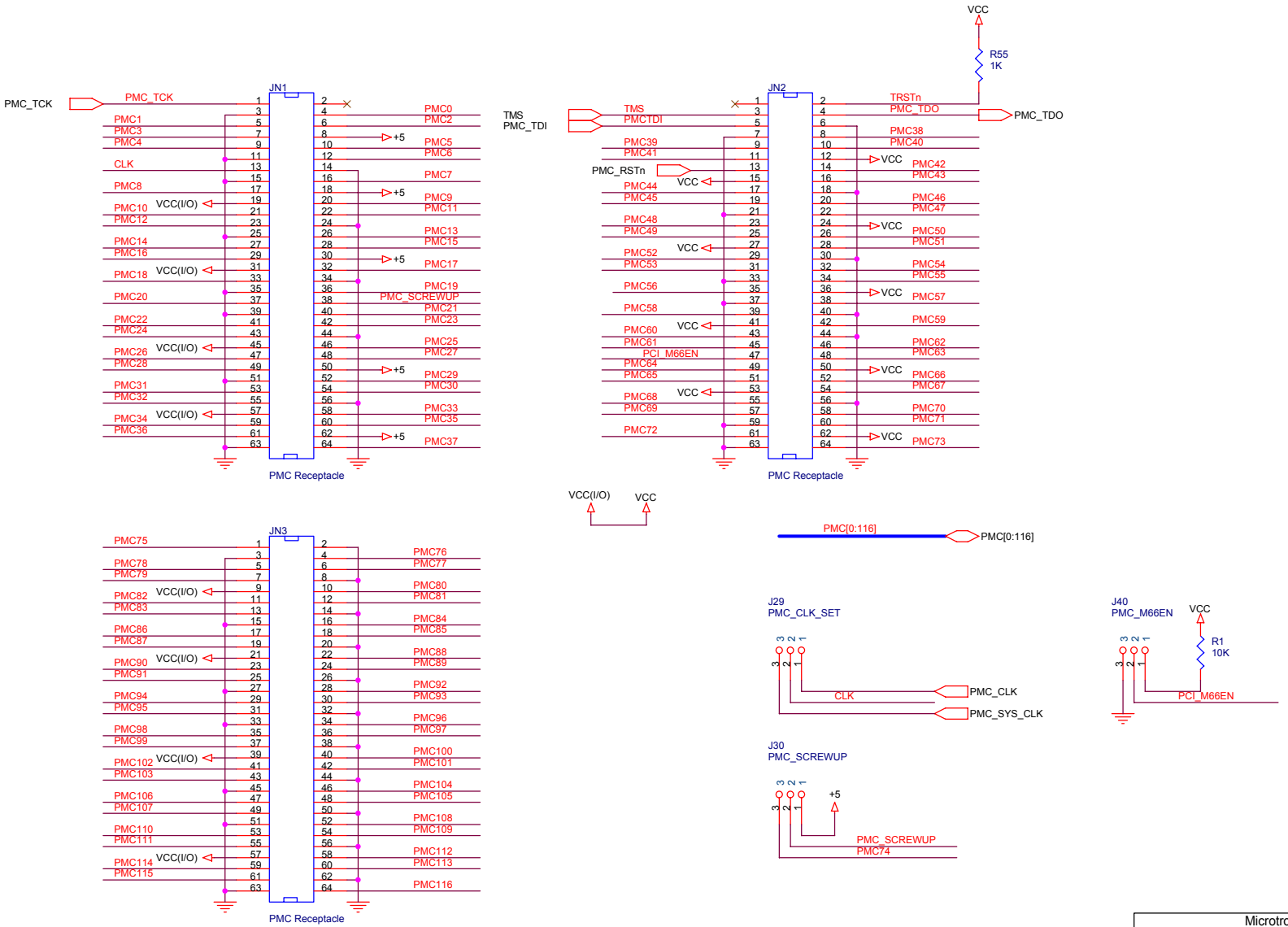

Microtronix Datacom			
Title: Stratix Development Board - PMC			
Size: B	Document Number: S6009	Approval: Y	Rev: C
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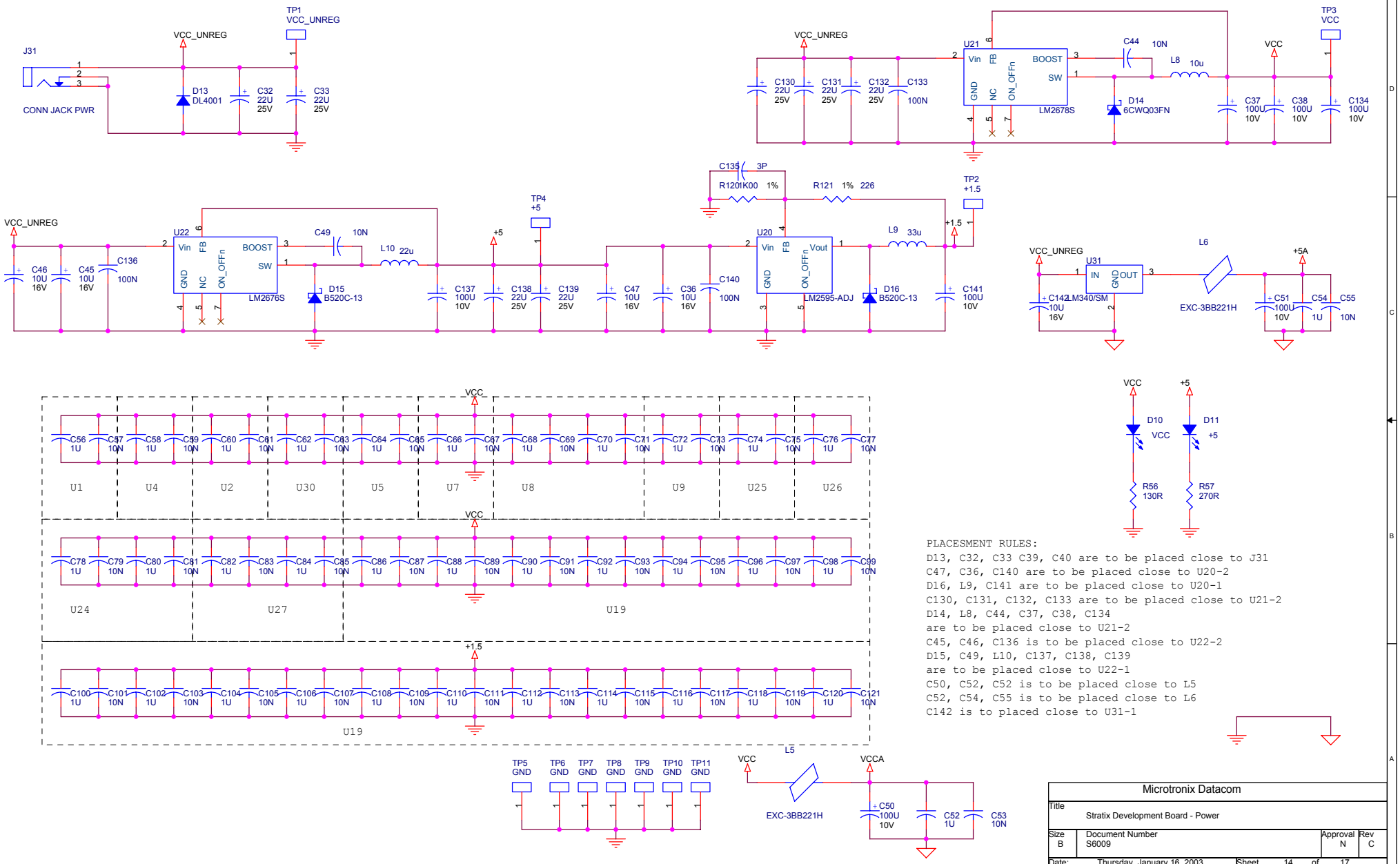
J31
CONN JACK PWR
D13
DL4001
C32
22U
25V
C33
22U
25V
TP1
VCC_UNREG
VCC_UNREG
C130
22U
25V
C131
22U
25V
C132
22U
25V
C133
100N
U21
Vin
FB
BOOST
SW
GND
NC
ON_OFFn
LM2678S
C44
10N
L8
10u
D14
6CWQ03FN
C37
100U
10V
C38
100U
10V
C134
100U
10V
TP3
VCC
VCC_UNREG
C46
10U
16V
C45
10U
16V
C136
100N
U22
LM2676S
C49
10N
L10
22u
D15
B520C-13
C137
100U
10V
C138
22U
25V
C139
22U
25V
TP4
+5
C47
10U
16V
C36
10U
16V
C140
100N
C135
3P
R1201K00
1%
R121
1%
226
TP2
+1.5
U20
LM2595-ADJ
L9
33u
D16
B520C-13
C141
100U
10V
VCC_UNREG
U31
LM340/SM
C142
10U
16V
L6
EXC-3BB221H
+5A
C51
100U
10V
C54
1U
C55
10N
VCC
+5
D10
D11
R56
130R
R57
270R
C56
1U
C57
10N
C58
1U
C59
10N
C60
1U
C61
10N
C62
1U
C63
10N
C64
1U
C65
10N
C66
1U
C67
10N
C68
1U
C69
10N
C70
1U
C71
10N
C72
1U
C73
10N
C74
1U
C75
10N
C76
1U
C77
10N
U1
U4
U2
U30
U5
U7
U8
U9
U25
U26
C78
1U
C79
10N
C80
1U
C81
10N
C82
1U
C83
10N
C84
1U
C85
10N
C86
1U
C87
10N
C88
1U
C89
10N
C90
1U
C91
10N
C92
1U
C93
10N
C94
1U
C95
10N
C96
1U
C97
10N
C98
1U
C99
10N
U24
U27
U19
C100
1U
C101
10N
C102
1U
C103
10N
C104
1U
C105
10N
C106
1U
C107
10N
C108
1U
C109
10N
C110
1U
C111
10N
C112
1U
C113
10N
C114
1U
C115
10N
C116
1U
C117
10N
C118
1U
C119
10N
C120
1U
C121
10N
U19
TP5
GND
TP6
GND
TP7
GND
TP8
GND
TP9
GND
TP10
GND
TP11
GND
L5
EXC-3BB221H
C50
100U
10V
C52
1U
C53
10N
PLACEMENT RULES:
D13, C32, C33 C39, C40 are to be placed close to J31
C47, C36, C140 are to be placed close to U20-2
D16, L9, C141 are to be placed close to U20-1
C130, C131, C132, C133 are to be placed close to U21-2
D14, L8, C44, C37, C38, C134
are to be placed close to U21-2
C45, C46, C136 is to be placed close to U22-2
D15, C49, L10, C137, C138, C139
are to be placed close to U22-1
C50, C52, C52 is to be placed close to L5
C52, C54, C55 is to be placed close to L6
C142 is to placed close to U31-1
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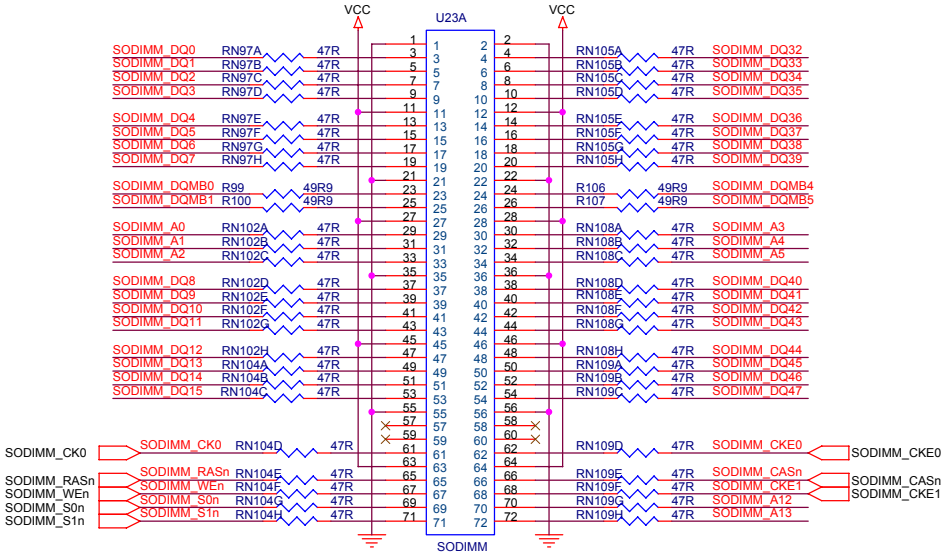

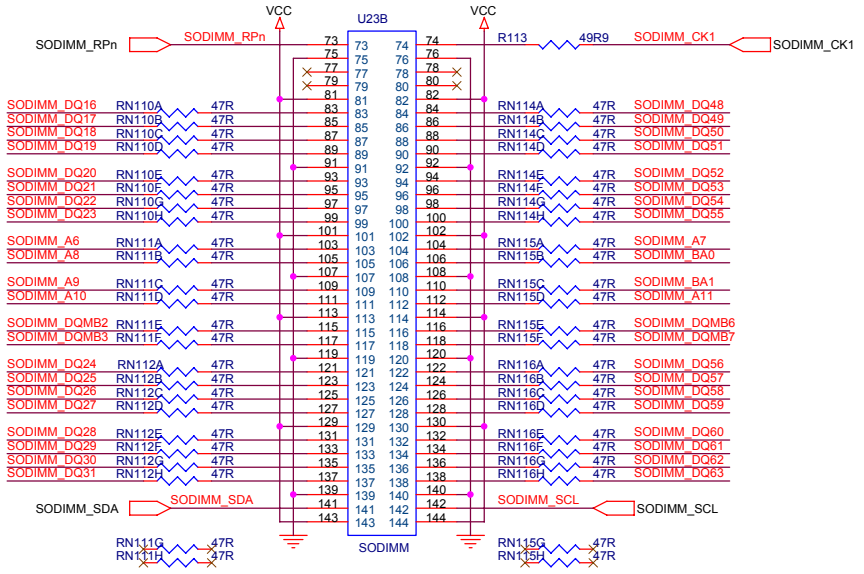

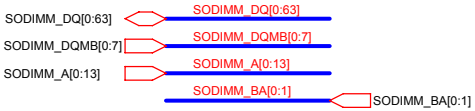

Resistors R97 to R116 are to be placed close to the connector U23.

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Title: Stratix Development Board - SODIMM			
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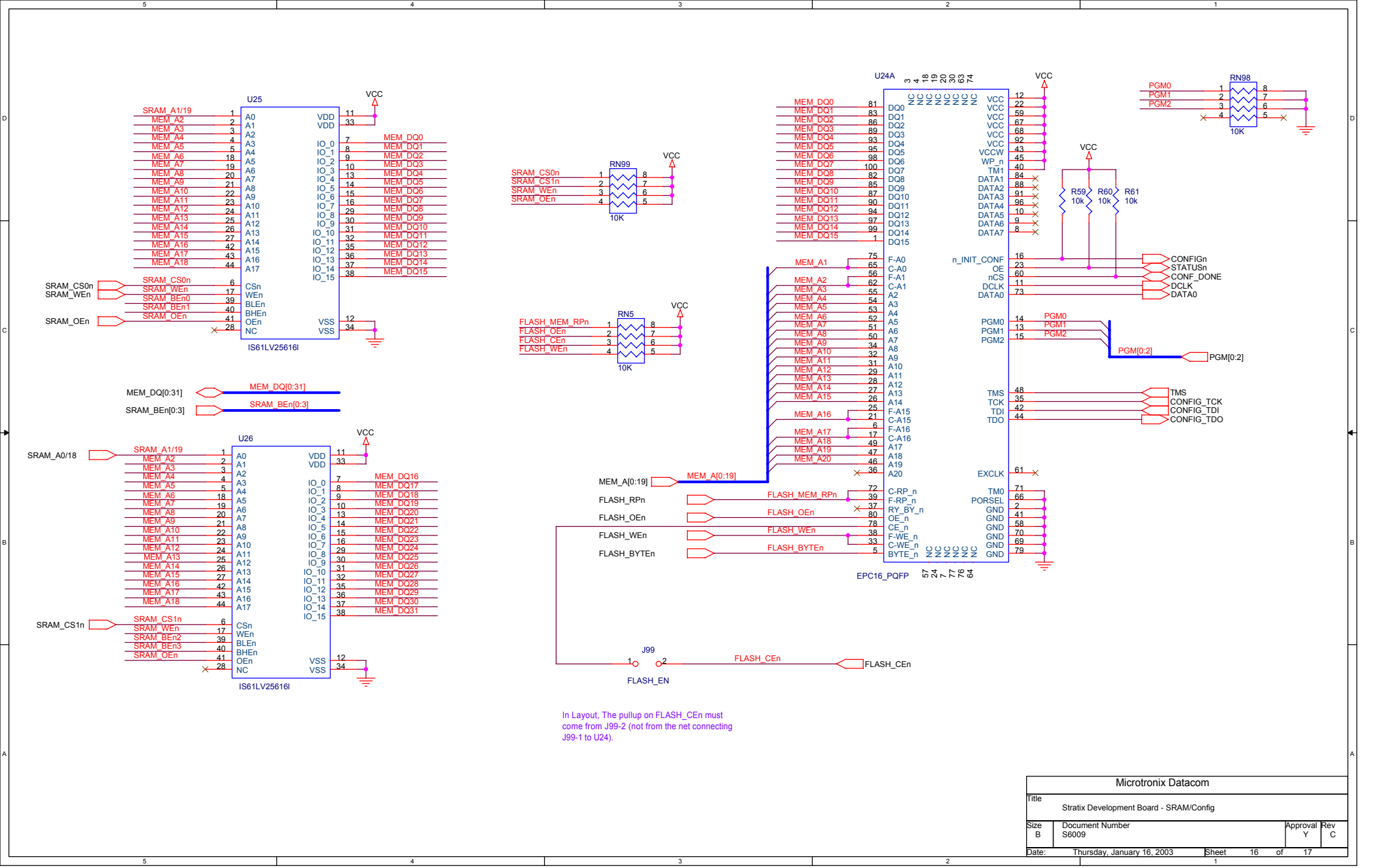

Microtronix Datacom			
Title: Stratix Development Board - SRAM/Config			
Size: B	Document Number: S6009	Approval: Y	Rev: C
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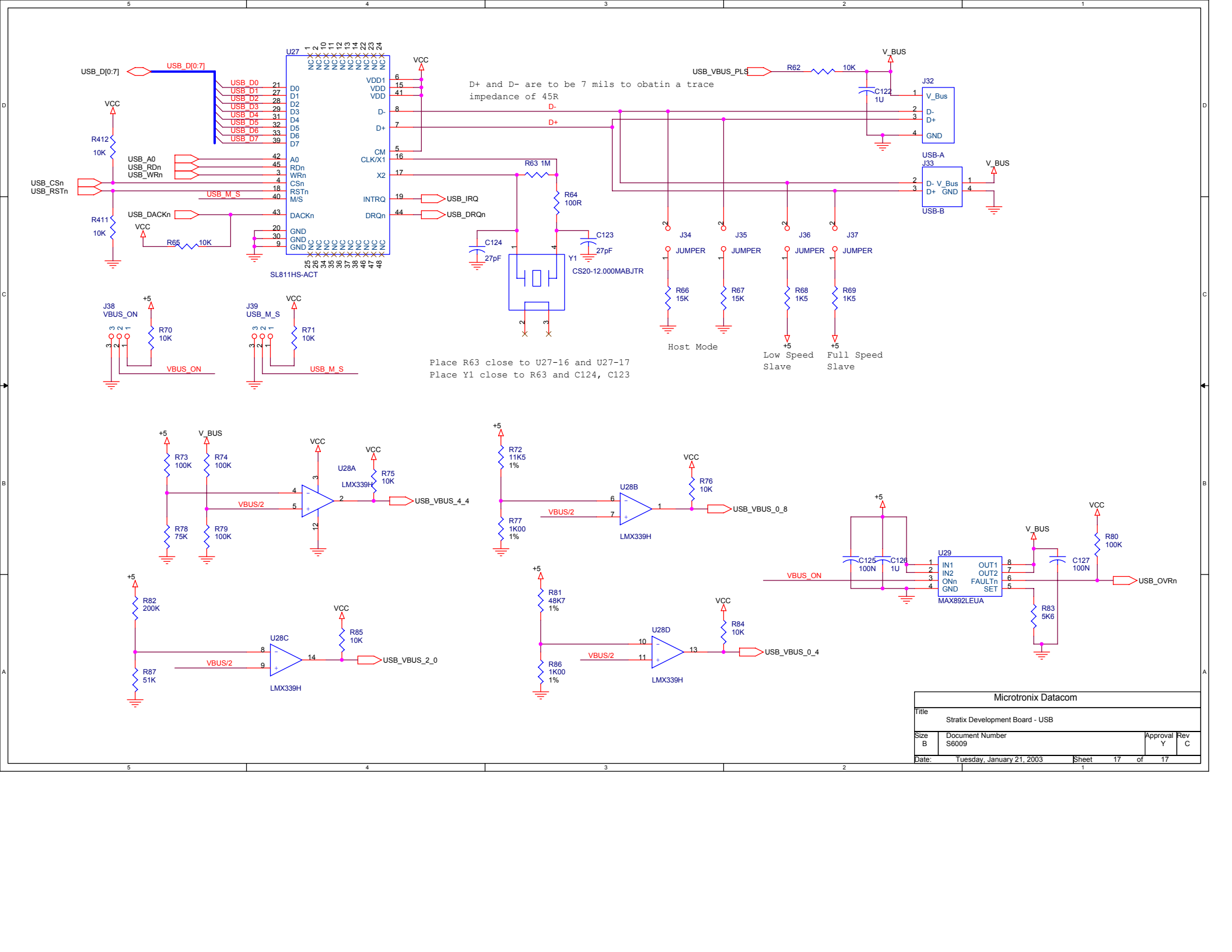
U27
SL811HS-ACT
USB_D[0:7]
USB_A0
USB_RDn
USB_WRn
USB_CSn
USB_RSTn
USB_M_S
USB_DACKn
USB_IRQ
USB_DRQn
D+ and D- are to be 7 mils to obatin a trace impedance of 45R
R63 1M
R64 100R
C124 27pF
C123 27pF
Y1 CS20-12.000MABJTR
Place R63 close to U27-16 and U27-17
Place Y1 close to R63 and C124, C123
USB_VBUS_PLS
R62 10K
C122 1U
J32
J33
USB-A
USB-B
J34 JUMPER
J35 JUMPER
J36 JUMPER
J37 JUMPER
R66 15K
R67 15K
R68 1K5
R69 1K5
Host Mode
Low Speed Slave
Full Speed Slave
J38 VBUS_ON
J39 USB_M_S
R70 10K
R71 10K
U28A LMX339H
U28B LMX339H
U28C LMX339H
U28D LMX339H
R73 100K
R74 100K
R75 10K
R76 10K
R78 75K
R79 100K
R72 11K5 1%
R77 1K00 1%
R81 48K7 1%
R82 200K
R84 10K
R85 10K
R86 1K00 1%
R87 51K
VBUS/2
USB_VBUS_4_4
USB_VBUS_0_8
USB_VBUS_0_4
USB_VBUS_2_0
U29 MAX892LEUA
C125 100N
C126 1U
C127 100N
R80 100K
R83 5K6
USB_OVRn
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