Universe II™ (CA91C142)

What's New?

The Universe™ (CA91C042) is the industry leading VME-PCI bus-bridge. In the past, the Universe has helped many designers integrate VME and PCI on a board level. It will soon help even more. Introducing the Universe II .

The Universe II builds on the previous version's performance and functionality and boasts full backwards compatibility. All this at a comparable price. Here are some Universe II highlights:

- Fully compliant, 64-bit, PCI and VME interfaces,
- Programmable DMA controller, with linked list support,
- Full VMEbus system controller functionality,
- Four, 32-bit mailboxes for interrupt generation on either bus,
- Location monitor for interrupts and message passing,
- Seven VME software interrupts,
- Industrial temperature operation (-40° to +85°C),
- Second PCI_BS register with 4Kbyte resolution,
- Two semaphore registers to control access to system resources,
- PCI Target Channel coupled cycle performance enhancement (2X)
- DMA performance enhancement,
- Power reduction (20%),
- Deep FIFOs (64 bits wide, 32 entries deep),
- Additional PCI Target Channel and VME Slave Channel images, and
- Full Universe pin and function compatibility.

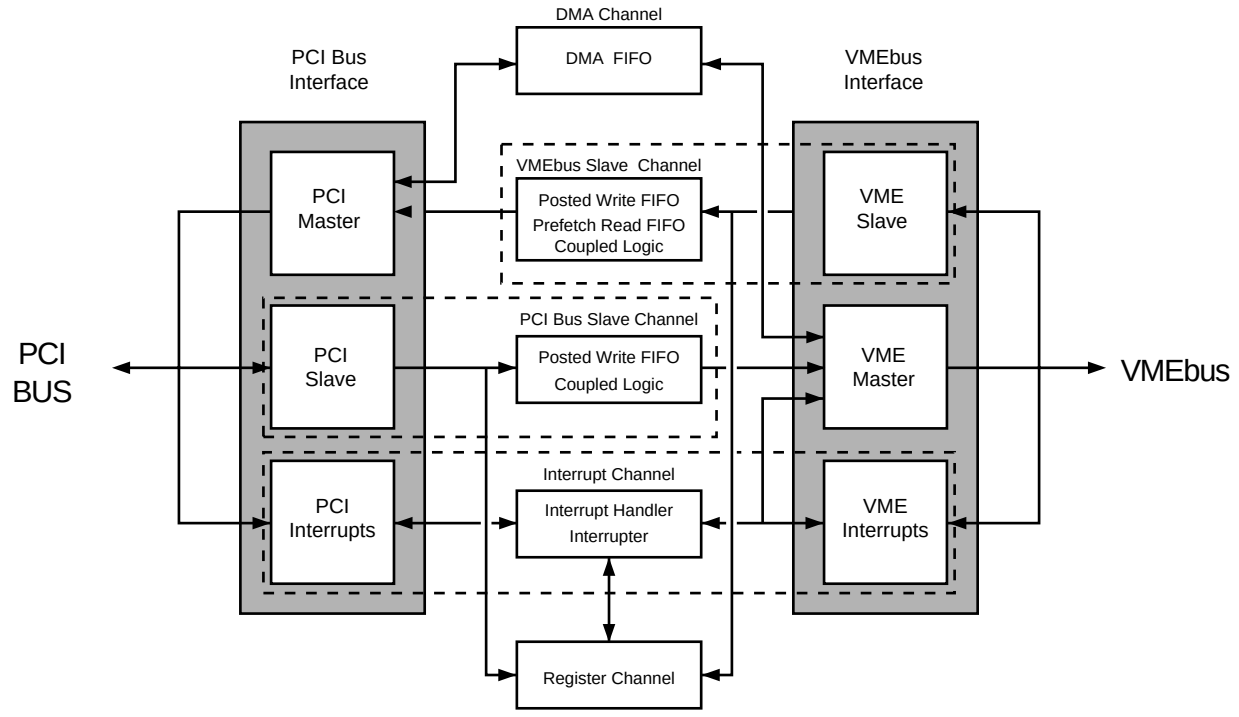


Figure 1 : Functional Block Diagram of the Universe II

1 Why Universe II?

The Universe's initial market introduction was well received. In fact, it is currently "designed in" by all major VMEbus merchant board vendors and continues to enjoy ever increasing industry acceptance.

Tundra recognizes the significance of its commitment to the VME community. As a result, we are dedicated to keeping pace with changes in VMEbus technology and intend to constantly increase the Universe's functionality and performance. The Universe II does just that.

The Universe II includes increased functionality in the form of additional programming resources, greater data transfer rates and lower power consumption while maintaining full Universe backwards compatibility. Current users can drop the Universe II into existing Universe sockets and expect correct, seamless operation.

2 New Features

The following section highlights the Universe II's increased performance and functionality.

2.1 Performance Enhancements

Universe II users will enjoy increased Universe performance in a number of areas. The DMA has been optimized to better utilize each bus in a range of applications, while PCI Target Channel coupled performance doubles. Linked-list DMA performance is also augmented with improved internal DMA read handling and by increasing the depth of all FIFOs. In addition, PCI bandwidth is optimized with support for bus parking and request mechanisms and a new PCI burst transfer length of 128 bytes.

2.2 Mailboxes

In order to add more interrupt generation power, the Universe II includes four 32-bit mailbox registers. These registers are located in the existing register space and are therefore accessible by both buses via the normal register access mechanisms. Each mailbox is capable of generating an interrupt on either bus.

2.3 Location Monitor

The Universe II includes a single VMEbus location monitor that allows the implementation of a VME interrupt broadcast mechanism. The Universe II's location monitor responds to a user specified address range by generating one of four interrupts on the PCI bus. The interrupt level that is generated is determined through an examination of VMEbus address bits [3:2]. Each interrupt can be individually enabled and routed to any PCI interrupt level. DTACK* is asserted by the initiating device only.

2.4 VME Software Interrupts

The Universe II expands on the existing software interrupt capability of the Universe by supporting seven new VMEbus software interrupts. Each of the new interrupts are accessible via the normal register space and are hardwired to a matching VMEbus level.

2.5 PCI Base Address Registers

In order to give users more flexibility in tightly constrained I/O space, the Universe's PCI register image was modified from its previous 64Kbyte granularity to a 4Kbyte grain. In addition, a second PCI image register with 4Kbyte resolution is included to allow Universe register accesses from Memory and I/O spaces.

2.6 Semaphore Register Addition

The Universe II supports eight semaphores, accessible in the normal register space. These semaphores provide improved control over access to system resources.

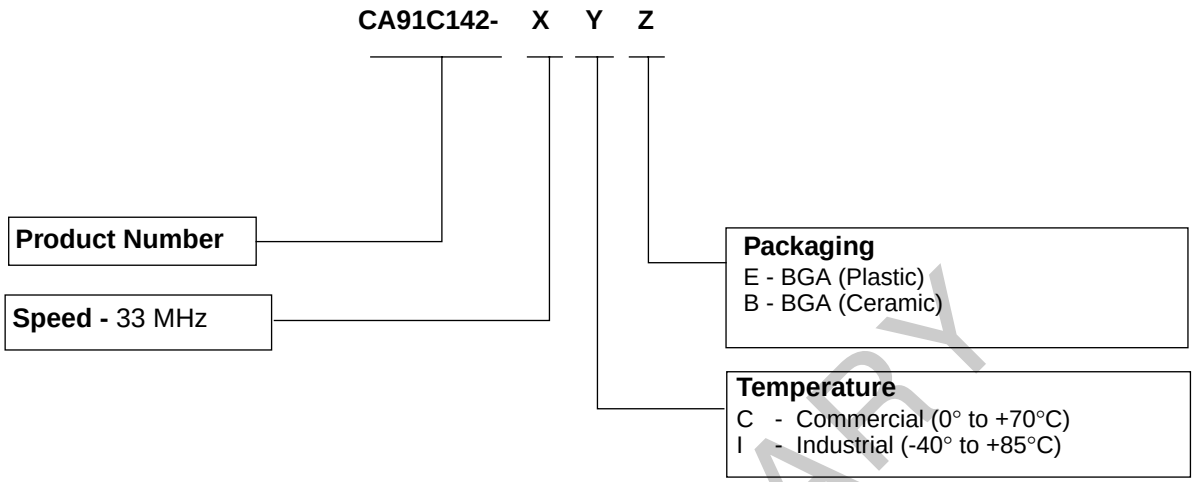
2.7 Power Reduction

Thanks to migration to a smaller geometry, Universe II users can expect a 20% power reduction from that of the Universe.

3 Further Information

The Universe II will be available for sampling in the spring of 1997. More detailed material on this product, in the form of a manual addendum, will be ready in April. For the most up-to-date information, please visit our website at www.tundra.com.

Ordering Information and Product Code



Tundra products are designated by a Product Code. When ordering, refer to products by their full code. For unusual, and/or specific packaging or processing requirements not covered by the standard product line, please contact our factory directly.

Note that all products are not necessarily available in all packages.

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