Universe II™ Users' Guide

Visit our Website at: **www.tundra.com**

603 March Rd., Kanata, Ontario, K2K 2M5
Tel: (613) 592-0714 • 1-800-267-7231 • Fax: (613) 592-1320

Document Number : 8091142.XS142.01
Printed in Canada
Information in this document is subject to change without notice

The information in this document is subject to change without notice and should not be construed as a commitment by Tundra Semiconductor Corporation. While reasonable precautions have been taken, Tundra Semiconductor Corporation assumes no responsibility for any errors that may appear in this document.

Tundra® products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Tundra product could create a situation where personal injury or death may occur. Should Buyer purchase or use Tundra products for any such unintended or unauthorized application, Buyer shall indemnify and hold Tundra and its officers, employees, subsidiaries, affiliates and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Tundra was negligent regarding the design or manufacture of the part.

The acceptance of this document will be construed as an acceptance of the foregoing conditions.

Universe II™ Users' Guide

Document: 8091142.XS142.01

Printed in Canada

Table of Contents

1 Introduction

Tundra's latest revision of its VME-PCI bridge, the Universe II™, was designed to correct errata, increase performance and have full backwards compatibility with the original Universe. In addition, the Universe II boasts a number of new features to provide greater flexibility and power when using the device.

In order to improve performance and correct errata, minor changes were, of necessity, made to the original design. These changes are transparent to existing Universe software (provided that users have connected their devices as recommended in the Universe manual). This document captures the most important of the changes and details the new features offered by the Universe II.

In order to understand the *complete* operation of the Universe II, this document should be used in conjunction with Tundra's *VMEbus Interface Components Manual* (document 9000000.MD303.01). The most current revisions of all Universe technical documentation are posted on our web site at **www.tundra.com.**

2 Changes

In order to properly address the performance and functionality issues of the original device, a number of minor changes were made to the original design. The most important of these are captured in this section.

Caution: Users who have connected their original Universe devices differently from the manner shown in Figure C.1 of the VMEbus Interface Components Manual may have compatibility problems when attempting to use the Universe II as a drop-in replacement.

2.1 Revision ID

The low byte of the PCI_CLASS register (page 17) has been changed to reflect the new device revision number (01).

2.2 PCI Clock Frequency

The PCI clock frequency of the Universe II must be between 25 and 33MHz. Lower frequencies will result in invalid VME timing.

2.3 Register Reset Values

A number of register bits in the original Universe device had undefined reset values ("x"). This is no longer the case. All registers in the Universe II now have defined reset values.

2.4 Use of the Coupled Request Timer

The Universe II no longer uses the coupled request timer (CRT) value in the LMISC register (see page 21). Now, the coupled request phase will expire if no coupled transfer occurs within 2^{15} PCI clock cycles. The CRT field may still be written to and read from.

2.5 MFUNCT Field in PCI_MISC0

The original Universe device set the MFUNCT field in the PCI_MISC0 field to '1'. This required that the Universe examine the state of the AD[10:8] lines during Type 0 configuration accesses. The MFUNCT field in the Universe II is now set to '0' (see page 16) and the address lines are not examined.

2.6 Config Type 1 Accesses

The Universe I insufficiently supported the mapping of PCI Config 1 Cycles to the VMEbus. In order to simplify the logic of the Universe II, Config Type 1 cycle mapping to VME was removed. Accordingly, the upper "Type 1 Configuration Space" bit was removed from each of the LAS fields in the Universe II's "PCI Slave Image Control" registers (LSIxx_CTL). The remaining LAS bit allows for the selection of either Memory or I/O type PCI accesses.

2.7 PCI Base Address Registers

The Universe's original PCI_BS register has been modified to have a 4Kbyte resolution. In addition, a second base address image with 4Kbyte resolution has been added. This will allow both greater flexibility in tightly constrained I/O space and the "on-the-fly" option to access the Universe II's registers from either I/O or Memory space.

The PCI_BS[15:12] bits of the original register settings are no longer hardwired to logic zero. However, since these bits power-up in a low configuration, existing Universe software should not be affected (providing that the software was not writing to PCI[15:8] - see page 18).

The new PCI_BS register called the "PCI Configuration Base Address Register1", or PCI_BS1, also has a 4Kbyte resolution. Its "space" field (i.e. Memory or I/O - page 19) will be the logical inversion of the comparable value found in the PCI_BS.

2.8 DGCS VON[3]

Bit 23 of the "DMA General Control / Status Register", on page 38, was not used in the original Universe design. It is now a reserved bit.

2.9 IACKIN* Monitoring

When configured as SYSCON, the Universe II will monitor IACK* rather than IACKIN*. This permits it to operate as the SYSCON in places other than slot 1. The slot with SYSCON in it becomes a virtual slot 1.

2.10 Rescinding DTACK

The state of the RESCIND bit in the MISC_CTL register (page 59) is ignored by the Universe II. Although it may still be written to and read from, its state no longer affects Universe operation. The Universe II always rescinds DTACK.

2.11 Changes to Resets

The original Universe device used to load power-up options only when a power-up reset occurred. If the Universe was reset at a later time by either PCI (RST#) or VME (SYSRESET*), the power-up options would be cleared.

The Universe II latches power-up options on the rising edge of PWRRST#. In the case of a subsequent SYSRST* or RST#, the values that were originally loaded at the rising edge of PWRRST# will be restored.

3 New Features

The Universe II has several new features. Each of these has been classified below as either "general" or "performance". General features are those that allow for greater overall flexibility and power when using the Universe II. The performance features are those that will allow Universe II users to enjoy increased performance over the original Universe device.

3.1 General

These features will give Universe II users more power to control their system operations. The use and operation each feature is explored and explained in detail.

3.1.1 Mailboxes

In order to give users increased "cross-bus interrupt generation power", the Universe II includes four, 32-bit mailbox registers, starting at offset 348 (see page 51). Once enabled, (in the "Local Interrupt Enable Register", on page 40) writing control and status data to these registers causes an interrupt to be generated on either or both buses. (Reading from the same mailboxes will not generate interrupts.) Interrupt handling routines can examine the status of the mailbox registers and retrieve data as appropriate.

Mailbox initiated interrupt generation is controlled by additions to existing Universe interrupt enable registers (see "Local Interrupt Enable Register", on page 40 and "VME Interrupt Enable Register", on page 44). Two new interrupt map registers ("Local Interrupt Map 2 Register", on page 49 and "VME Interrupt Map 2 Register", on page 50) allow each of the mailboxes to generate one of eight interrupts on PCI and one of the seven on VME. Mailbox interrupt status may be verified by examining the appropriate bits that have been added to the "Local Interrupt Status Register" on page 42, and the "VME Interrupt Status Register" on page 47.

3.1.2 Location Monitor

The Universe II's location monitor allows for broadcast events across the VME backplane. Each Universe II that shares the same enabled location monitor image will respond to a read or write within that range by generating one of four internal Universe "interrupts". Each of these can be individually enabled and mapped to specific interrupts on PCI. (The location monitor does not respond to block transfers or ADO cycles.) If a Universe II initiated the cycle, it will properly terminate the cycle with the assertion of DTACK. Otherwise, another agent is responsible to do so.

The Universe's new location monitor is governed by the settings in the "Location Monitor Control" register (page 61). From there, the image is enabled and the transaction decode type (AM code, address width) defined. The base address of the 4Kbyte image is programmed into the "Location Monitor Base Address Register" (page 62). Once accessed correctly, an

internal "interrupt" is generated whose level is based on the value of VME address bits [4:3] (see Table 3.1). Each of the four internal interrupts can be individually enabled and routed to any of eight PCI interrupt levels in the "Local Interrupt Map 2 Register", on page 49.

Table 3.1: Mapping AD[4:3] to LM0-LM3

AD[4:3]	LMx
00	LM0
01	LM1
10	LM2
11	LM3

3.1.3 Additional Slave Images

The Universe II has four additional programmable slave images for each of the two buses. On both PCI and VME, a new image with 4 Kbyte granularity has been added. The three additional images have 64 Kbyte granularity. These new images (starting at offset 1A0 for PCI and F90 for VME) will give users greater flexibility for passing data from one bus to the other.

3.1.4 VME Software Interrupts

In the past, Universe users generated software initiated VME interrupts by mapping the single software interrupt to a specific IRQ level and then activating it. Later, if they wanted to generate an interrupt on a different level, they would have to reprogram the interrupt mapping.

The Universe II has expanded VME software interrupts such that each of the seven IRQ levels can be generated *directly* by writing to the appropriate register location (see "VME Interrupt Enable Register", on page 44). The status of each of the interrupts can be verified by examining the new bits included in the "VME Interrupt Status Register" on page 47.

3.1.5 Semaphores

The Universe II has eight semaphores, accessible from two registers in the normal register space (page 55). Each of the registers has a status bit ("active" or "inactive") and an associated 7 bit tag field. Designers can use the semaphores to ensure exclusive access to system resources on either of the two buses.

Each of the semaphores power-up with logic zero. When a process wishes to gain control of a specific resource, it writes a one to the status bit and a unique pattern to the tag field of the resource's associated semaphore. If a subsequent read of the tag field returns the same pattern, the process can consider itself the owner of the semaphore. Writing a zero to the semaphore's status field releases it for use by other processes.

Once the semaphore field is set, the semaphore and the tag data cannot be changed unless the new semaphore value is zero; the semaphore can only be updated if the semaphore value is zero. Semaphore registers should be accessed with byte-wide accesses.

3.1.6 New SCYC_CTL LAS Field

The Universe II now supports both Memory and I/O accesses to the special cycle generator image. Accordingly, a new LAS bit has been added to the SCYC_CTL register (see page 20).

3.2 Performance

In addition to double FIFO depth, optimized state machines and improved linked list performance, the Universe II includes a number of handy features whose use will result in increased performance over the original Universe device. This section details those features.

3.2.1 Early Release of BBSY*

Whenever possible, the Universe II will execute an early release of BBSY* in order to optimize its use of the VMEbus.

3.2.2 VOFF/VON

Three additional settings, 2, 4 and 8µsecs, have been added to the VOFF timer that is found in the DGCS (page 38). These new settings will allow users to better "fine-tune" VMEbus usage. In addition, the Universe II's DMA will now execute an early release of BBSY* if the VON timer expires.

3.2.3 Aligned Burst Size

The original Universe had two PCI aligned burst sizes (PABS) of 32 and 64 bytes. The Universe II supports an additional PABS setting of 128 bytes. An additional bit has been added to the PABS field in the MAST_CTL register (page 57) in order to accommodate this change.

The PABS setting no longer effects watermarks in FIFOs and will only impact bursting onto the PCI bus by the Universe II's PCI Master module. Burst transactions addressed to the Universe II and initiated by external PCI masters will be accepted provided there are at least 128 bytes free in the TXFIFO.

3.2.4 PCI Bus Parking

When the PCI Master module of the Universe I is ready to begin a transaction, it always asserts REQ# and then waits for GNT# before beginning its transfer. The Universe II will only assert REQ# if it is not already the PCI bus master. This eliminates a possible one clock cycle delay before starting a transaction on the PCI bus.

4 Registers

Table 4.1 details the complete register set for the Universe II. Only registers that have changed or are newly defined are included in the expanded descriptions that follow.

Rows that are greyed-out indicate changes to previously existing Universe registers. Change bars indicate registers that are newly defined for the Universe II.

Table 4.1 Universe II Register Map

Offset	Register	Name
000	PCI Configuration Space ID Register	PCI_ID
004	PCI Configuration Space Control and Status Register	PCI_CSR
008	PCI Configuration Class Register	PCI_CLASS
00C	PCI Configuration Miscellaneous 0 Register	PCI_MISC0
010	PCI Configuration Base Address Register	PCI_BS
014	PCI Configuration Base Address Register 1	PCI_BS1
018	PCI Unimplemented	
01C	PCI Unimplemented	
020	PCI Unimplemented	
024	PCI Unimplemented	
028	PCI Reserved	
02C	PCI Reserved	
030	PCI Unimplemented	
034	PCI Reserved	
038	PCI Reserved	
03C	PCI Configuration Miscellaneous 1 Register	PCI_MISC1
040-0FF	PCI Unimplemented	
100	PCI Slave Image 0 Control	LSI0_CTL
104	PCI Slave Image 0 Base Address Register	LSI0_BS
108	PCI Slave Image 0 Bound Address Register	LSI0_BD
10C	PCI Slave Image 0 Translation Offset	LSI0_TO
110	Universe Reserved	
114	PCI Slave Image 1 Control	LSI1_CTL
118	PCI Slave Image 1 Base Address Register	LSI1_BS
11C	PCI Slave Image 1 Bound Address Register	LSI1_BD
120	PCI Slave Image 1 Translation Offset	LSI1_TO
124	Universe Reserved	
128	PCI Slave Image 2 Control	LSI2_CTL

Table 4.1 Universe II Register Map

Offset	Register	Name
12C	PCI Slave Image 2 Base Address Register	LSI2_BS
130	PCI Slave Image 2 Bound Address Register	LSI2_BD
134	PCI Slave Image 2 Translation Offset	LSI2_TO
138	Universe Reserved	
13C	PCI Slave Image 3 Control	LSI3_CTL
140	PCI Slave Image 3 Base Address Register	LSI3_BS
144	PCI Slave Image 3 Bound Address Register	LSI3_BD
148	PCI Slave Image 3 Translation Offset	LSI3_TO
14C-16C	Universe reserved	
170	Special Cycle Control Register	SCYC_CTL
174	Special Cycle PCI bus Address Register	SCYC_ADDR
178	Special Cycle Swap/Compare Enable Register	SCYC_EN
17C	Special Cycle Compare Data Register	SCYC_CMP
180	Special Cycle Swap Data Register	SCYC_SWP
184	PCI Miscellaneous Register	LMISC
188	Special PCI Slave Image	SLSI
18C	PCI Command Error Log Register	L_CMDERR
190	PCI Address Error Log	LAERR
194-19C	Universe reserved	
1A0	Local Slave Image 4 Control	LSI4_CTL
1A4	Local Slave Image 4 Base Address Register	LSI4_BS
1A8	Local Slave Image 4 Bound Address Register	LSI4_BD
1AC	Local Slave Image 4 Translation Offset	LSI4_TO
1B0	Universe Reserved	
1B4	Local Slave Image 5 Control	LSI5_CTL
1B8	Local Slave Image 5 Base Address Register	LSI5_BS
1BC	Local Slave Image 5 Bound Address Register	LSI5_BD
1C0	Local Slave Image 5 Translation Offset	LSI5_TO
1C4	Universe Reserved	
1C8	Local Slave Image 6 Control	LSI6_CTL
1CC	Local Slave Image 6 Base Address Register	LSI6_BS
1D0	Local Slave Image 6 Bound Address Register	LSI6_BD
1D4	Local Slave Image 6 Translation Offset	LSI6_TO
1D8	Universe Reserved	
1DC	Local Slave Image 7 Control	LSI7_CTL
1E0	Local Slave Image 7 Base Address Register	LSI7_BS
1E4	Local Slave Image 7 Bound Address Register	LSI7_BD
1E8	Local Slave Image 7 Translation Offset	LSI7_TO
1EC-1FC	Universe Reserved	

Table 4.1 Universe II Register Map

Offset	Register	Name
200	DMA Transfer Control Register	DCTL
204	DMA Transfer Byte Count Register	DTBC
208	DMA PCI bus Address Register	DLA
20C	Universe Reserved	
210	DMA VMEbus Address Register	DVA
214	Universe Reserved	
218	DMA Command Packet Pointer	DCPP
21C	Universe Reserved	
220	DMA General Control and Status Register	DGCS
224	DMA Linked List Update Enable Register	D_LLUE
228-2FC	Universe reserved	
300	PCI Interrupt Enable	LINT_EN
304	PCI Interrupt Status	LINT_STAT
308	PCI Interrupt Map 0	LINT_MAP0
30C	PCI Interrupt Map 1	LINT_MAP1
310	VMEbus Interrupt Enable	VINT_EN
314	VMEbus Interrupt Status	VINT_STAT
318	VMEbus Interrupt Map 0	VINT_MAP0
31C	VMEbus Interrupt Map 1	VINT_MAP1
320	Interrupt Status/ID Out	STATID
324	VIRQ1 STATUS/ID	V1_STATID
328	VIRQ2 STATUS/ID	V2_STATID
32C	VIRQ3 STATUS/ID	V3_STATID
330	VIRQ4 STATUS/ID	V4_STATID
334	VIRQ5 STATUS/ID	V5_STATID
338	VIRQ6 STATUS/ID	V6_STATID
33C	VIRQ7 STATUS/ID	V7_STATID
340	Local Interrupt Map 2 Register	LINT_MAP2
344	VME Interrupt Map 2 Register	VINT_MAP2
348	Mailbox 0	MBOX0
34C	Mailbox 1	MBOX1
350	Mailbox 2	MBOX2
354	Mailbox 3	MBOX3
358	Semaphore 0 Register	SEMA0
35C	Semaphore 1 Register	SEMA1
360-3FC	Universe reserved	
400	Master Control	MAST_CTL
404	Miscellaneous Control	MISC_CTL
408	Miscellaneous Status	MISC_STAT

Table 4.1 Universe II Register Map

Offset	Register	Name
40C	User AM Codes Register	USER_AM
410-EFC	Universe reserved	
F00	VMEbus Slave Image 0 Control	VSI0_CTL
F04	VMEbus Slave Image 0 Base Address Register	VSI0_BS
F08	VMEbus Slave Image 0 Bound Address Register	VSI0_BD
F0C	VMEbus Slave Image 0 Translation Offset	VSI0_TO
F10	Universe reserved	
F14	VMEbus Slave Image 1 Control	VSI1_CTL
F18	VMEbus Slave Image 1 Base Address Register	VSI1_BS
F1C	VMEbus Slave Image 1 Bound Address Register	VSI1_BD
F20	VMEbus Slave Image 1 Translation Offset	VSI1_TO
F24	Universe reserved	
F28	VMEbus Slave Image 2 Control	VSI2_CTL
F2C	VMEbus Slave Image 2 Base Address Register	VSI2_BS
F30	VMEbus Slave Image 2 Bound Address Register	VSI2_BD
F34	VMEbus Slave Image 2 Translation Offset	VSI2_TO
F38	Universe reserved	
F3C	VMEbus Slave Image 3 Control	VSI3_CTL
F40	VMEbus Slave Image 3 Base Address Register	VSI3_BS
F44	VMEbus Slave Image 3 Bound Address Register	VSI3_BD
F48	VMEbus Slave Image 3 Translation Offset	VSI3_TO
F4C-F60	Universe reserved	
F64	Location Monitor Control	LM_CTL
F68	Location Monitor Base Address Register	LM_BS
F6C	Universe reserved	
F70	VMEbus Register Access Image Control Register	VRAI_CTL
F74	VMEbus Register Access Image Base Address	VRAI_BS
F78-F7C	Universe reserved	
F80	VMEbus CSR Control Register	VCSR_CTL
F84	VMEbus CSR Translation Offset	VCSR_TO
F88	VMEbus AM Code Error Log	V_AMERR
F8C	VMEbus Address Error Log	VAERR
F90	VMEbus Slave Image 4 Control	VSI4_CTL
F94	VMEbus Slave Image 4 Base Address Register	VSI4_BS
F98	VMEbus Slave Image 4 Bound Address Register	VSI4_BD
F9C	VMEbus Slave Image 4 Translation Offset	VSI4_TO
FA0	Universe reserved	
FA4	VMEbus Slave Image 5 Control	VSI5_CTL
FA8	VMEbus Slave Image 5 Base Address Register	VSI5_BS

Table 4.1 Universe II Register Map

Offset	Register	Name
FAC	VMEbus Slave Image 5 Bound Address Register	VSI5_BD
FB0	VMEbus Slave Image 5 Translation Offset	VSI5_TO
FB4	Universe reserved	
FB8	VMEbus Slave Image 6 Control	VSI6_CTL
FBC	VMEbus Slave Image 6 Base Address Register	VSI6_BS
FC0	VMEbus Slave Image 6 Bound Address Register	VSI6_BD
FC4	VMEbus Slave Image 6 Translation Offset	VSI6_TO
FC8	Universe reserved	
FCC	VMEbus Slave Image 7 Control	VSI7_CTL
FD0	VMEbus Slave Image 7 Base Address Register	VSI7_BS
FD4	VMEbus Slave Image 7 Bound Address Register	VSI7_BD
FD8	VMEbus Slave Image 7 Translation Offset	VSI7_TO
FDC-FEC	Universe reserved	
FF0	VME CR/CSR Reserved	
FF4	VMEbus CSR Bit Clear Register	VCSR_CLR
FF8	VMEbus CSR Bit Set Register	VCSR_SET
FFC	VMEbus CSR Base Address Register	VCSR_BS

PCI Configuration Miscellaneous 0 Register (PCI_MISC0)

Register Name: PCI_MISC0	Offset:00C

Bits	Function						
31-24	BISTC	SBIST	PCI Reserved		CCODE		
23-16	MFUNCT	LAYOUT					
15-08	LTIMER				0	0	0
07-00	PCI Unimplemented						

PCI_MISC0 Description

Name	Type	Reset By	Reset State	Function
BISTC	R	all	0	BIST Capable
SBIST	R	all	0	Start BIST The Universe is not BIST capable
CCODE	R	all	0	Completion Code The Universe is not BIST capable
MFUNCT	R	all	0	Multifunction Device 0=No, 1=Yes This field is now set to 0. The Universe II ignores the address lines AD[10:8] during Type 0 configuration access.
LAYOUT	R	all	0	Configuration Space Layout
LTIMER [7:3]	R/W	all	0	Latency Timer: The latency timer has a resolution of 8 clocks

PCI Configuration Class Register

Register Name: PCI_CLASS	Offset:008

Bits	Function
31-24	BASE
23-16	SUB
15-08	PROG
07-00	RID

PCI_CLASS Description

Name	Type	Reset By	Reset State	Function
BASE[7..0]	R		06	Base Class Code
SUB[7..0]	R		80	Sub Class Code
PROG[7..0]	R		0	Programming Interface
RID[7..0]	R		01	Revision ID

The revision id has been changed to one.

PCI Configuration Base Address Register

Register Name: PCI_BS	Offset:010

Bits	Function							
31-24	BS							
23-16	BS							
15-08	BS				0	0	0	0
07-00	0	0	0	0	0	0	0	SPACE

PCI_BS Description

Name	Type	Reset By	Reset State	Function
SPACE	R		Power-up Option	Local bus Address Space 0=Memory, 1=I/O
BS[31..12]	R/W		0	Base Address

This register specifies the 4Kbyte aligned base address of the 4Kbyte Universe register space on PCI.

A power-up option determines if the registers are mapped into Memory or I/O space. If mapped into Memory space, the user is free to locate the registers anywhere in the 32-bit address space. The registers are not prefetchable.

A write must occur to this register before the Universe register space can be accessed through this mechanism. This write can be performed with a PCI configuration transaction or a VMEbus register access.

PCI Configuration Base Address Register1

Register Name: PCI_BS1	Offset:014

Bits	Function							
31-24	BS							
23-16	BS							
15-08	BS				0	0	0	0
07-00	0	0	0	0	0	0	0	SPACE

PCI_BS1 Description

Name	Type	Reset By	Reset State	Function
SPACE	R		Power-up Option	Local bus Address Space 0=Memory, 1=I/O
BS[31..12]	R/W		0	Base Address

This register specifies the 4Kbyte aligned base address of the Universe register space on PCI.

A power-up option determines if the registers are mapped into Memory or I/O space. PCI_BS1 is mapped into the opposite space of PCI_BS. For example, if PCI_BS is mapped into Memory space, PCI_BS1 is mapped into I/O space.

A write must occur to this register before the Universe register space can be accessed through this mechanism. This write can be performed with a PCI configuration transaction or a VMEbus register access.

Special Cycle Control Register (SCYC_CTL)

Register Name: SCYC_CTL	Offset: 170

Bits	Function		
31-24	Universe Reserved		
23-16	Universe Reserved		
15-08	Universe Reserved		
07-00	Universe Reserved	LAS	SCYC

SCYC_CTL Description

Name	Type	Reset By	Reset State	Function
LAS	R/W	all	0	PCI bus Memory Space 0=PCI bus Memory Space, 1=PCI bus I/O Space
SCYC	R/W	all	0	Special Cycle 00=Disable, 01=RMW, 10=LOCK, 11=Reserved

The special cycle generator will generate an LOCK or RMW cycle on VME when the 32-bit PCI bus address which matches the programmed address in SCYC_ADDR is accessed. A Read-Modify-Write command is initiated by a read to the specified address. Lock cycles are initiated by either read or write cycles.

PCI Miscellaneous Register (LMISC)

Register Name: LMISC	Offset: 184

Bits	Function		
31-24	CRT	Reserved	CWT
23-16	Universe Reserved		
15-08	Universe Reserved		
07-00	Universe Reserved		

LMISC Description

Name	Type	Reset By	Reset State	Function
CRT	R/W	all	0001	Coupled Request Timer This field no longer effects the function of the Universe device. It can still be written to and read from.
CWT	R/W	all	000	Coupled Window Timer 000=Disable - release after first coupled transaction, 001=16 PCI Clocks, 010=32 PCI Clocks, 011=64 PCI Clocks, 100=128 PCI Clocks, 101=256 PCI Clocks, 110=512 PCI Clocks, others=RESERVED

If a PCI master generates a coupled transaction and the PCI Slave Channel in the Universe is not currently the owner of the VMEbus, then the Universe retries the PCI master and requests VMEbus ownership. The Universe II will wait for 2^{15} PCI clock cycles for the initiating PCI master to return before relinquishing the VMEbus. The timer is restarted each time a PCI master attempts the coupled transaction.

The Universe uses the coupled window timer (CWT) to determine how long to hold ownership of the VMEbus on behalf of the PCI Slave Channel after processing a coupled transaction. The timer is restarted each time the Universe processes a coupled transaction. If this timer expires, then the PCI Slave Channel releases the VME Master Interface.

Device behaviour is unpredictable if the CWT is changed during coupled cycle activity. These registers should be set only at configuration time, or after disabling all PCI Slave Images.

Local Slave Image 4 Control (LSI4_CTL)

Register Name: LSI4_CTL	Register Offset:1A0

Bits	Function						
31-24	EN	PWEN	Universe Reserved				
23-16	VDW		Reserved			VAS	
15-08	Reserved	PGM	Reserved	SUPER	Universe Reserved		VCT
07-00	Universe Reserved						LAS

LSI4_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
VDW	R/W	all	10	VMEbus Maximum Datawidth 00=8 bit datawidth, 01=16 bit datawidth, 10=32 bit datawidth, 11=64 bit datawidth (MBLT)
VAS	R/W	all	0	VMEbus Address Space 000=A16, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=CR/CSR, 110=User1, 111=User2
PGM	R/W	all	0	VMEbus Program/Data AM Code 0=Data, 1=Program
SUPER	R/W	all	0	VMEbus Supervisor/User AM Code 0=Non-Privileged, 1=Supervisor
VCT	R/W	all	0	VMEbus Cycle Type 0=No BLT Transfers on VMEbus, 1=BLT Transfers on VMEbus if (VAS=A24 or VAS=A32) and (VDW=8 bits, or VDW=16 bits, or VDW=32 bits)
LAS	R/W	all	0	PCI bus Memory Space 0=PCI bus Memory Space, 1=PCI bus I/O Space

Local Slave Image 4 Base Address Register (LSI4_BS)

Register Name: LSI4_BS	Register Offset:1A4

Bits	Function	
31-24	BS	
23-16	BS	
15-08	BS	Universe Reserved
07-00	Universe Reserved	

LSI4_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:12]	R/W	VME and PWRST	0	Base Address

Local Slave Image 4 Bound Address Register (LSI4_BD)

Register Name: LSI4_BD	Register Offset:1A8

Bits	Function	
31-24	BD	
23-16	BD	
15-08	BD	Universe Reserved
07-00	Universe Reserved	

LSI4_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:12]	R/W	VME and PWRST	0	Bound Address

Local Slave Image 4 Translation Offset (LSI4_TO)

Register Name: LSI4_TO	Register Offset:1AC

Bits	Function	
31-24	TO	
23-16	TO	
15-08	TO	Universe Reserved
07-00	Universe Reserved	

LSI4_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:12]	R/W	VME and PWRST	0	Translation Offset

Local Slave Image 5 Control (LSI5_CTL)

Register Name: LSI5_CTL	Register Offset:1B4

Bits	Function					
31-24	EN	PWEN	Universe Reserved			
23-16	VDW		Universe Reserved		VAS	
15-08	Reserved	PGM	Reserved	SUPER	Universe Reserved	VCT
07-00	Universe Reserved					LAS

LSI5_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
VDW	R/W	all	10	VMEbus Maximum Datawidth 00=8 bit datawidth, 10=16 bit datawidth, 10=32 bit datawidth, 11=64 bit datawidth
VAS	R/W	all	0	VMEbus Address Space 000=A16, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=CR/CSR, 110=User1, 111=User2
PGM	R/W	all	0	Program/Data AM Code 0=Data, 1=Program
SUPER	R/W	all	0	Supervisor AM Code 0=Non-Privileged, 1=Priviledged
VCT	R/W	all	0	VMEbus Cycle Type 0=No BLT Transfers on VMEbus, 1= BLT Transfers on VMEbus (MBLT)
LAS	R/W	all	0	PCI bus Memory Space 0=PCI bus Memory space, 1=PCI bus I/O space

Local Slave Image 5 Base Address Register (LSI5_BS)

Register Name: LSI5_BS	Register Offset:1B8

Bits	Function
31-24	BS
23-16	BS
15-08	Universe Reserved
07-00	Universe Reserved

LSI5_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:16]	R/W	VME and PWRST	0	Base Address

Local Slave Image 5 Bound Address Register (LSI5_BD)

Register Name: LSI5_BD	Register Offset:1BC

Bits	Function
31-24	BD
23-16	BD
15-08	Universe Reserved
07-00	Universe Reserved

LSI5_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:16]	R/W	VME and PWRST	0	Bound Address

Local Slave Image 5 Translation Offset (LSI5_TO)

Register Name: LSI5_TO	Register Offset:1C0

Bits	Function
31-24	TO
23-16	TO
15-08	Universe Reserved
07-00	Universe Reserved

LSI5_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:16]	R/W	VME and PWRST	0	Translation Offset

Local Slave Image 6 Control (LSI6_CTL)

Register Name: LSI6_CTL	Register Offset:1C8

Bits	Function						
31-24	EN	PWEN	Universe Reserved				
23-16	VDW		Reserved			VAS	
15-08	Reserved	PGM	Reserved	SUPER	Universe Reserved		VCT
07-00	Universe Reserved						LAS

LSI6_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
VDW	R/W	all	10	VMEbus Maximum Datawidth 00=8 bit datawidth, 01=16 bit datawidth, 10=32 bit datawidth, 11=64 bit datawidth
VAS	R/W	all	0	VMEbus Address Space 000=A16, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=CR/CSR, 110=User1, 111=User2
PGM	R/W	all	0	Program/Data AM Code 0=Data, 1=Program
SUPER	R/W	all	0	Supervisor AM Code 0=Non-Privileged, 1=Priviledged
VCT	R/W	all	0	VMEbus Cycle Type 0=No BLT Transfers on VMEbus, 1= BLT Transfers on VMEbus (MBLT)
LAS	R/W	all	0	PCI bus Memory Space 0=PCI bus Memory space, 1=PCI bus I/O space

Local Slave Image 6 Base Address Register (LSI6_BS)

Register Name: LSI6_BS	Register Offset:1CC

Bits	Function
31-24	BS
23-16	BS
15-08	Universe Reserved
07-00	Universe Reserved

LSI6_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:16]	R/W	VME and PWRST	0	Base Address

Local Slave Image 6 Bound Address Register (LSI6_BD)

Register Name: LSI6_BD	Register Offset:1D0

Bits	Function
31-24	BD
23-16	BD
15-08	Universe Reserved
07-00	Universe Reserved

LSI6_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:16]	R/W	VME and PWRST	0	Bound Address

Local Slave Image 6 Translation Offset (LSI6_TO)

Register Name: LSI6_TO	Register Offset:1D4

Bits	Function
31-24	TO
23-16	TO
15-08	Universe Reserved
07-00	Universe Reserved

LSI6_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:16]	R/W	VME and PWRST	0	Translation Offset

Local Slave Image 7 Control (LSI7_CTL)

Register Name: LSI7_CTL	Register Offset:1DC

Bits	Function					
31-24	EN	PWEN	Universe Reserved			
23-16	VDW		Reserved		VAS	
15-08	Reserved	PGM	Reserved	SUPER	Universe Reserved	VCT
07-00	Universe Reserved					LAS

LSI7_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
VDW	R/W	all	10	VMEbus Maximum Datawidth 00=8 bit datawidth, 01=16 bit datawidth, 10=32 bit datawidth, 11=64 bit datawidth
VAS	R/W	all	0	VMEbus Address Space 000=A16, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=CR/CSR, 110=User1, 111=User2
PGM	R/W	all	0	Program/Data AM Code 0=Data, 1=Program
SUPER	R/W	all	0	Supervisor AM Code 0=Non-Privileged, 1=Priviledged
VCT	R/W	all	0	VMEbus Cycle Type 0=No BLT Transfers on VMEbus, 1= BLT Transfers on VMEbus (MBLT)
LAS	R/W	all	0	PCI bus Memory Space 0=PCI bus Memory space, 1=PCI bus I/O space

Local Slave Image 7 Base Address Register (LSI7_BS)

Register Name: LSI7_BS	Register Offset:1E0

Bits	Function
31-24	BS
23-16	BS
15-08	Universe Reserved
07-00	Universe Reserved

LSI7_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:16]	R/W	VME and PWRST	0	Base Address

Local Slave Image 7 Bound Address Register (LSI7_BD)

Register Name: LSI7_BD	Register Offset:1E4

Bits	Function
31-24	BD
23-16	BD
15-08	Universe Reserved
07-00	Universe Reserved

LSI7_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:16]	R/W	VME and PWRST	0	Bound Address

Local Slave Image 7 Translation Offset (LSI7_TO)

Register Name: LSI7_TO	Register Offset:1E8

Bits	Function
31-24	TO
23-16	TO
15-08	Universe Reserved
07-00	Universe Reserved

LSI7_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:16]	R/W	VME and PWRST	0	Translation Offset

DMA General Control / Status Register

Register Name: DGCS	Register Offset:220

Bits	Function							
31-24	GO	STOP_REQ	HALT_REQ	0	CHAIN	0	0	0
23-16	Reserved	VON			VOFF			
15-08	ACT	STOP	HALT	0	DONE	LERR	VERR	P_ERR
07-00	0	INT_STOP	INT_HALT	0	INT_DONE	INT_LERR	INT_VERR	INT_ME_ERR

DMA_GCSR Description

Name	Type	Reset By	Reset State	Function
GO	W/Read 0 always		0	DMA Go Bit 0=No effect, 1=Enable DMA Transfers
STOP_REQ	W/Read 0 always		0	DMA Stop Request 0=No effect, 1=Stop the DMA transfer when all buffered data has been written
HALT_REQ	W/Read o always		0	DMA Halt Request 0=No effect, 1=Halt the DMA transfer at the completion of the current command packet.
CHAIN	R/W		0	DMA Chaining 0=DMA Direct Mode, 1=DMA Command Chaining Mode
VON [2:0]	R/W		0	VMEbus Aligned DMA Transfer Count 000=Until done, 001=256 bytes, 010=512 bytes, 011=1024 bytes, 100=2048 bytes, 101=4096 bytes, 110=8192 bytes, 111=16384 bytes. The DMA will release the VME master when the programmed alignment is reached.
VOFF [3:0]	R/W		0	VMEbus DMA Off Timer 0000=0 µsec, 0001=16 µsec, 0010=32 µsec, 0011=64 µsec, 0100=128 µsec, 0101=256 µsec, 0110=512 µsec, 0111=1024 µsec, 1000=2 µsec, 1001=4 µsec, 1010=8 µsec, others=Reserved. The DMA will not re-request the VME master until this timer expires.
ACT	R		0	DMA Active Flag 0=Not Active, 1=Active
STOP	R/Write 1 to clear		0	DMA Stopped Flag 0=Not Stopped, 1=Stopped
HALT	R/Write 1 to clear		0	DMA Halted Flag 0=Not halted, 1=Halted
DONE	R/Write 1 to clear		0	All DMA Transfers Complete 0=Not Complete, 1=Complete
LERR	R/Write 1 to clear		0	DMA PCI Bus Error 0=No Error, 1=Error
VERR	R/Write 1 to clear		0	DMA VMEbus Error 0=No Error, 1=Error

DMA_GCSR Description (Continued)

Name	Type	Reset By	Reset State	Function
P_ERR	R/Write 1 to clear		0	Protocol Error Asserted if PCI master disabled or lower three bits of local and VME addresses differ. 0=No Error, 1=Error
INT_STOP	R/W		0	Interrupt when Stopped 0=Disable, 1=Enable
INT_HALT	R/W		0	Interrupt when Halted 0=Disable, 1=Enable
INT_DONE	R/W		0	Interrupt when Done 0=Disable, 1=Enable
INT_LERR	R/W		0	Interrupt on LERR 0=Disable, 1=Enable
INT_VERR	R/W		0	Interrupt on VERR 0=Disable, 1=Enable
INT_ME_ERR	R/W		0	Interrupt on Master Enable Error 0=Disable, 1=Enable

Additional settings for VOFF have been added.
VOFF bit function description has been changed.
VON [3] is reserved.

Local Interrupt Enable Register

Register Name: LINT_EN	Offset: 300

Bits	Function							
31-24	UNIVERSE RESERVED							
23-16	LM3	LM2	LM1	LM0	MBOX3	MBOX2	MBOX1	MBOX0
15-08	ACFAIL	SYSFAIL	LCL_ SW_INT	VME_ SW_IACK		LCL_ VERR	LCL_ LERR	LCL_ DMA
07-00	VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	VOWN

LINT_EN Description

Name	Type	Reset By	Reset State	Function
LM3	R/W		0	Location Monitor 3 Mask 0 : LM3 Interrupt masked 1 : LM3 Interrupt enabled
LM2	R/W		0	Location Monitor 2 Mask 0 : LM2 Interrupt masked 1 : LM2 Interrupt enabled
LM1	R/W		0	Location Monitor 1 Mask 0 : LM1 Interrupt masked 1 : LM1 Interrupt enabled
LM0	R/W		0	Location Monitor 0 Mask 0 : LM0 Interrupt masked 1 : LM0 Interrupt enabled
MBOX3	R/W		0	Mailbox 3 Mask 0 : MBOX3 Interrupt masked 1 : MBOX3 Interrupt enabled
MBOX2	R/W		0	Mailbox 2 Mask 0 : MBOX2 Interrupt masked 1 : MBOX2 Interrupt enabled
MBOX1	R/W		0	Mailbox 1 Mask 0 : MBOX1 Interrupt masked 1 : MBOX1 Interrupt enabled
MBOX0	R/W		0	Mailbox 0 Mask 0 : MBOX0 Interrupt masked 1 : MBOX0 Interrupt enabled

LINT_EN Description

ACFAIL	R/W	all	0	ACFail Interrupt Mask 0 : ACFail Interrupt masked 1 : ACFail Interrupt enabled
SYS-FAIL	R/W	all	0	SysFail Interrupt Mask 0 : SysFail Interrupt masked 1 : SysFail Interrupt enabled
LCL_ SW_INT	R/W	all	0	Local Software Interrupt Mask 0 : Local Software Interrupt masked 1 : Local Software Interrupt enabled A zero-to-one transition will cause the Local software interrupt to be asserted. Subsequent zeroing of this bit will cause the interrupt to be masked, but will not clear the LCL Software Interrupt Status bit.
VME_ SW_IACK	R/W	all	0	"VME Software IACK" Mask 0 : "VME Software IACK" Interrupt masked 1 : "VME Software IACK" Interrupt enabled
LCL_ VERR	R/W	all	0	Local VErr Interrupt Mask 0 : Local VErr Interrupt masked 1 : Local VErr Interrupt enabled
LCL_ LERR	R/W	all	0	Local LErr Interrupt Mask 0 : Local LErr Interrupt masked 1 : Local LErr Interrupt enabled
LCL_ DMA	R/W	all	0	Local DMA Interrupt Mask 0 : Local DMA Interrupt masked 1 : Local DMA Interrupt enabled
VIRQ7-VIRQ1	R/W	all	0	VIRQ*x* Interrupt Mask 0 : VIRQ*x* Interrupt masked 1 : VIRQ*x* Interrupt enabled
VOWN	R/W	all	0	VOwn Interrupt Mask 0: VOwn Interrupt masked 1: VOwn Interrupt Enabled

Location monitor and mailbox local interrupt enables have been added.

Local Interrupt Status Register

Register Name: LINT_STAT	Offset: 304

Bits	Function							
31-24	Universe Reserved							
23-16	LM3	LM2	LM1	LM0	MBOX3	MBOX2	MBOX1	MBOX0
15-08	ACFAIL	SYSFAIL	LCL_ SW_INT	VME_ SW_IACK	Reserved	LCL_ VERR	LCL_ LERR	LCL_ DMA
07-00	VIRQ7	VIRQ6	VIRQ5	VIRQ4	VIRQ3	VIRQ2	VIRQ1	VOWN

LINT_STAT Description

Name	Type	Reset By	Reset State	Function
LM3	R/Write 1 to Clear	all	0	Location Monitor 3 Status/Clear 0 : no Location Monitor 3 Interrupt 1 : Location Monitor 3 Interrupt active
LM2	R/Write 1 to Clear	all	0	Location Monitor 2 Status/Clear 0 : no Location Monitor 2 Interrupt 1 : Location Monitor 2 Interrupt active
LM1	R/Write 1 to Clear	all	0	Location Monitor 1 Status/Clear 0 : no Location Monitor 1 Interrupt 1 : Location Monitor 1 Interrupt active
LM0	R/Write 1 to Clear	all	0	Location Monitor 0 Status/Clear 0 : no Location Monitor 0 Interrupt 1 : Location Monitor 0 Interrupt active
MBOX3	R/Write 1 to Clear	all	0	Mailbox 3 Status/Clear 0 : no Mailbox 3 Interrupt 1 : Mailbox 3 Interrupt active
MBOX2	R/Write 1 to Clear	all	0	Mailbox 2 Status/Clear 0 : no Mailbox 2 Interrupt 1 : Mailbox 2 Interrupt active
MBOX1	R/Write 1 to Clear	all	0	Mailbox 1 Status/Clear 0 : no Mailbox 1 Interrupt 1 : Mailbox 1 Interrupt active
MBOX0	R/Write 1 to Clear	all	0	Mailbox 0 Status/Clear 0 : no Mailbox 0 Interrupt 1 : Mailbox 0 Interrupt active

LINT_STAT Description

ACFAIL	RO	all	0	ACFail Interrupt Status/Clear 0 : no ACFAIL Interrupt 1 : ACFail Interrupt active
SYS-FAIL	RO	all	0	SysFail Interrupt Status/Clear 0 : no SYSFAIL Interrupt 1 : SysFail Interrupt active
LCL_ SW_INT	R/Write 1 to Clear	all	0	Local Software Interrupt Status/Clear 0 : no Local Software Interrupt 1 : Local Software Interrupt active
VME_ SW_IAC K	R/Write 1 to Clear	all	0	"VME Software IACK" Status/Clear 0 : no "VME Software IACK" Interrupt 1 : "VME Software IACK" Interrupt active
LCL_ VERR	R/Write 1 to Clear	all	0	Local VErr Interrupt Status/Clear 0 : no Local VERR Interrupt 1 : Local VErr Interrupt active
LCL_ LERR	R/Write 1 to Clear	all	0	Local LErr Interrupt Status/Clear 0 : no Local LErr Interrupt 1 : Local LErr Interrupt active
LCL_ DMA	R/Write 1 to Clear	all	0	Local DMA Interrupt Status/Clear 0 : noLocal DMA Interrupt 1 : Local DMA Interrupt active
VIRQ7-VIRQ1	R/Write 1 to Clear	all	0	VIRQ*x* Interrupt Status/Clear 0 : no VIRQx Interrupt StatusID vector available 1 : VIRQ*x* Interrupt StatusID vector available
VOWN	R/Write 1 to Clear	all	0	VOwn Interrupt Status/Clear 0: no VOwn Interrupt active 1: VOwn Interrupt active

Location monitor and mailbox local interrupt status bits have been added. They are edge sensitive: the status is latched when the interrupt event occurs. These status bits can be cleared independently of the state of the interrupt source by writing a "1" to the status register. Clearing the status bit does not imply the source of the interrupt is cleared. The status bit will not be reasserted until the source of the interrupt is negated and reasserted.

VME Interrupt Enable Register

Register Name: VINT_EN	Offset: 310

Bits	Function							
31-24	VME_SW 7	VME_SW 6	VME_SW 5	VME_SW 4	VME_SW 3	VME_SW 2	VME_SW 1	Reserved
23-16	Universe Reserved				MBOX3	MBOX2	MBOX1	MBOX0
15-08	Universe Reserved			VME_ SW_INT	Reserved	VME_ VERR	VME_ LERR	VME_ DMA
07-00	LINT7	LINT6	LINT5	LINT4	LINT3	LINT2	LINT1	LINT0

VINT_EN Description

Name	Type	Reset By	Reset State	Function
VME_SW7	R/W	all	0	VME Software 7 Interrupt Mask 0 : VME Software 7 Interrupt masked 1 : VME Software 7 Interrupt enabled A zero-to-one transition will cause a VME level 7 interrupt to be generated..
VME_SW6	R/W	all	0	VME Software 6 Interrupt Mask 0 : VME Software 6 Interrupt masked 1 : VME Software 6 Interrupt enabled A zero-to-one transition will cause a VME level 6 interrupt to be generated.
VME_SW5	R/W	all	0	VME Software 5 Interrupt Mask 0 : VME Software 5 Interrupt masked 1 : VME Software 5 Interrupt enabled A zero-to-one transition will cause a VME level 5 interrupt to be generated.
VME_SW4	R/W	all	0	VME Software 4 Interrupt Mask 0 : VME Software 4 Interrupt masked 1 : VME Software 4 Interrupt enabled A zero-to-one transition will cause a VME level 4 interrupt to be generated.
VME_SW3	R/W	all	0	VME Software 3 Interrupt Mask 0 : VME Software 3 Interrupt masked 1 : VME Software 3 Interrupt enabled A zero-to-one transition will cause a VME level 3 interrupt to be generated.

VINT_EN Description

VME_SW2	R/W	all	0	VME Software 2 Interrupt Mask 0 : VME Software 2 Interrupt masked 1 : VME Software 2 Interrupt enabled A zero-to-one transition will cause a VME level 2 interrupt to be generated.
VME_SW1	R/W	all	0	VME Software 1 Interrupt Mask 0 : VME Software 1 Interrupt masked 1 : VME Software 1 Interrupt enabled A zero-to-one transition will cause a VME level 1 interrupt to be generated.
MBOX3	R/W	all	0	Mailbox 3 Mask 0 : MBOX3 Interrupt masked 1 : MBOX3 Interrupt enabled
MBOX2	R/W	all	0	Mailbox 2 Mask 0 : MBOX2 Interrupt masked 1 : MBOX2 Interrupt enabled
MBOX1	R/W	all	0	Mailbox 1 Mask 0 : MBOX1 Interrupt masked 1 : MBOX1 Interrupt enabled
MBOX0	R/W	all	0	Mailbox 0 Mask 0 : MBOX0 Interrupt masked 1 : MBOX0 Interrupt enabled
VME_SW_INT	R/W	all	Power-up Option	VME Software Interrupt Mask 0 : VME Software Interrupt masked 1 : VME Software Interrupt enabled A zero-to-one transition will cause the VME software interrupt to be asserted. Subsequent zeroing of this bit will cause the interrupt to be masked, but will not clear the VME Software Interrupt Status bit.
VME_VERR	R/W	all	0	VME VErr Interrupt Mask 0 : VME VErr Interrupt masked 1 : VME VErr Interrupt enabled
VME_LERR	R/W	all	0	VME LErr Interrupt Mask 0 : VME LErr Interrupt masked 1 : VME LErr Interrupt enabled
VME_DMA	R/W	all	0	VME DMA Interrupt Mask 0 : VME DMA Interrupt masked 1 : VME DMA Interrupt enabled
LINT7 - LINT0	R/W	all	0	LINTx Interrupt Mask 0 : LInt*x* Interrupt masked 1 : LInt*x* Interrupt enabled

Seven new VMEbus software interrupt and mailbox interrupt enables have been added.

VME Interrupt Status Register

Register Name: VINT_STAT	Offset: 314

Bits	Function							
31-24	VME_SW 7	VME_SW 6	VME_SW 5	VME_SW 4	VME_SW 3	VME_SW 2	VME_SW 1	Reserved
23-16	Universe Reserved				MBOX3	MBOX2	MBOX1	MBOX0
15-08	Universe Reserved			VME_ SW_INT		VME_ VERR	VME_ LERR	VME_ DMA
07-00	LINT7	LINT6	LINT5	LINT4	LINT3	LINT2	LINT1	LINT0

VINT_STAT Description

Name	Type	Reset By	Reset State	Function
VME_SW7	R/Write 1 to Clear	all	0	VME Software 7 Interrupt Status/Clear 0 : no VME Software 7 Interrupt 1 : VME Software 7 Interrupt active
VME_SW6	R/Write 1 to Clear	all	0	VME Software 6 Interrupt Status/Clear 0 : no VME Software 6 Interrupt 1 : VME Software 6 Interrupt active
VME_SW5	R/Write 1 to Clear	all	0	VME Software 5 Interrupt Status/Clear 0 : no VME Software 5 Interrupt 1 : VME Software 5 Interrupt active
VME_SW4	R/Write 1 to Clear	all	0	VME Software 4 Interrupt Status/Clear 0 : no VME Software 4 Interrupt 1 : VME Software 4 Interrupt active
VME_SW3	R/Write 1 to Clear	all	0	VME Software 3 Interrupt Status/Clear 0 : no VME Software 3 Interrupt 1 : VME Software 3 Interrupt active
VME_SW2	R/Write 1 to Clear	all	0	VME Software 2 Interrupt Status/Clear 0 : no VME Software 2 Interrupt 1 : VME Software 2 Interrupt active
VME_SW1	R/Write 1 to Clear	all	0	VME Software 1 Interrupt Status/Clear 0 : no VME Software 1 Interrupt 1 : VME Software 1 Interrupt active
MBOX3	R/Write 1 to Clear	all	0	Mailbox 3 Status/Clear 0 : no Mailbox 3 Interrupt 1 : Mailbox 3 Interrupt active

VINT_STAT Description

MBOX2	R/Write 1 to Clear	all	0	Mailbox 2 Status/Clear 0 : no Mailbox 2 Interrupt 1 : Mailbox 2 Interrupt active
MBOX1	R/Write 1 to Clear	all	0	Mailbox 1 Status/Clear 0 : no Mailbox 1 Interrupt 1 : Mailbox 1 Interrupt active
MBOX0	R/Write 1 to Clear	all	0	Mailbox 0 Status/Clear 0 : no Mailbox 0 Interrupt 1 : Mailbox 0 Interrupt active
VME_ SW_INT	R/Write 1 to Clear	all	Pow-er-up Option	VME Software Interrupt Status/Clear 0 : no VME Software Interrupt 1 : VME Software Interrupt active
VME_ VERR	R/Write 1 to Clear	all	0	VME VErr Interrupt Status/Clear 0 : no VME VErr Interrupt 1 : VME VErr Interrupt active
VME_ LERR	R/Write 1 to Clear	all	0	VME LErr Interrupt Status/Clear 0 : no VME LErr Interrupt 1 : VME LErr Interrupt active
VME_ DMA	R/Write 1 to Clear	all	0	VME DMA Interrupt Status/Clear 0 : no VME DMA Interrupt 1 : VME DMA Interrupt active
LINT7 - LINT0	RO	all	0	LINTx Interrupt Status/Clear 0 : no LInt*x* Interrupt 1 : LInt*x* Interrupt active

Seven new VMEbus software interrupt and mailbox interrupt status bits have been added.

Local Interrupt Map 2 Register

Register Name: LINT_MAP2	Offset: 340

Bits	Function			
31-24	Reserved	LM3	Reserved	LM2
23-16	Reserved	LM1	Reserved	LM0
15-08	Reserved	MBOX3	Reserved	MBOX2
07-00	Reserved	MBOX1	Reserved	MBOX0

LINT_MAP2 Description

Name	Type	Reset By	Reset State	Function
LM3	R/W	all	0	Location Monitor 3 interrupt destination
LM2	R/W	all	0	Location Monitor 2 interrupt destination
LM1	R/W	all	0	Location Monitor 1 interrupt destination
LM0	R/W	all	0	Location Monitor 0 interrupt destination
MBOX3	R/W	all	0	Mailbox 3 interrupt destination
MBOX2	R/W	all	0	Mailbox 2 interrupt destination
MBOX1	R/W	all	0	Mailbox 1 interrupt destination
MBOX0	R/W	all	0	Mailbox 0 interrupt destination

Location monitor and mailbox mappings have been added. A value of 0b000 maps the corresponding interrupt source to LINT[0], a value of 0b001 maps to LINT[1], etc.

VME Interrupt Map 2 Register

Register Name: VINT_MAP2	Offset: 344

Bits	Function			
31-24	Reserved			
23-16	Reserved		Reserved	
15-08	Reserved	MBOX3	Reserved	MBOX2
07-00	Reserved	MBOX1	Reserved	MBOX0

VINT_MAP2 Description

Name	Type	Reset By	Reset State	Function
MBOX3	R/W	all	0	VIRQ Mapping
MBOX2	R/W	all	0	VIRQ Mapping
MBOX1	R/W	all	0	VIRQ Mapping
MBOX0	R/W	all	0	VIRQ Mapping

Mailbox mappings have been added. A value of 0b001 maps the corresponding interrupt source to VIRQ1, a value of 0b010 maps to VIRQ2, etc. A value of 0b000 effectively masks the interrupt since there is no corresponding VIRQ0 pin.

Mailbox 0

Register Name: MBOX0	Offset:348

Bits	Function
31-24	MBOX
23-16	MBOX
15-08	MBOX
07-00	MBOX

MBOX0 Description

Name	Type	Reset By	Reset State	Function
MBOX[31..0]	R/W	all	0	Mailbox

General purpose mailbox register. Writes to this register can cause interrupt generation on PCI or VMEbus.

Mailbox 1

Register Name: MBOX1	Offset:34C

Bits	Function
31-24	MBOX
23-16	MBOX
15-08	MBOX
07-00	MBOX

MBOX1 Description

Name	Type	Reset By	Reset State	Function
MBOX[31..0]	R/W	all	0	Mailbox

General purpose mailbox register. Writes to this register can cause interrupt generation on PCI or VMEbus.

Mailbox 2

Register Name: MBOX2	Offset:350

Bits	Function
31-24	MBOX
23-16	MBOX
15-08	MBOX
07-00	MBOX

MBOX2 Description

Name	Type	Reset By	Reset State	Function
MBOX[31..0]	R/W	all	0	Mailbox

General purpose mailbox register. Writes to this register can cause interrupt generation on PCI or VMEbus.

Mailbox 3

Register Name: MBOX3	Offset:354

Bits	Function
31-24	MBOX
23-16	MBOX
15-08	MBOX
07-00	MBOX

MBOX3 Description

Name	Type	Reset By	Reset State	Function
MBOX[31..0]	R/W	all	0	Mailbox

General purpose mailbox register. Writes to this register can cause interrupt generation on PCI or VMEbus.

Semaphore 0 Register

Register Name: SEMA0	Offset:358

Bits	Function	
31-24	SEM3	TAG3
23-16	SEM2	TAG2
15-08	SEM1	TAG1
07-00	SEM0	TAG0

SEMA Description

Name	Type	Reset By	Reset State	Function
SEM3	R/W	all	0	Semaphore 3
TAG3[6:0]	R/W	all	0	Tag3
SEM2	R/W	all	0	Semaphore 2
TAG2[6:0]	R/W	all	0	Tag2
SEM1	R/W	all	0	Semaphore 1
TAG1[6:0]	R/W	all	0	Tag1
SEM0	R/W	all	0	Semaphore 0
TAG0[6:0]	R/W	all	0	Tag0

This register provides support for four semaphores and associated tag data. If the current value of the semaphore field is a logic one, the value of the semaphore and the tag data can only be changed when a zero is written to the semaphore field.

Semaphore 1 Register

Register Name: SEMA1	Offset:35C

Bits	Function	
31-24	SEM7	TAG7
23-16	SEM6	TAG6
15-08	SEM5	TAG5
07-00	SEM4	TAG4

SEMA Description

Name	Type	Reset By	Reset State	Function
SEM7	R/W	all	0	Semaphore 7
TAG7[6:0]	R/W	all	0	Tag7
SEM6	R/W	all	0	Semaphore 6
TAG6[6:0]	R/W	all	0	Tag6
SEM5	R/W	all	0	Semaphore 5
TAG5[6:0]	R/W	all	0	Tag5
SEM4	R/W	all	0	Semaphore 4
TAG4[6:0]	R/W	all	0	Tag4

This register provides support for four semaphores and associated tag data. If the current value of the semaphore field is a logic one, the value of the semaphore and the tag data can only be changed when a zero is written to the semaphore field.

Master Control Register (MAST_CTL)

Register Name: MAST_CTL	Register Offset:400

Bits	Function					
31-24	MAXRTRY			PWON		
23-16	VRL	VRM	VREL	VOWN	VOWN_ACK	Reserved
15-08	Reserved	PABS		Reserved		
07-00	BUS_NO					

MAST_CTL Description

Name	Type	Reset By	Reset State	Function
MAXRTRY [3:0]	R/W	all	1000	Maximum Number of Retries 0000=Retry Forever, Multiples of 64 (0001 through 1111). Maximum number of retries before the PCI master interface signals error condition.
PWON [3:0]	R/W	all	0000	Posted Write Transfer Count 0000=128 bytes, 0001=256 bytes, 0010=512 bytes, 0011=1024 bytes, 0100=2048 bytes, 0101=4096 bytes, 1111=BBSY* release after each transaction, Others=Reserved. Transfer count at which the PCI Slave Channel Posted Writes FIFO gives up the VME Master Interface.
VRL [1:0]	R/W	all	11	VMEbus Request Level 00=Level 0, 01=Level 1, 10=Level2, 11=Level 3
VRM	R/W	all	0	VMEbus Request Mode 0=Demand, 1=Fair
VREL	R/W	all	0	VMEbus Release Mode 0=Release when Done, 1=Release on Request
VOWN	W	all	0	VME Ownership Bit 0=Release VMEbus, 1=Aquire and Hold VMEbus
VOWN_ACK	R	all	0	VME Ownership Bit Acknowledge 0=VMEbus not owned, 1=VMEbus acquired and held due to assertion of VOWN
PABS	R/W	all	00	PCI Aligned Burst Size 00=32 byte, 01=64 byte, 10=128 byte, Others=Reserved Controls the PCI address boundary at which the Universe breaks up a PCI transaction.
BUS_NO [7:0]	R/W	all	0000 0000	PCI Bus Number

VOWN_ACK is synchronized to the PCI clock.

VMEbus masters should not set the VOWN bit since this will lock up the VMEbus, until cleared by a PCI master.

The Universe II's PWON field has an additional setting ('1111') which will result in an early release of BBSY* at the completion of each transaction.

The Universe II's PABS field has an additional bit that allows for the new 128 byte setting.

Miscellaneous Control Register (MISC_CTL)

Register Name: MISC_CTL	Offset: 404

Bits	Function							
31-24	VBTO				Reserved	VARB	VARBTO	
23-16	SW_LRST	SW_SRST	Reserved	BI	ENGBI	RESCIND	SYSCON	V64AUTO
15-08	Universe Reserved							
07-00	Universe Reserved							

MISC_CTL Description

Name	Type	Reset By	Reset State	Function
VBTO	R/W	all	0011	VME Bus Time-out 0000=Disable, 0001=16 µsec, 0010=32 µsec, 0011=64 µsec, 0100=128 µsec, 0101=256 µsec, 0110=512 µsec, 0111=1024 µsec, others=RESERVED
VARB	R/W	all	0	VMEbus Arbitration Mode 0=Round Robin, 1=Priority
VARBTO	R/W	all	01	VMEbus Arbitration Time-out 00=Disable Timer, 01=16 µs, 10=256 µs, others=Reserved
SW_LRST	W	all	0	Software PCI Reset 0=No affect, 1=Initiate LRST# A read always returns 0.
SW_SYSRST	W	all	0	Software VMEbus SYSRESET 0=No affect, 1=Initiate SYSRST* A read always returns 0.
BI	R/W	all	Power-up Option	BI-Mode 0=Universe is not in BI-Mode, 1=Universe is in BI-Mode Write to this bit to change the Universe BI-Mode status. This bit is also affected by the global BI-Mode initiator VRIRQ1*, if this feature is enabled.
ENGBI	R/W	all	0	Enable Global BI-Mode Initiator 0=Assertion of VIRQ1 ignored, 1=Assertion of VIRQ1 puts device in BI-Mode
RESCIND	R/W	all	1	Rescinding DTACK Enable The Universe II ALWAYS rescinds DTACK.
SYSCON	R/W	all	Power-up Option	SYSCON 0=Universe is not VMEbus System Controller, 1=Universe is VMEbus System Controller
V64AUTO	R/W	all	Power-up Option	VME64 Auto ID Write: 0=No effect, 1=Initiate sequence This bit initiates Universe VME64 Auto ID Slave participation.

VMEbus masters should not write to SW_SYSRST, and PCI masters should not write to SW_LRST.

The bits VBTO, VARB and VARBTO support SYSCON functionality.

Universe participation in the VME64 Auto ID mechanism is controlled by the VME64AUTO bit. When this bit is detected high, the Universe uses the SW_IACK mechanism to generate VXIRQ2 on the VMEbus, then releases VXSYSFAIL. Access to the CR/CSR image is enabled when the level 2 interrupt acknowledge cycle completes. This sequence can be initiated with a power-up option or by software writing a 1 to this bit.

The RECIND bit can be written to and read from, however, its state no longer effects the operation of the Universe. DTACK is *always* rescinded by the Universe II.

Location Monitor Control

Register Name: LM_CTL	Offset:F64

Bits	Function			
31-24	EN	Universe Reserved		
23-16	PGM	SUPER		VAS
15-08	Universe Reserved			
07-00	Universe Reserved			

LM_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W		0	Image Enable 0=Disable, 1=Enable
PGM	R/W		11	Program/Data AM Code 00=Reserved, 01=Data, 10=Program, 11=Both
SUPER	R/W		11	Supervisor/User AM Code 00=Reserved, 01=Non-Privileged, 10=Supervisor, 11=Both
VAS	R/W		0	VMEbus Address Space 000=A16, 001=A24, 010=A32, 011= Reserved, 100=Reserved, 101=Reserved, 110=User1, 111=User2

This register specifies the VMEbus controls for the location monitor image. This image has a 4Kbyte resolution and a 4Kbyte size. The image responds to a VME read or write within the 4Kbyte space and matching one of the address modifier codes specified. Block transfers are not supported.

VMEbus address bits [4:3] are used to set the status bit in LINT_STAT for one of the four location monitor interrupts. If the onboard Universe master is the owner of the VMEbus, the Universe will also generate DTACK to terminate the transaction.

Location Monitor Base Address Register

Register Name: LM_BS	Offset:F68

Bits	Function	
31-24	BS	
23-16	BS	
15-08	BS	Universe Reserved
07-00	Universe Reserved	

LM_BS Description

Name	Type	Reset By	Reset State	Function
BS[31..12]	R/W	all	0	Base Address

The base address specifies the lowest address in the 4Kbyte range that will be decoded as a location monitor access.

VMEbus Slave Image 4 Control

Register Name: VSI4_CTL	Register Offset:F90

Bits	Function					
31-24	EN	PWEN	PREN	Reserved		
23-16	PGM		SUPER	Reserved	VAS	
15-08	Reserved					
07-00	LD64EN	LLRMW	Reserved			LAS

VSI4_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
PREN	R/W	all	0	Prefetched Read Enable 0=Disable, 1=Enable
PGM	R/W	all	11	Program/Data AM Code 00=Reserved, 01=Data, 10=Program, 11=Both
SUPER	R/W	all	11	Supervisor/User AM Code 00=Reserved, 01=Non-Privileged, 10=Supervisor, 11=Both
VAS	R/W	all	0	VMEbus Address Space 000=Reserved, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=Reserved, 110=User1, 111=User2
LD64EN	R/W	all	0	Enable 64-bit PCI bus Transactions 0=Disable, 1=Enable
LLRMW	R/W	all	0	Enable PCI bus lock of VMEbus RMW 0=disable, 1=Enable
LAS	R/W	all	0	PCI bus Address Space 00=PCI bus Memory Space, 01=PCI bus I/O Space, 10=PCI bus Configuration Space, 11=Reserved

VMEbus Slave Image 4 Base Address Register

Register Name: VSI4_BS	Register Offset:F94

Bits	Function	
31-24	BS	
23-16	BS	
15-08	BS	Universe Reserved
07-00	Universe Reserved	

VSI4_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:12]	R/W	VME and PWRST	0	Base Address

The base address specifies the lowest address in the address range that will be decoded.

VMEbus Slave Image 4 Bound Address Register

Register Name: VSI4_BD	Register Offset:F98

Bits	Function	
31-24	BD	
23-16	BD	
15-08	BD	Universe Reserved
07-00	Universe Reserved	

VSI4_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:12]	R/W	VME and PWRST	0	Bound Address

The addresses decoded in a slave image are those which are greater than or equal to the base address and less than the bound register. If the bound register is 0, then the addresses decoded are those greater than or equal to the base address.

VMEbus Slave Image 4 Translation Offset

Register Name: VSI4_TO	Register Offset:F9C

Bits	Function	
31-24	TO	
23-16	TO	
15-08	TO	Universe Reserved
07-00	Universe Reserved	

VSI4_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:12]	R/W	VME and PWRST	0	Translation Offset

The translation offset is added to the source address that is decoded and this new address becomes the destination address. If a negative offset is desired, the offset must be expressed as a two's complement.

VMEbus Slave Image 5 Control

Register Name: VSI5_CTL	Register Offset:FA4

Bits	Function					
31-24	EN	PWEN	PREN	Reserved		
23-16	PGM		SUPER	Reserved	VAS	
15-08	Universe Reserved					
07-00	LD64EN	LLRMW	Universe Reserved			LAS

VSI5_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
PREN	R/W	all	0	Prefetch Read Enable 0=Disable, 1Enable
PGM	R/W	all	11	Program/Data AM Code 00=Reserved, 01=Data, 10=Program, 11=Both
SUPER	R/W	all	11	Supervisor/User AM Code 00=Reserved, 01=Non-Privileged, 10=Supervisor, 11=Both
VAS	R/W	all	0	VMEbus Address Space 000=Reserved, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=Reserved, 110=User1, 111=User2
LD64EN	R/W	all	0	Enable 64-bit PCI bus Transactions 0=Disable, 1=Enable
LLRMW	R/W	all	0	Enable PCI bus lock of VMEbus RMW 0=disable, 1=Enable
LAS	R/W	all	0	PCI bus Address Space 00=PCI bus Memory Space, 01=PCI bus I/O Space, 10=PCI bus Configuration Space, 11=Reserved

VMEbus Slave Image 5 Base Address Register

Register Name: VSI5_BS	Register Offset:FA8

Bits	Function
31-24	BS
23-16	BS
15-08	Universe Reserved
07-00	Universe Reserved

VSI5_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:16]	R/W	VME and PWRST	0	Base Address

The base address specifies the lowest address in the address range that will be decoded.

VMEbus Slave Image 5 Bound Address Register

Register Name: VSI5_BD	Register Offset:FAC

Bits	Function
31-24	BD
23-16	BD
15-08	Universe Reserved
07-00	Universe Reserved

VSI5_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:16]	R/W	VME and PWRST	0	Bound Address

The addresses decoded in a slave image are those which are greater than or equal to the base address and less than the bound register. If the bound register is 0, then the addresses decoded are those greater than or equal to the base address.

VMEbus Slave Image 5 Translation Offset

Register Name: VSI5_TO	Register Offset:FB0

Bits	Function
31-24	TO
23-16	TO
15-08	Universe Reserved
07-00	Universe Reserved

VSI5_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:16]	R/W	VME and PWRST	0	Translation Offset

The translation offset is added to the source address that is decoded and this new address becomes the destination address. If a negative offset is desired, the offset must be expressed as a two's complement.

VMEbus Slave Image 6 Control

Register Name: VSI6_CTL	Register Offset:FB8

Bits	Function					
31-24	EN	PWEN	PREN	Universe Reserved		
23-16	PGM		SUPER	Reserved	VAS	
15-08	Universe Reserved					
07-00	LD64EN	LLRMW	Universe Reserved			LAS

VSI6_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
PREN	R/W	all	0	Prefetch Read Enable 0=Disable, 1=Enable
PGM	R/W	all	11	Program/Data AM Code 00=Reserved, 01=Data, 10=Program, 11=Both
SUPER	R/W	all	11	Supervisor/User AM Code 00=Reserved, 01=Non-Privileged, 10=Supervisor, 11=Both
VAS	R/W	all	0	VMEbus Address Space 000=Reserved, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=Reserved, 110=User1, 111=User2
LD64EN	R/W	all	0	Enable 64-bit PCI bus Transactions 0=Disable, 1=Enable
LLRMW	R/W	all	0	Enable PCI bus lock of VMEbus RMW 0=disable, 1=Enable
LAS	R/W	all	0	PCI bus Address Space 00=PCI bus Memory Space, 01=PCI bus I/O Space, 10=PCI bus Configuration Space, 11=Reserved

VMEbus Slave Image 6 Base Address Register

Register Name: VSI6_BS	Register Offset:FBC

Bits	Function
31-24	BS
23-16	BS
15-08	Universe Reserved
07-00	Universe Reserved

VSI6_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:16]	R/W	VME and PWRST	0	Base Address

The base address specifies the lowest address in the address range that will be decoded.

VMEbus Slave Image 6 Bound Address Register

Register Name: VSI6_BD	Register Offset:FC0

Bits	Function
31-24	BD
23-16	BD
15-08	Universe Reserved
07-00	Universe Reserved

VSI6_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:16]	R/W	VME and PWRST	0	Bound Address

The addresses decoded in a slave image are those which are greater than or equal to the base address and less than the bound register. If the bound register is 0, then the addresses decoded are those greater than or equal to the base address.

VMEbus Slave Image 6 Translation Offset

Register Name: VSI6_TO	Register Offset:FC4

Bits	Function
31-24	TO
23-16	TO
15-08	Universe Reserved
07-00	Universe Reserved

VSI6_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:16]	R/W	VME and PWRST	0	Translation Offset

The translation offset is added to the source address that is decoded and this new address becomes the destination address. If a negative offset is desired, the offset must be expressed as a two's complement.

VMEbus Slave Image 7 Control

Register Name: VSI7_CTL	Register Offset:FCC

Bits	Function					
31-24	EN	PWEN	PREN	Reserved		
23-16	PGM		SUPER	Reserved	VAS	
15-08	Universe Reserved					
07-00	LD64EN	LLRMW	Universe Reserved			LAS

VSI7_CTL Description

Name	Type	Reset By	Reset State	Function
EN	R/W	all	0	Image Enable 0=Disable, 1=Enable
PWEN	R/W	all	0	Posted Write Enable 0=Disable, 1=Enable
PREN	R/W	all	0	Prefetch Read Enable 0=Disable, 1=Enable
PGM	R/W	all	11	Program/Data AM Code 00=Reserved, 01=Data, 10=Program, 11=Both
SUPER	R/W	all	11	Supervisor/User AM Code 00=Reserved, 01=Non-Privileged, 10=Supervisor, 11=Both
VAS	R/W	all	0	VMEbus Address Space 000=Reserved, 001=A24, 010=A32, 011=Reserved, 100=Reserved, 101=Reserved, 110=User1, 111=User2
LD64EN	R/W	all	0	Enable 64-bit PCI bus Transactions 0=Disable, 1=Enable
LLRMW	R/W	all	0	Enable PCI bus lock of VMEbus RMW 0=disable, 1=Enable
LAS	R/W	all	0	PCI bus Address Space 00=PCI bus Memory Space, 01=PCI bus I/O Space, 10=PCI bus Configuration Space, 11=Reserved

VMEbus Slave Image 7 Base Address Register

Register Name: VSI7_BS	Register Offset:FD0

Bits	Function
31-24	BS
23-16	BS
15-08	Universe Reserved
07-00	Universe Reserved

VSI7_BS Description

Name	Type	Reset By	Reset State	Function
BS [31:16]	R/W	VME and PWRST	0	Base Address

The base address specifies the lowest address in the address range that will be decoded.

VMEbus Slave Image 7 Bound Address Register

Register Name: VSI7_BD	Register Offset:FD4

Bits	Function
31-24	BD
23-16	BD
15-08	Universe Reserved
07-00	Universe Reserved

VSI7_BD Description

Name	Type	Reset By	Reset State	Function
BD [31:16]	R/W	VME and PWRST	0	Bound Address

The addresses decoded in a slave image are those which are greater than or equal to the base address and less than the bound register. If the bound register is 0, then the addresses decoded are those greater than or equal to the base address.

VMEbus Slave Image 7 Translation Offset

Register Name: VSI7_TO	Register Offset:FD8

Bits	Function
31-24	TO
23-16	TO
15-08	Universe Reserved
07-00	Universe Reserved

VSI7_TO Description

Name	Type	Reset By	Reset State	Function
TO [31:16]	R/W	VME and PWRST	0	Translation Offset

The translation offset is added to the source address that is decoded and this new address becomes the destination address. If a negative offset is desired, the offset must be expressed as a two's complement.