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Front-End Signals from CHER to SUNNY

1) ABORTP: (pulse true low, two link clocks wide, can be generated anytime while link is ready) There is
also a pulse at powerup or manual reset time.) This signal is used by the ASIC boards to reset after an event
abort, and also used to reset state machines used to strobe ASIC's (no reply needed)

2) EOFEVNT: (level-true low) End of Event signal to all three ASIC boards. Reset by FE_CLR.

3) M1D[19:0]: Data lines to first ASIC board (true high)
M2D[19:0]: Data lines to second ASIC board
M3D[19:0]: Data lines to third ASIC board

4) M1A[3:1]: Three strobe signals for first ASIC board (true high)
M2A[3:1]: Three strobe signals for second ASIC board
M3A[3:1]: Three strobe signals for third ASIC board

5) PEDCLK: A strobe pulse sent to all three ASIC boards so header data byte 16 can be used (true high)
by the SVT boards to store a 'SCA offset count'. A local switch presents the same
data on both halves of the 20 bit word.

6) FLT_IRQ: (level-true low) Signal used to inform the processors on the ASIC boards of a Fault condition.
All three processors should acknowledge this condition before the fault latches are reset by
FE_CLR. This is an "OR" of (busyerr, headerbad, linkerr, watchdogtimer) Currently abort also
will clear this latch.

7) EENDWDT: (level-true low) Timer started at end of received event , if FE_CLR doesn't arrive before
the timer expires this fault will set. Event end Watchdog Timer.
Signals from Front-end to VRAM control logic

1) SER_EN#: (true-low) Serial enable line on VRAM chip to store header imformation.

2) SER_CLK: (true high) Serial clock line to VRAM chip to strobe in header data.

3) LHD[9:0]: (true high)Latched header data lines to VRAM.

4) HEADDONE: (level-true high) Set when header ends and reset by FE_CLR . Goes to VRAM control .

5)ABORTP: (pulse two link clocks wide-true low)Abort pulse used by VRAM logic .

Signals from Three ASIC boards to Front-end

1) FE_CLR: (true-high) Signal needed from all three ASIC boards before resetting busy state or Fault
conditions that caused an Interrupt.

2) FE_OE[1:0]: Gate signals from processors to enable reading the Front-end status registers.
(allows up to three eight bit registers)
status = FE_OE [01]
error = FE_OE [10]
spare = FE_OE [11]

3) SFTBSYA#: Soft busy from ASIC board "A". [Yellow LED]
SFTBSYB#: Soft busy from ASIC board "B". [Yellow LED]
SFTBSYC#: Soft busy from ASIC board "C". [Yellow LED]

4) CLRBSY0#: ASIC board "A"is busy [Green LED]
CLRBSY1#: ASIC board "B" is busy [Green LED]
CLRBSY2#: ASIC board "C" is busy [Green LED]

5) MCPURES_M1 CPU busy status[Red LED]
MCPURES_M1 CPU busy status[Red LED]
MCPURES_M1 CPU busy status[Red LED]

6) TPCMODE: Logic 1 selects TPC mode Logic 0 selects SVT mode

Status Register of CHER Front-end G-Link
The Status and Error Register Bytes are read only with latched flags reset on FE_CLR
(All signals are true-high)

7) LNKRDY- Link Ready signal from HP Receiver indicating the current state of the optical link .
Dynamic bit (true high)

6) Busy – The busy state is an ‘or’ of BUSYLAT # !LINKRDY(Link not ready) # SOFTBSY(any of three
soft busies) # CLRBSY (any of three Mezz. Busies) # LNKERR (a link error)
The BUSYLAT is set by a start event and is reset by FE_CLR or an abort command over the link.
The LINKRDY is a signal from the HP part and is filtered to generate one clean pulse at powerup.
SOFTBSY and CLRBSY are software controled
LNKERR is a latched ‘or’ of linkrdy and another signal (HPERR) from the HP part

5) spare 4)spare 3) spare
2) EOFEVNT- A full new event has been received
1) BST01- Two State bits to indicate the current stage of any event in progress.
0) BST00- IDLE(00), HEADER(01), DATA(10), ILLEGAL(11)

Error Register of CHER Front-end G-Link

7) LNKERR- A latched error flag set by link not ready or the receiver error logic (error pin).
The error logic is asserted when a frame is received that does not correspond to
either a valid Data, Control, or Fill frame encoding. A flag bit alteration error will
also cause an error to be latched. This is currently reset on power up and when an abort pulse is
received

6) BUSYERR- A start event was sensed while the busy state was active.(data overrun)
(See Busy status for details of busy)

5) WDTERR- Watch Dog Timer error, a latched error flag set when an event end is not sensed.

4) HEADBAD- A latched error flag set when the header block is not 64 words.
3) spare 2) spare 1) spare 0) spare

Glink Front -End Signals on CHER board.