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Module  CHERST1
Title   'MUX DATA FROM HP TO ASIC for CHER board, second part'

"-------------------------------------------------------------"
" This CPLD is used by CHERII and contains the following logic:    "
" 1)The Header block is checked for size and a strobe is generated "
"   on the 16th word for a pedestal clock [PEDCLK]                 "
" 2)The Header bad latch is here, output is [HBAD#]                "
" 3)The Busy error latch is here, output is [BERR#]                "
" 4)End of Event is a level generated output [EOFEVNT]             "
" 5)A signal is generated to put header data from the low half word"
"   on the high half for pedestal use, output is [XDATA]           "
" 6)A pulse is generated [CLRWDT#] to reset the event arrival WDT  "
"   on event end or FE_CLR# or PRWRST#                             "
" 7)A second pulse is generated[EECLR#] to reset the event process "
"    WDT on FE_CLR# or PRWRST#.                                    "
" 8)The signal [HEADCNT] is generated to latch the header data     "
"                                                                  "
" PATH: stardaq/home2/bob/powerview/cher1 cherst1.abl              "
" Fix xdata     6/2/98       cherst1.abl -I jedec file             "
"-------------------------------------------------------------"

" Inputs
"HPSTRB          PIN;"
ADJSTRB          PIN;
!HPCAVT          PIN;
!HPDAVT          PIN;
HPDA00           PIN;
HPDA01           PIN;
HPDA02           PIN;
"HPDA03          PIN;"
FE_CLR           PIN;
ST00             PIN;
ST01             PIN;
BUSY             PIN;"Input to check for data overrun and set busy fault."
ABORTP           PIN;
!CLRBSY0         PIN;
!CLRBSY1         PIN;
!CLRBSY2         PIN;
!LINKRDY         PIN;
TPCMODE  PIN;"Enable Pedestal strobe for TPC mode"
"!MRST   PIN_29; used for powerup reset, this gets 'ored' with FE_CLR"
"             and ABORT at the GLB level"
PLSI PROPERTY 'Y1_as_reset on';

" Outputs
HQ6..HQ0 node istype 'reg_T';
ST01D    node istype 'reg_D';
SEREN    node istype 'reg_SR';
PEDCLK   pin istype 'reg,buffer';
MRESET   node istype 'com';
HEADCNT  pin  istype 'com,buffer';
HEADCLK  node istype 'com';
HEADB15  node istype 'com';
EVTACT   node istype 'collapse';
EVTEND   node istype 'collapse';
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 57: EVTDONE  node  istype 'reg_D';
 58: HBADLAT  node  istype 'reg_D';
 59: BSYERR   pin  istype 'buffer';
 60: XDATA    pin  istype 'com,buffer';
 61: CLRWDT   pin  istype 'buffer';
 62: EECLR    pin  istype 'com,buffer';
 63: CLRBSY   pin  istype 'com,buffer';
 64: HEADDONE pin  istype 'reg,buffer';
 65: SER_EN   pin  istype 'com,buffer';
 66: EVTSTRT  pin  istype 'com,buffer';
 67: BSYERRL  node istype 'reg_D';
 68: HBAD     pin  istype 'com';
 69: EOFEVNT  pin  istype 'com';
 70: equations
 71:
 72: MRESET  = FE_CLR # !ABORTP;"Abortp polarity changed 1/29/98"
 73:
 74: " FE_CLR is the normal clear of busy and status flags after an event."
 75: " ABORT is a pulse received over the link if the event needs to be terminated"
 76: " for some reason. There is also a pulse on ABORT at powerup or on front"
 77: " panel reset to clear all status conditions."
 78:
 79: HEADCLK = ST00 & !ST01 & ADJSTRB & HPDAVT & !BSYERRL;"Clock for header counte
 80: HEADCNT = HEADCLK;"Use as strobe pulse for ext. memory"
 81: HEADB15 = HQ0 & HQ1 & HQ2 & HQ3 & !HQ4 & !HQ5 & !HQ6; "Header word fifteen"
 82:
 83: EVTACT  =!ST00 & ST01 & LINKRDY & !BSYERRL;" start WDT and latch HEADDONE"
 84: HEADDONE.D = EVTACT;
 85: HEADDONE.CLK = ADJSTRB;
 86: HEADDONE.AR = MRESET;
 87: EVTSTRT = EVTACT;
 88: PEDCLK.D  = ST00  & HEADB15 & !TPCMODE;"PED_OFFSET_CLK used by SVT"
 89: PEDCLK.CLK = ADJSTRB & HPDAVT;
 90: EVTEND  = HPCAVT & HPDA02 & ADJSTRB & LINKRDY;
 91:
 92: "        Latch Event end State       "
 93: EVTDONE.D =!BSYERRL;
 94: EVTDONE.CLK = EVTEND;
 95: EVTDONE.AR  = MRESET;
 96: EOFEVNT = !EVTDONE;
 97: XDATA  = (ST00 & !ST01 & !TPCMODE);"mux low 10 bits to both asics(SVTMODE)"
 98: CLRWDT =!(EVTDONE # MRESET);
 99: EECLR  = !MRESET;
100: "Header Counter, used to select word 16 for PED_OFFSET_VALUE"
101: "                and check for exactly 64 words."
102: [HQ6..HQ0].CLK = HEADCLK;
103: [HQ6..HQ0].AR = MRESET # !LINKRDY;
104: HQ6.T = HQ5 & HQ4 & HQ3 & HQ2 & HQ1 & HQ0;
105: HQ5.T = HQ4 & HQ3 & HQ2 & HQ1 & HQ0;
106: HQ4.T = HQ3 & HQ2 & HQ1 & HQ0;
107: HQ3.T = HQ2 & HQ1 & HQ0;
108: HQ2.T = HQ1 & HQ0;
109: HQ1.T = HQ0;
110: HQ0.T = 1;
111:
112: " 'or' three busy signals for CHERST2 logic"
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113: " busy is cleared when all signals are low"
114:
115: CLRBSY = CLRBSY0 # CLRBSY1 # CLRBSY2;
116:
117: "Enable VRAM for header information"
118: ST01D.D   = ST01; "Delay turnoff for last header word"
119: ST01D.CLK = ADJSTRB;
120: SEREN.CLK = ADJSTRB;
121: SEREN.S  = ST00;
122: SEREN.R  = ST01D;
123: !SER_EN  = SEREN;
124:
125: "Latch bad Header length"
126:
127: HBADLAT.CLK = HPCAVT & HPDA01 & ADJSTRB & !BSYERRL;
128: HBADLAT.D   = !(HQ6 & !HQ5 & !HQ4 & !HQ3 & !HQ2 & !HQ1 & !HQ0);
129: HBADLAT.AR  = MRESET;
130: HBAD        = !(HBADLAT # !LINKRDY);
131:
132: "Latch a busy error if start of event is received while still busy"
133:
134: BSYERRL.CLK = HPCAVT & HPDA00 & ADJSTRB;
135: BSYERRL.D   = !BUSY;
136: BSYERRL.AR  = MRESET;
137: BSYERR    = !(BSYERRL # !LINKRDY);
138: end
139:
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