Trigger Level 0 Architecture: TCU and DSM Boards

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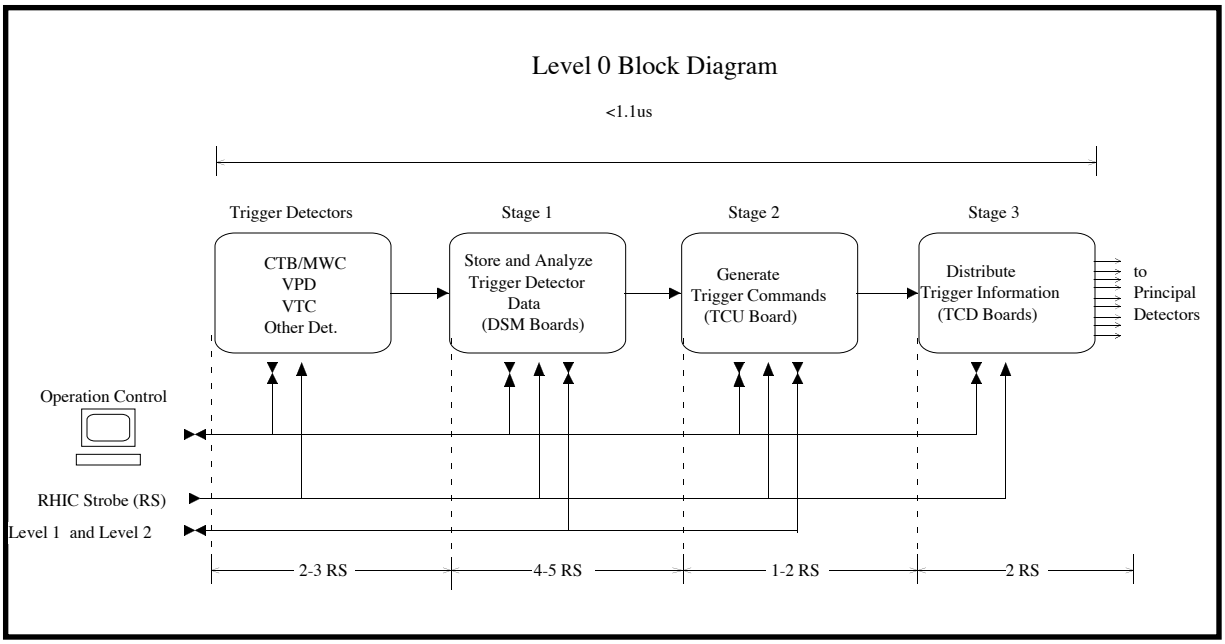
1.0 Introduction

FIGURE 1. Level 0 Block Diagram



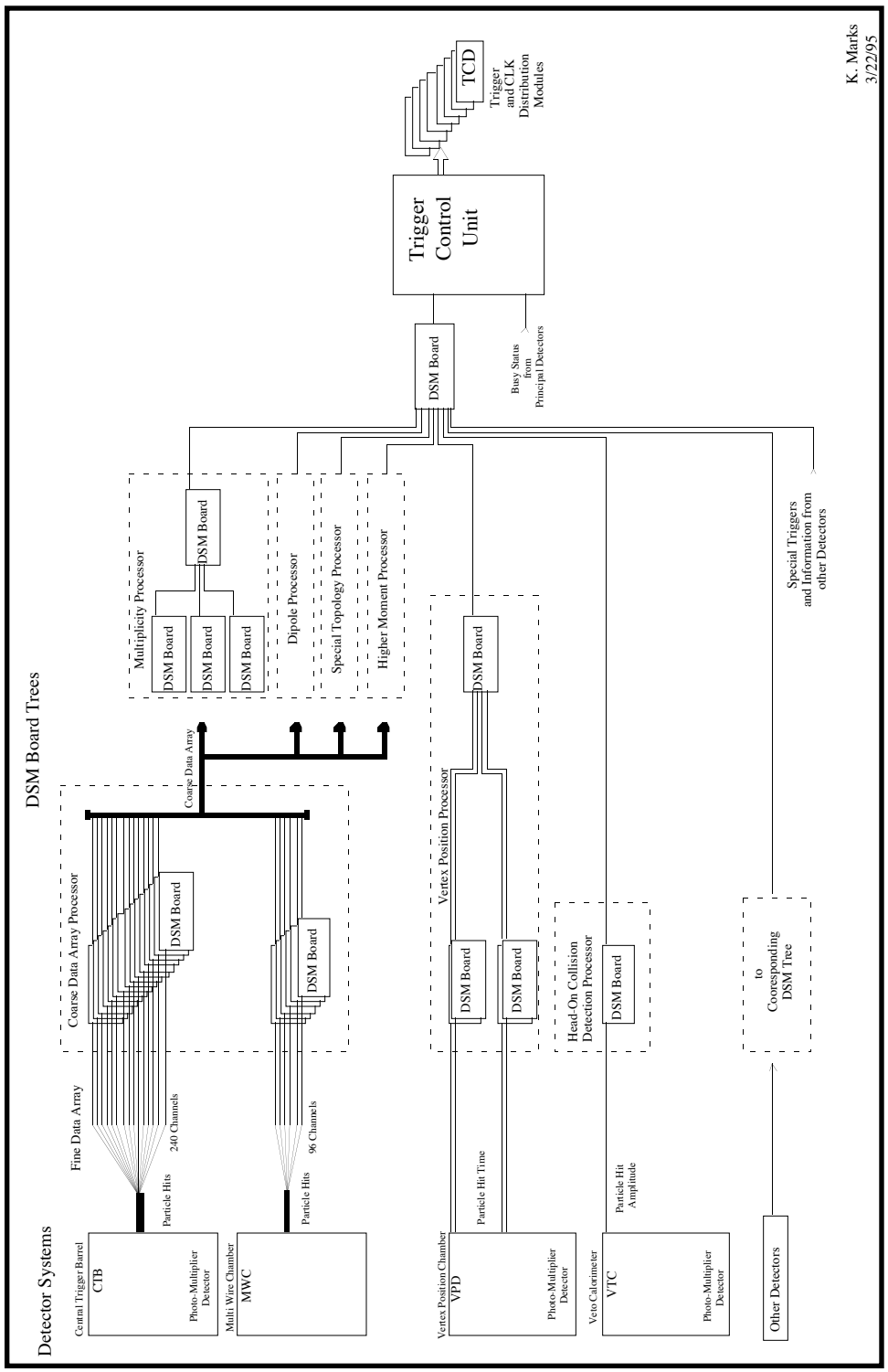
Level 0 is the first stage in the production and processing of STAR triggers. It is the origin of all commands to take data; subsequent levels can only abort events, and they do that by asking Level 0 to send an abort command. Additionally, Level 0 must store all data delivered by the trigger detectors, and process this data within 1 μs.

In order to meet these various requirements, Level 0 is pipelined and split into three stages (see figure 1). The first stage stores the trigger detector data and executes the appropriate algorithms. The second stage produces an event description based on the outputs of Level 0 analysis and generates trigger commands. The third stage distributes these trigger commands and two user defined clocks to the detector systems. These three stages are implemented with three corresponding boards: the Data Storage and Manipulation Board, the Trigger Control Unit, and the Trigger and Clock Distribution Board.

2.0 The Data Storage and Manipulation Board

The Data Storage and Manipulation Board is a 9U VME module designed to store and process data supplied by the trigger detectors. It is configured to accept 128 input bits and output 32 bits. The board is being designed to operate in one RHIC Strobe (RS-110ns). By connecting several DSM boards, Level 0 algorithms are pipelined as illustrated in figure 2.

FIGURE 2. DSM Board Trees



Note that the output of the CTB combined with the output of the MWC is treated as a single virtual detector. The output of these two detectors is summed in a tree of DSM boards. The first level of summation is referred to as the coarse pixel array and is used for multiplicity analysis, special topology analysis, dipole analysis, and higher moment analysis. The coarse pixel array is read out by Level 1 processors in addition to the outputs of the individual DSM trees. Level 2 processors read out all 396 channels of raw detector data in addition to the outputs of the individual DSM trees.

The data from the VPD system is used to calculate where the collision occurred in the TPC and compared to a window to determine if interaction falls within the region of interest. The VTC detectors are used to check that a bunch crossing caused a central collision.

2.1 Data Receiving Section

The DSM board accepts 128 inputs (that can be structured as sixteen 8-bit channels) received on eight connectors on the rear of the VME board (see figure 3). It will also accept simulated data to facilitate system and board debugging. Simulated data is downloaded by Operation Control over VME; 32 KBytes per channel are provided for the storage of this data. The data on the input connectors is multiplexed with the data from simulation memory, allowing the board to be configured to accept either as input.

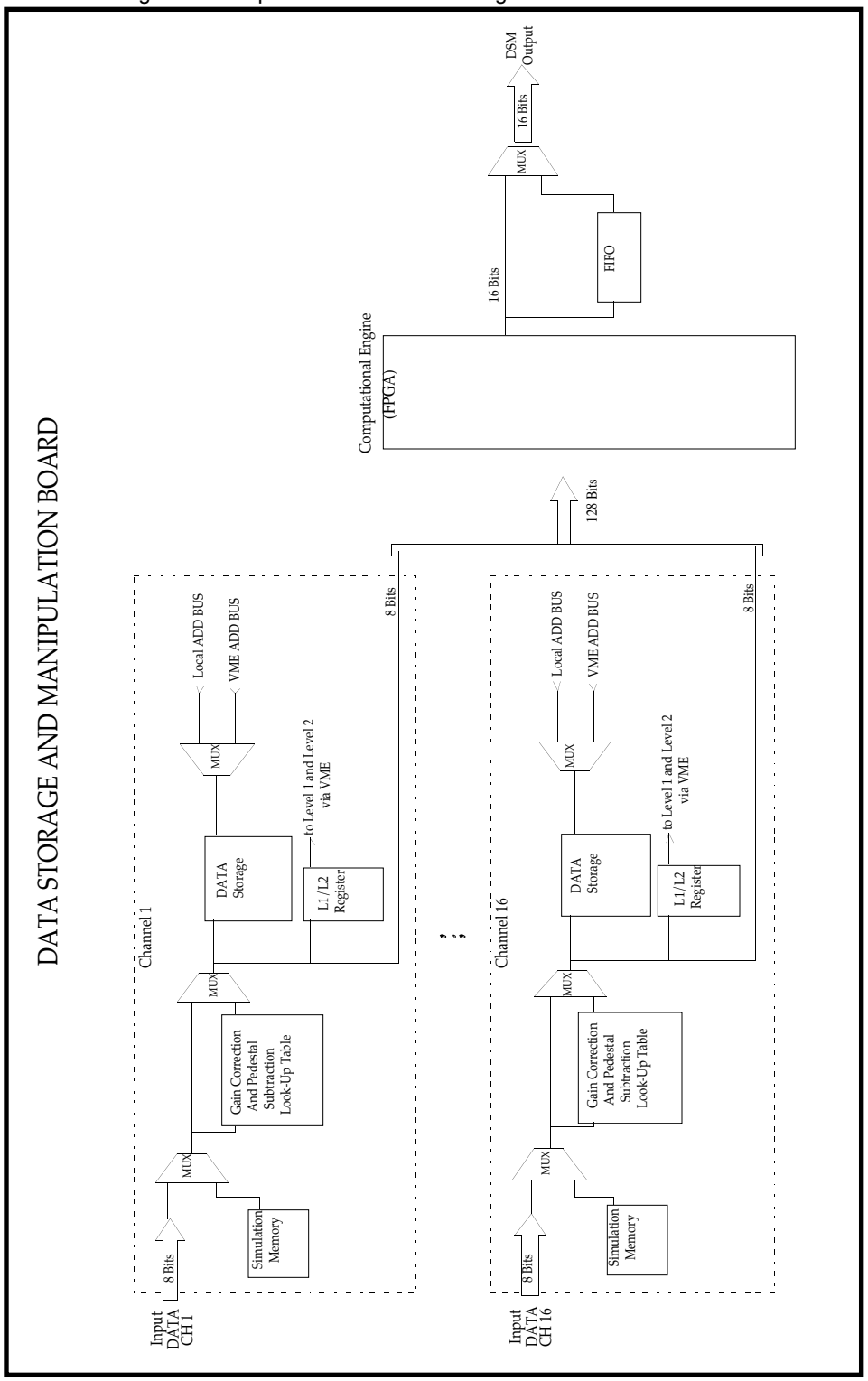
Each channel's input, simulated or real, is fed to a "Gain Correction and Pedestal Subtraction" Look-Up Table (LUT). The DSM board can be configured to use sixteen 8-bit LUTs or eight 16-bit LUTs as illustrated in figure 4. The 8-bit LUTs map to an 8-bit word and the 16-bit LUTs map to a 16-bit word. The output of either type of LUT is made available for board storage. Although the 128 input bits can be configured in anyway, the LUTs are only meaningful when the data is structured as eight or sixteen bit words. Otherwise, the LUTs should be loaded in such a manner that the input is passed, unchanged, to the output. The LUTs are loaded by Operation Control over VME.

2.2 Data Storage Section

The DSM board must store all data for future examination. It uses 64 KBytes of memory per channel as a cyclical storage ring in which all data is held for 7ms before being overwritten. (7ms was calculated as an upper bound for Level 1 and Level 2 to access the data necessary for their processing.) For this data to be useful, an address pointer must be uniquely associated with each event. To synchronize the address pointer of every DSM board, an "Address Pointer Reset" will be distributed to all boards. The value to which a board's pointer is reset corresponds to its depth in the tree, enabling all data from one crossing to be stored in the same memory location.

Level 1 and Level 2 also have read access, over VME, to the memory on each DSM board. Incoming data is given priority, and any read request from VME is held off until a write cycle is complete. The use of high speed (20ns) memory ensures that between every RHIC Strobe there is ample time to do both read and write cycles. Access times are further improved through the use of a temporary register for every channel.

FIGURE 3. Data Storage and Manipulation Board Block Diagram

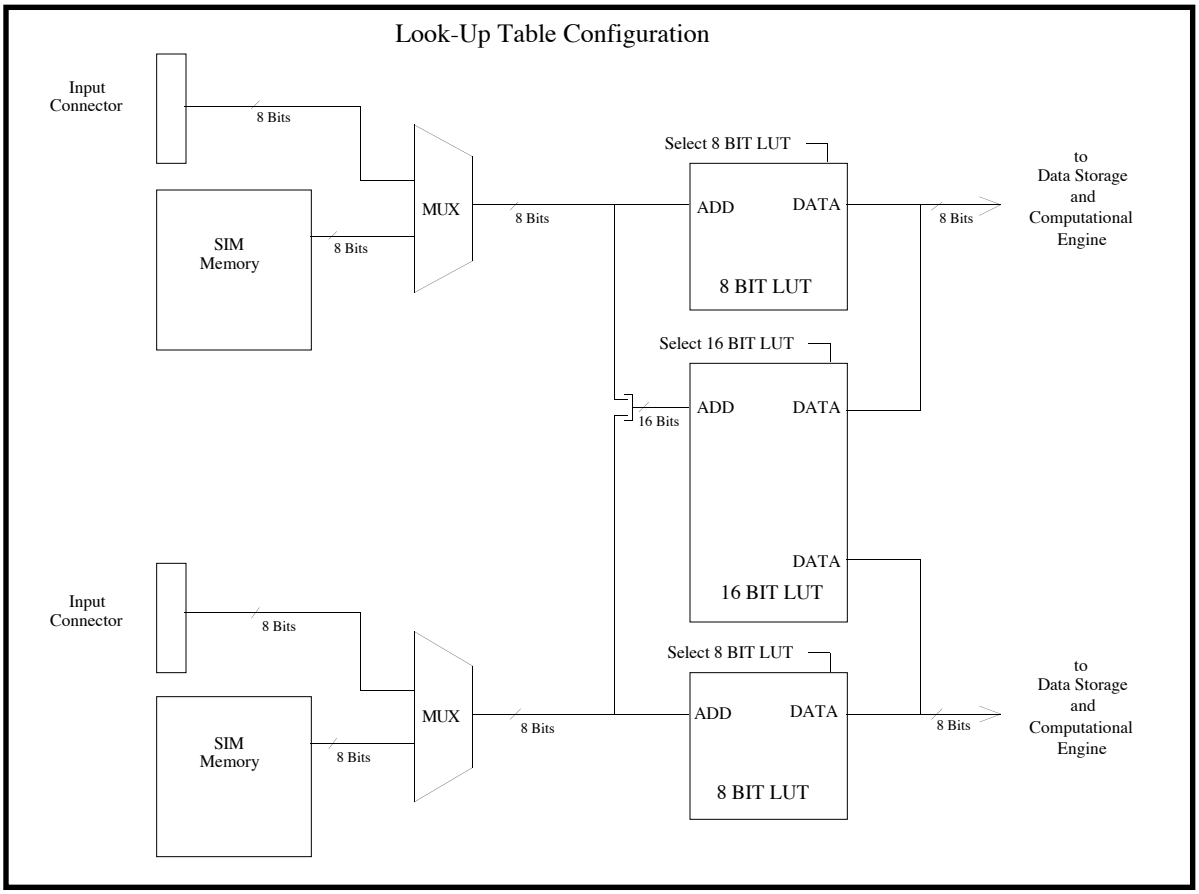


The temporary register is written whenever the DSM boards receive an appropriate “broadcast” over VME. (A VME “broadcast” is a method of communicating with several slaves simultaneously, and can only be used to distribute write commands). This broadcast specifies a particular event by placing its address on the VME Data Bus. Recipient DSM boards shift the data from that address on each channel into their temporary registers. Level 1 and Level 2 are then able to have continuous access to these without the delays associated with shared memory and are able to do block reads.

2.3 Computational Section

Each DSM board has one computational engine where the 16 channels of received data are manipulated according to a downloaded algorithm. This engine is implemented using a Field Programmable Gate Array (FPGA), thereby enabling unique algorithms to be loaded onto individual DSM boards, and also allowing these algorithms to change. Operation Control configures each FPGA by pushing a serial bit stream over VME. The computational engine (FPGA) has 128 inputs and outputs a 32 bit word. Because the DSM board has one RS from input to output, the FPGA has to perform all Level 0 algorithms in less than 80ns. The output of the FPGA is stored in a FIFO which can be accessed for board debugging and which can be used to drive the output of the DSM board.

FIGURE 4. Look-Up Table Configuration



2.4 Output Section

The output of every DSM board is connected to either another DSM board or to the next stage of Level 0. Each DSM board can be configured by Operation Control to either drive the output directly with the results of the FPGA or to drive it via a FIFO. In most cases the output can be driven directly from the FPGA, but in the instance where there are DSM Trees of varying length, the output is passed through the FIFO.

It is necessary for the output of all merging trees to be based on the same bunch crossing so that all the information provided to the next stage is consistent. This behavior is facilitated through the use of the output FIFO. The FiFos on the last DSM boards of shorter trees are preloaded with "space holders." For example, if a tree with three stages and one with a single stage are to be merged, then the FIFO ending the single stage tree would be loaded with two space holders. By the time the tree with three stages outputs its results, the FIFO of the short tree will have discarded its two space holders and will be ready to output a corresponding result.

3.0 Trigger Control Unit

The Trigger Control Unit (TCU) is a 9U VME module designed to produce Trigger Commands (see figure 4). It is the only stage in the trigger system from which triggers are issued. Triggers, generated every RHIC Strobe, include a Trigger Command, a DAQ Command, a Detector Bitmask, and a Token. The Trigger Commands that are distributed are shown in table 1. "Initiate Event" and "Ignore Event" Commands are produced according to the analysis done by the DSM boards, the "busy" status of the detectors, and prescale values. Abort and Accept Commands are received from Level 1, Level 2, and Level 3 and are stored on the TCU board until they can be issued. The TCU also stores "Initiate Event" Commands for Level 1 to access for further processing.

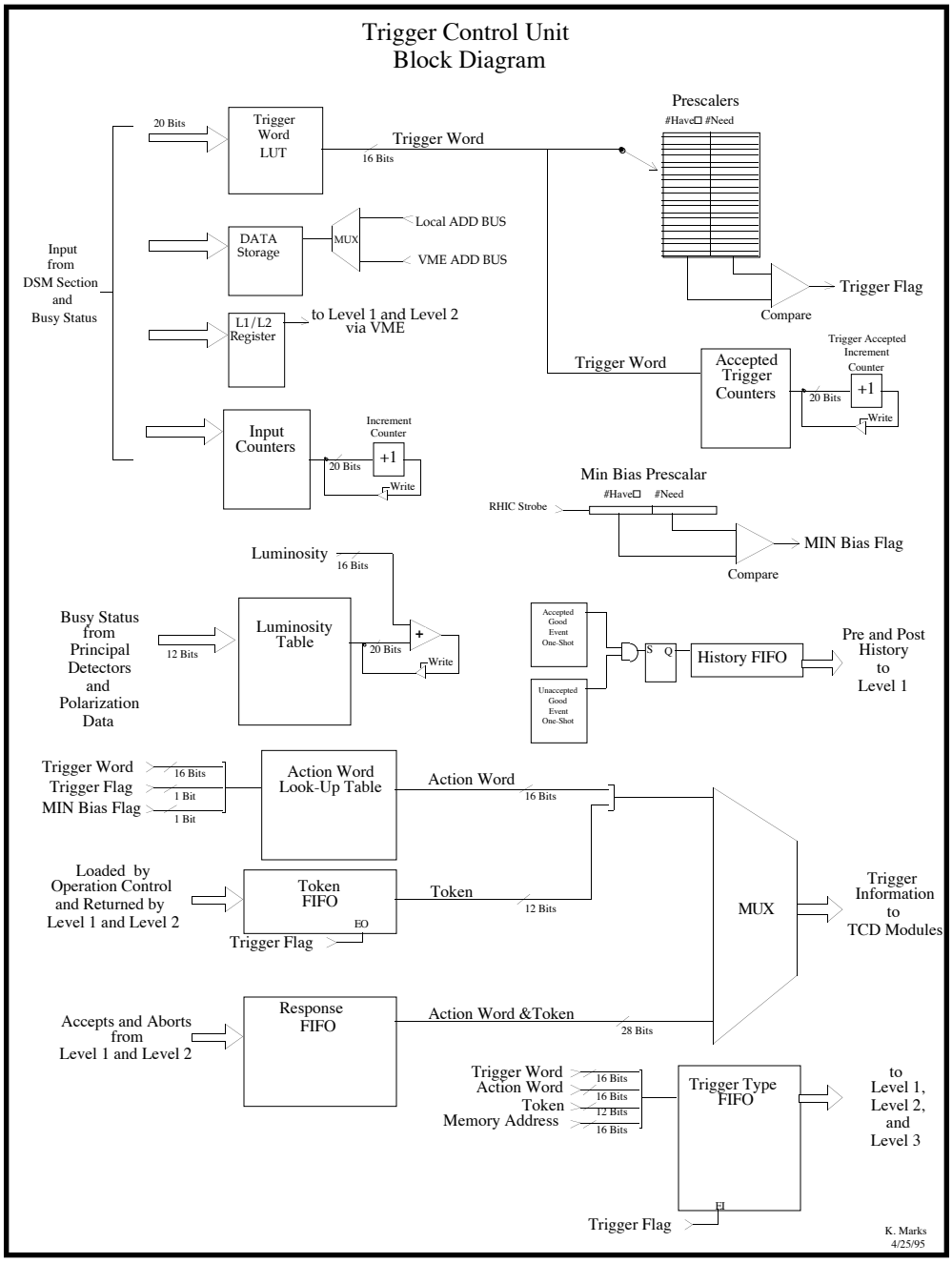
TABLE 1. Trigger Commands

0000	Ignore Event
0001	Initiate Event
0010	Abort Event
0011	Accept Event

3.1 Storage and Look-Up Table

The final DSM board gathers the outputs of the preceding DSM trees along with the special event information from the Detector Systems (see figure 2). Its FPGA is configured to produce a 12 bit word which is used to summarize the physics analysis done by the DSM trees. This 12 bit word, combined with the 8 bits of "Busy Status" from the Detector Systems, is received by the TCU and referred to as the "Trigger Input Word." The Trigger Input Word is stored in memory to which an address pointer and register are associated in the same fashion as the DSM boards. There is also a counter associated with each Input Word that is incremented whenever that word is received. The contents of these counters can be shifted to temporary buffers to be read over VME. In addition, the TCU uses a Look-Up table to translate this Input Word into another 16 bit word called the Trigger Word. The Trigger Word names the kind of event that has occurred, and its Look-Up Table is built by Operation Control over VME.

FIGURE 5. Trigger Control Unit Block Diagram



3.2 Trigger Prescaler

To each Trigger Word there is associated a unique prescaler which is set by Operation Control over VME. The purpose of this prescaler is to control the rate of accepted events with a particular trigger word. If the prescale factor for a Trigger Word is n, then every nth event described by that Trigger Word will be accepted. This function is implemented via a 64KWord table that is loaded by Operation Control with 20 bit prescale factors for every nonzero Trigger Word. The TCU board also stores in this table the number of each type of Trigger Word generated. Every RHIC Strobe, the TCU accesses the prescaler associated with the current Trigger Word and compares it to the number previously received. If these numbers are equal the Trigger Flag is set, the event is accepted, and the counter is reset; otherwise the event is rejected and the counter is incremented.

There is also an "Accepted Trigger" Counter for each Trigger Word. This counter is incremented whenever its corresponding Trigger Word is "accepted", i.e. causes an event. The contents of the Accepted Trigger Counters can be shifted to temporary buffers for access over VME.

To enable the system to automatically acquire a minimum number of events (regardless of the physics) the TCU also generates a minimum bias trigger. This is implemented with a 24 bit prescaler and a counter that is incremented every RHIC Strobe. When these match it sets a Minimum Bias Flag that is used to initiate an event for all non-busy detectors.

3.3 Trigger History

The TCU determines if there were additional interactions before or after a TPC Initiated Event. This is accomplished through the firing of a one-shot whenever a TPC event is initiated. (The output of the one-shot corresponds to the drift time through the TPC.) Another one-shot is fired whenever an event occurs that is not initiated. If both one-shots are ever simultaneously true, then a bit is set in the "History FIFO" to indicate that the Initiated Event has been corrupted. Level 1 reads the contents of this FIFO over VME when processing TPC Initiated Events.

3.4 Action Word Look-Up Table and Tokens

The Action Word Look-Up Table is loaded by Operation Control and is used to translate the Trigger Word and Flags to an Action Word. The Action word is a combination of a four bit Trigger Command, a four bit DAQ Command, and an eight bit Detector Bitmask.

If the Trigger Flag has been set, the TCU allows the assignment of a nonzero token to this Action Word. Tokens are unique 12 bit words that are held in a FIFO by the TCU, with a new one assigned to every accepted event. This FIFO is initially loaded by Operation Control, and if it should become empty no further events are accepted until a token is returned to the FIFO. This constraint allows control over the total rate of accepted events. When an event has finished being taken or is aborted, Level 1, Level 2, or DAQ return the associated event token, allowing its reuse. The Token FIFO is 2^12 deep to accommodate the maximum number of tokens that could be needed by the trigger system.

All detectors receive the Action Word and Token, allowing them to decide if they are required to initiate or abort an event. The TCU puts these two words on VME connector P3, allowing them to be distributed by the Trigger and Clock Distribution Board.

3.5 Luminosity Table

The eight detector "Busy Status" bits combined with the four "Polarization" bits describe 4096 possible configurations, and to each of these is associated a number in the "Luminosity Table." Every RHIC Strobe the received Luminosity (16-bits) for that beam crossing is summed into the appropriate slot of the Luminosity Table. If the TCU receives a command to read out the Luminosity Table, it copies the contents to a temporary buffer for access over VME. The stored summations are thus made available without their acquisition being disrupted.

3.6 Level 1 and Level 2 Handshake

For every nonzero token, the Action Word and Token get stored along with the Trigger Word and the corresponding Event Memory Address in the "Trigger Type FIFO." The Memory Address is the location of a given event on the DSM board. (This address can be simultaneously reset on all DSM boards.) Level 1 accesses the Trigger Type FIFO and begins processing the associated event.

When Level 1 or Level 2 decide to abort or accept an event, the TCU is given the corresponding event Token and Action Word. This information is stored on the TCU board in it's "Response FIFO." Whenever the Trigger Flag is false (i.e. no trigger needs to be issued for this RS), the TCU issues any Abort or Accept Commands waiting in the Response FIFO (or a "Ignore Event" command if it is empty) for distribution to all detectors.