DAQ EMC Receiver Board's Manual

Date: May 24, 2001
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Version 1.1

Board Registers

	Address (hex)
Universe	28080000

Mezzanine Fibers

Fiber 0 (A or lowest)	**Address (hex)**
Control Registers	28000000
PLX Controls	28040000
Memory	10000000

Fiber 1 (B)	**Address (hex)**
Control Registers	28010000
PLX Controls	28050000
Memory	10800000

Fiber 2 (C)	**Address (hex)**
Control Registers	28020000
PLX Controls	28060000
Memory	11000000

Fiber 3 (D or upmost)	**Address (hex)**
Control Registers	28030000
PLX Controls	28070000
Memory	11800000

** The Towers Receiver Board has only one fiber, which then maps to Fiber 0 (A).*

Memory

Each board has 256 kBytes (2 X 16 X 64 kb SRAM) of memory organized in 32 buffers of 8192 bytes each.

The first 4 bytes in the event buffer are junk – ignore them. They are an artifact ("feature") of the SRAM chip used.

The data is structureless – there is no difference between the "STAR Header" and the data. There are no special boundaries and the Header data is not treated or used in any special way. In effect, the Start Of Data CAV is plainly ignored.

The data is stored as it arrives on the fiber. No assumptions are made about the "packet" size. The End Of Data CAV is only used for interrupt generation and doesn't delimit the data in any other way. This in turn means that if one sends more DAVs then expected they would most likely overwrite some port of the previous/next event.

The bits of the memory image follow the bits of the Glink fiber i.e. Glink fiber bit 0 is stored in bit 0 of the memory. *Be careful about the endianess of your machine!*

SMD Data Format

The data appears in consecutive memory locations as it appears on the fiber. The data from each fiber strobe (DAV) is sent to a 4 byte memory location: the least significant 10 bits of the fiber data go to the least significant 10bits of the memory location. The next significant 10 bits of the fiber go to bits 16-25. The unused memory bits are zeroed on input.

Thus for example:

DAV (counts from 1)	Memory Address	Upper 10 Glink bits	Lower 10 Glink bits	Resulting 32 bits (little endian)
1	0x00000004	0x3FF	0x3FF	0x03FF03FF
2	0x00000008	0x123	0x321	0x01230321
5	0x00000014	0x3AB	0x298	0x03AB0298

Towers Data Format

The data appears in consecutive memory locations as it appears on the fiber. The data from each fiber strobe (DAV) is sent to a 2 byte memory location with the upper 4 bits of the 20 bit fiber word masked out.

Thus for example:

DAV (counts from 1)	Memory Address	Upper 10 Glink bits	Lower 10 Glink bits	Resulting 16 bits (little endian)
1	0x00000004	0x3FF	0x3FF	0xF3FF
2	0x00000006	0x123	0x321	0x3321
5	0x0000000E	0x3AB	0x298	0xB298

Registers

Each fiber has 3 6 bit registers in the Control Register Space mapped on 4 byte boundaries.

The remaining 2 bits are junk so be careful to mask them off!

Interrupt/Status Register (offset 0x0)

Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RW	RW	RW	RW	RW	RW
LSERR	DAQERR	ABORT	EVTEND	DSTART	ESTART

A write of '1' clears the bit.
A read of '1' means that it is asserted (TRUE).

ESTART Start of Event CAV latched.
DSTART Start of Data CAV latched.
EVTEND End of Data CAV latched.
ABORT ABORT CAV latched.
DAQERR a) Link Error or Link not Ready
b) BUSY Overrun – a new Start of Event fired while the BUSY was ON
NOTE: Clearing DAQERR will not clear the cause of the error! One must at least issue a CLEAR command in the Status/Command Register.

LSERR PLX Board Failure (PLX LSERR#)

EVTEND or DAQERR or LSERR cause the LINTI# pin of the PLX to be asserted which in turn fires a VME interrupt.
The ABORT is directly routed to the Universe and will also cause a different VME interrupt to fire (if enabled in the Universe).

Universe LINTI# routing and Interrupt Level assignment

SMD Board

- PLX A is routed to LINT4#; ABORTS to LINT0#
- PLX B is routed to LINT5#; ABORTS to LINT1#
- PLX C is routed to LINT6#; ABORTS to LINT2#
- PLX D is routed to LINT7#; ABORTS to LINT3#

Tower Board

- All PLX interrupts are routed to LINT3# *[which is unfortunate – they should have been routed to LINT4# for consistency with the SMD Receiver]*
- ABORTS are routed to LINT0#

Command/Status Register (offset 0x4)

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RO	RO	RO	WO	RW	RO
0	0	DAQERR	CLEAR	SOFT_ BUSY	BUSY

A read of '1' means that it is asserted (TRUE).

BUSY Shows the state of the BUSY output signal.
SOFT_BUSY '1' Force BUSY TRUE
'0' Release Force BUSY
CLEAR Writing a '1' resets the Fiber Logic
DAQERR Same as in the Interrupt register

Buffer Register (offset 0x8)

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RW	RW	RW	RW	RW	RW
-	-	-	-	-	-

The value (0-31) of the current buffer in effect, which is used for writing data from the fiber.